11-7025-202-34

TM 11-7025-202-34

TECHNICAL MANUAL

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL

MULTIPLEXER TD-976/G (NSN 7025-01-048-9678)

This copy is a reprint which includes current pages from Changes 1 and 2.

HEADQUARTERS, DEPARTMENT OF THE ARMY
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WARNINGS

Potentially *lethal* voltages are present within the TD-976/G and the TD-982/G. These voltages can be present within the TD-976/G even when the equipment is turned off. Always observe the WARNINGS and CAUTIONS throughout the manual when making electrical interconnections and performing maintenance functions within the TD-976/G.

115 VOLTS AC

The 115-volt ac primary power is always applied to TB1 in the card file and to S9 on the front panel when the power cable is connected between the ac power source and the TD-976/G. Always disconnect the power cable when working in the TD-976/G.

400 VOLTS DC

Cable drive power of 400 volts dc with a constant current of 45 milliamperes may be present in the equipment when the POWER IN and POWER OUT indicators are lit. The high voltage can be generated within the unit or the voltage may be applied from another TD-976/G that is connected to the unit being serviced.

HIGH-VOLTAGE CAPACITORS

Wait at least 15 seconds after cable power is removed from the TD-976/G to ensure that high-voltage capacitors in the unit are discharged.

CHANGE)
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No. 2)

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Maintenance Manual
MULTIPLEXER TD-976/G (NSN 7025-01-048-9678)

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MULTIPLEXER TD-976/G (NSN 7025-01-048-9678)

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3-3 and 3-4	3-3 and 3-4
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FO-9 (sheet 3)	FO-9 (sheet 3)
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FO-14 (sheet 1)	FO-14 (sheet 1)
FO-17 (sheet 1)	FO-17 (sheet 1)
FO-20 (sheet 1)	FO-20 (sheet 1)

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- Sig Sec USA Dep (1)
- Ft Richardson (CERCOM Ofc) (2)
- Units org under fol TOE:
  - 29-207 (2)
  - 29-610 (2)

NG: None
USAR: None
For explanation of abbreviations used, see AR 310-50.

TECHNICAL MANUAL

No. 11-7025-202-34

HEADQUARTERS
DEPARTMENT OF THE ARMY
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DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL

MULTIPLEXER TD-976/G

(NSN 7025-01-048-9678)

REPORTING OF ERRORS

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NOTE

The Remote Access Unit (RAU). 21A15, and the Digital Data Orderwire Printed Circuit Board, 21A8, have been removed from the TD-976/G; they are no longer required. Any reference or illustration of these items or of their associated equipment such as RAU Feedthru Box or the RAU Breakout Box within this technical manual must be disregarded.

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope

a. This manual contains functional descriptions and direct support and general support maintenance instructions for Multiplexer TD-976/G (hereafter referred to as the TD-976/G). Chapter 2 contains functional descriptions of the equipment. Chapters 3 and 4 contain detailed direct support and general maintenance instructions.

b. Sections I through III of chapter 2 contain general discussions of the TD-976/G interfaces, the supergroup (SG) message formats, and the basic equipment concepts. Section IV of chapter 2 is devoted to an overall block diagram discussion of the TD-976/G. Additional sections of chapter 2 contain detailed block diagram and logic/schematic discussions for each plug-in printed circuit card and the power supply.

c. The direct support maintenance instructions in chapter 3 consist of detailed testing, troubleshooting, and performance tests for the overall TD-976/G, the front panel, and the remote access unit (RAU). Also, maintenance instructions for repair of the assemblies that make up the TD-976/G, less the plug-in printed circuit cards, are included in chapter 3. Detailed troubleshooting and repair of the plug-in printed circuit cards is a depot level function and instructions are contained in DMWR 11-7025-202. The general support maintenance instructions in chapter 4 consist of detailed testing, troubleshooting, and performance tests for the power supply. Also, maintenance instructions for repair of the power supply are included in chapter 4.

1-2. Maintenance Forms and Records

Department of the Army forms and procedures used for equipment maintenance will be those prescribed in TM 38-750.

1-3. Destruction of Army Materiel To Prevent Enemy Use

Refer to TM 750-244-2 for procedures to be followed for destruction of materiel to prevent enemy use.

1-4. Administrative Storage

Refer to TM 740-90-1 for procedures, forms, records, and inspections required during administrative storage of the TD-976/G.

1-5. Reporting Equipment Improvement Recommendations (EIR's)

EIR's will be prepared using SF 368, Quality Deficiency Report, Maintenance Request. Instructions for preparing EIR's are provided in TM 38-750, The Army Maintenance Management System. EIR's should be mailed direct to Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEL-ME-MQ, Fort Monmouth, NJ 07703. A reply will be furnished direct to you.

Section II. DESCRIPTION AND DATA

1-6. Equipment Description

Physical descriptions and illustrations of the TD-976/G are contained in TM 11-7025-202-12. Additional equipment descriptions and illustrations needed for direct support maintenance of the TD-976/G are contained in chapter 3. General support maintenance information is contained in chapter 4.

1-7. Tabulated Data

The operating characteristics and physical dimensions of the TD-976/G are contained in the tabulated data in TM 11-7025-202-12.

1-8. Common Names and Reference Designations

Common names and reference designations for major components of the TD-976/G are listed in table 1-1. The plug-in printed circuit cards are assigned reference designations 21A1 through 21A11 (common multiple use plug-in cards are assigned the same reference designation). The common names listed in the "Common name" column of table 1-1 are the abbreviated names used throughout the manual for these items. The "Card connector" column lists the reference designation (J number) of each connector in the card file into which a printed circuit card is plugged.

1-9. Common Terms

The common terms used in this manual in discussions of various data handling functions are defined in the glossary.

1-10. Signal Names

a. The functional signals used in the TD-976/G are assigned signal names in the form of mnemonic codes (in most cases, formed from initial letters or syllables of selected words) chosen to convey useful information. The signal names and their definitions are listed in table 1-2. Additionally, the card or assembly that generates the signal is listed in the "Source" column of table 1-2 while the card (or cards) and/or assembly (or assemblies) to which the signal is applied are listed in the "Destination(s)" column.

b. A bar (—) indicator appears at the end of selected signal names. When shown on a block or schematic diagram or in text, the bar indicator means that the negative (low) level of the signal is the true condition required for the specific logic function being performed.

c. The mnemonic CT (card test) appears frequently at card input/output pins on the logic diagrams. These particular card pins are used only during card testing. Therefore, the mnemonic CT is not listed in table 1-2.

Table 1-1. Reference Designations and Common Names

Reference designation	Item	Common name	Card connector
21A1	Alarm detector card.	AD.	J31
21A2	Group traffic monitor card.	GTM.	J32
21A3	Digital data orderwire encoder card.	DDOW encoder.	J33
21A4	Master oscillator/combiner card.	MO/C.	J34
21A5	Timing and control card (mux).	TC (M).	J35
21A5	Timing and control card (demux).	TC (D).	J40
21A6	Dual group processor card No. 1.	DGP No. 1.	J36
21A6	Dual group processor card No. 2.	DGP No. 2.	J37
21A6	Dual group processor card No. 3.	DGP No. 3.	J38
21A6	Dual group processor card No. 4.	DGP No. 4.	J39
21A7	Frame sync card.	FS.	J41
21A8	Digital data orderwire decoder card.	DDOW decoder.	J42
21A9	Supergroup driver/receiver card.	SG D/R.	J43
21A10	Analog voice orderwire card.	AVOW.	J44
21A11	Digital voice orderwire card.	DVOW.	J45
21A12	Power supply.	Power supply.	
21A13	Card file assembly.	Card file.	
21A14	Control panel assembly.	Front panel.	
21A15	Remote access unit.	RAU.	

Table 1-2. Signal Names and Definitions

Signal name	Definition	Source	Destination(s)
AALRM--	Audible alarm.	AD.	Front panel.
AARSSW	Audible alarm reset switch.	Front panel.	AD.
ACHOT	Alternating current hot.	AC input.	Front panel.
ACHOTO	Alternating current hot output.	Front panel.	Power supply.
ACNEUT	Alternating current neutral.	AC input.	Front panel.
ACNEUTO	Alternating current neutral output.	Front panel.	Power supply.
ACT (CH A)	(Refer to ACT 1 through ACT 4.)		
ACT (CH B)	(Refer to ACT 5 through ACT 8.)		
ACT 1	Activity select group 1 (CH A).	DGP No. 1.	GTM.
ACT 2	Activity select group 2 (CH A).	DGP No. 2.	GTM.
ACT 3	Activity select group 3 (CH A).	DGP No. 3.	GTM.
ACT 4	Activity select group 4 (CH A).	DGP No. 4.	GTM.
ACT 5	Activity select group 5 (CH B).	DGP No. 1.	GTM.
ACT 6	Activity select group 6 (CH B).	DGP No. 2.	GTM.
ACT 7	Activity select group 7 (CH B).	DGP No. 3.	GTM.
ACT 8	Activity select group 8 (CH B).	DGP No. 4.	GTM.
ADCT01	AD card test loop 1.	. .[1]	. .[1]
ADCT02	AD card test loop 2.	. .[1]	. .[1]
ADCT03	AD card test loop 3.	. .[1]	. .[1]
ALRMT	Alarm test.	AD.	AVOW.

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
APAT 1	Activity pattern 1.	GTM.	DGP No. 1. DGP No. 3.
APAT 2	Activity pattern 2.	GTM.	DGP No. 2. DGP No. 4.
AVCAL—	Analog voice call.	AVOW.	AD.
AVCALS	Analog voice call signal.	AD.	Front panel.
AVCT01	AVOW card test loop 1.	..[1]	..[1]
AVEMPR	Analog voice EMP receive.	21A13T2.	SG D/R.
AVEMPT	Analog voice EMP transmit.	SG D/R.	21A13T1.
AVRNG—	Analog voice ring.	..[1]	AVOW.
CABFLT	Cable fault.	SG D/R.	AVOW.
CFNRM—	Cable fault normal.	Front panel.	AVOW. SG D/R.
CHAN	Channel clock (4608 kHz).	MO/C.	DGP's.
CMBUS	Common bus.	RAU.	AVOW.
CNSAUD—	Console audible.	AD.	RAU.
DDCAL—	Digital data call.	DDOW decoder.	AD.
DDCALS	Digital data call signal.	AD.	RAU.
DDCLK	Digital data clock (4915.2 kHz).	MO/C.	DDOW encoder.
DDCT01	DDOW decoder card test loop 1.	..[1]	..[1]
DDCT02	DDOW decoder card test loop 2.	..[1]	..[1]
DDCT03	DDOW decoder card test loop 3.	..[1]	..[1]
DDCT04	DDOW decoder card test loop 4.	..[1]	..[1]
DDCT05	DDOW decoder card test loop 5.	..[1]	..[1]
DDI—	Digital data input (ground).	DDOW encoder.	RAU.
DDRG—	Digital data ring.	RAU.	DDOW decoder. DDOW encoder.
DDRV—	Digital data receive.	RAU.	DDOW decoder.
DDRY—	Digital data ready.	RAU.	DDOW decoder. DDOW encoder.
DDSD—	Digital data send.	RAU.	DDOW decoder. DDOW encoder.
DECT01	DDOW encoder card test loop 1.	..[1]	..[1]
DECT02	DDOW encoder card test loop 2.	..[1]	..[1]
DECT03	DDOW encoder card test loop 3.	..[1]	..[1]
DECT04	DDOW encoder card test loop 4.	..[1]	..[1]
DECT05	DDOW encoder card test loop 5.	..[1]	..[1]
DGPCT0X	DGP card test loop 1.	..[1]	..[1]
DGPCT0Y	DGP card test loop 2.	..[1]	..[1]
DMLPS	Dummy lamp.	AD.	Front panel. RAU.
DRCT01	SG D/R card test loop 1.	..[1]	..[1]
DRCT02	SG D/R card test loop 2.	..[1]	..[1]
DS	Dummy sync.	GTM.	AD.
DVCAL—	Digital voice call.	DVOW.	AD.
DVCALS	Digital voice call signal.	AD.	Front panel.
DVCT01	DVOW card test loop 1.	..[1]	..[1]
DVCT02	DVOW card test loop 2.	..[1]	..[1]
DVEAR	Digital voice earphone.	DVOW.	AVOW.
DVEXI	Digital voice extension input.	RAU.	DVOW.
DVEXI—	Digital voice extension input (return).	RAU.	DVOW.
DVEXO	Digital voice extension output.	DVOW.	RAU.
DVEXO—	Digital voice extension output (return).	DVOW.	RAU.
DVMIC	Digital voice microphone.	AVOW.	DVOW.
DVOWI	Digital voice orderwire input.	DVOW.	MO/C.
DVRNG—	Digital voice ring.	..[1]	AVOW.
DVRNGS	Digital voice ring signal.	AVOW.	DVOW.
D12EN	Digital data 1200-baud enable.	DDOW encoder.	DDOW decoder.
D75EN	Digital data 75-baud enable.	DDOW encoder.	DDOW decoder.
D12I	Digital data 1200-baud input.	RAU.	DDOW encoder.
D75I	Digital data 75-baud input.	RAU.	DDOW encoder.

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
D12O	Digital data 1200-baud output.	DDOW decoder.	RAU.
D12O—	Digital data 1200-baud output (return).	DDOW decoder.	RAU.
D75O	Digital data 75-baud output.	DDOW decoder.	RAU.
D75O—	Digital data 75-baud output (return).	DDOW decoder.	RAU.
EQLPS	Equipment lamp.	AD.	Front panel. RAU.
EXAT	External alarm test.	RAU.	AD.
FMGD	Frame ground.	Card file.	Front panel.
FSCT01	FS card test loop 1.	. .[1]	. .[1]
FSCT02	FS card test loop 2.	. .[1]	. .[1]
FSCT03	FS card test loop 3.	. .[1]	. .[1]
FTLB1	Fault light bit 1.	AVOW.	Front panel.
FTLB2	Fault light bit 2.	AVOW.	Front panel.
FTLB4	Fault light bit 4.	AVOW.	Front panel.
FTLB8	Fault light bit 8.	AVOW.	Front panel.
FTLB16	Fault light bit 16.	AVOW.	Front panel.
GF1	Group frame scan address bit 1.	GTM.	AD.
GF2	Group frame scan address bit 2.	GTM.	AD.
GF4	Group frame scan address bit 4.	GTM.	AD.
GF8	Group frame scan address bit 8.	GTM.	AD.
GF8—	Group frame scan address bit 8.	GTM.	AD.
GFMST	Group frame monitor strobe.	GTM.	AD.
GFMTC—	Group frame monitor terminal count.	GTM.	AD.
GRP (CH A)	(Refer to GRP 1 through GRP 4.)		
GRP (CH B)	(Refer to GRP 5 through GRP 8.)		
GRP 1	Group 1 (CH A).	DGP No. 1.	MO/C.
GRP 2	Group 2 (CH A).	DGP No. 2.	MO/C.
GRP 3	Group 3 (CH A).	DGP No. 3	MO/C.
GRP 4	Group 4 (CH A).	DGP No. 4.	MO/C.
GRP 5	Group 5 (CH B).	DGP No. 1.	MO/C.
GRP 6	Group 6 (CH B).	DGP No. 2	MO/C.
GRP 7	Group 7 (CH B).	DGP No. 3.	MO/C.
GRP 8	Group 8 (CH B).	DGP No. 4.	MO/C.
GS	Good status.	GTM.	AD.
GTMCT01	GTM card test loop 1.	. .[1]	. .[1]
GTMCT02	GTM card test loop 2.	. .[1]	. .[1]
GTMCT03	GTM card test loop 3.	. .[1]	. .[1]
GTMCT04	GTM card test loop 4.	. .[1]	. .[1]
GTMCT05	GTM card test loop 5.	. .[1]	. .[1]
GTMCT06	GTM card test loop 6.	. .[1]	. .[1]
ICH1LPS	Input channel 1 lamp.	AD.	Front panel. RAU.
ICH2LPS	Input channel 2 lamp.	AD.	Front panel. RAU.
ICH3LPS	Input channel 3 lamp.	AD.	Front panel. RAU.
ICH4LPS	Input channel 4 lamp.	AD.	Front panel. RAU.
ICH5LPS	Input channel 5 lamp.	AD.	Front panel. RAU.
ICH6LPS	Input channel 6 lamp.	AD.	Front panel. RAU.
ICH7LPS	Input channel 7 lamp.	AD.	Front panel. RAU.
ICH8LPS	Input channel 8 lamp.	AD.	Front panel. RAU.
IDLE	Group idle.	GTM.	AD.
IDLE—	Group idle.	GTM.	AD.
IGRP (CH A) D	(Refer to IGRP1D through IGRP4D.)		
IGRP (CH B) D	(Refer to IGRP5D through IGRP8D.)		
IGRP1D	Input group 1 data (CH A).	GTM.	DGP No. 1.

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
IGRP2D	Input group 2 data (CH A).	GTM.	DGP No. 2.
IGRP3D	Input group 3 data (CH A).	GTM.	DGP No. 3.
IGRP4D	Input group 4 data (CH A).	GTM.	DGP No. 4.
IGRP5D	Input group 5 data (CH B).	GTM.	DGP No. 1.
IGRP6D	Input group 6 data (CH B).	GTM.	DGP No. 2.
IGRP7D	Input group 7 data (CH B).	GTM.	DGP No. 3.
IGRP8D	Input group 8 data (CH B).	GTM.	DGP No. 4.
IGS (CH A)—	(Refer to IGS1— through IGS4—.)		
IGS (CH B)—	(Refer to IGS5— through IGS8—.)		
IGS1—	Input good status group 1 (CH A).	AD.	DGP No. 1.
IGS2—	Input good status group 2 (CH A).	AD.	DGP No. 2.
IGS3—	Input good status group 3 (CH A).	AD.	DGP No. 3.
IGS4—	Input good status group 4 (CH A).	AD.	DGP No. 4.
IGS5—	Input good status group 5 (CH B).	AD.	DGP No. 1.
IGS6—	Input good status group 6 (CH B).	AD.	DGP No. 2.
IGS7—	Input good status group 7 (CH B).	AD.	DGP No. 3.
IGS8—	Input good status group 8 (CH B).	AD.	DGP No. 4.
INAT	Internal alarm test.	Front panel.	AD.
LATL—	Local analog talk/listen.	Front panel.	AVOW.
LDTL—	Local digital talk/listen.	Front panel.	AVOW. DVOW.
LEAR	Local earphone.	AVOW.	Front panel.
LMIC	Local microphone.	Front panel.	AVOW.
LOOP—	Loopback	Front panel.	SG D/R.
MOCT01	MO/C card test loop 1.	. .[1]	. .[1]
MOCT02	MO/C card test loop 2.	. .[1]	. .[1]
MOCT03	MO/C card test loop 3.	. .[1]	. .[1]
NRZOUT	Nonreturn to zero output.	MO/C.	SG D/R.
OCH1LPS	Output channel 1 lamp.	AD.	Front panel. RAU.
OCH2LPS	Output channel 2 lamp.	AD.	Front panel. RAU.
OCH3LPS	Output channel 3 lamp.	AD.	Front panel. RAU.
OCH4LPS	Output channel 4 lamp.	AD.	Front panel. RAU.
OCH5LPS	Output channel 5 lamp.	AD.	Front panel. RAU.
OCH6LPS	Output channel 6 lamp.	AD.	Front panel. RAU.
OCH7LPS	Output channel 7 lamp.	AD.	Front panel. RAU.
OCH8LPS	Output channel 8 lamp.	AD.	Front panel. RAU.
OGRP (CH A) D	(Refer to OGRP1D through OGRP4D.)		
OGRP (CH B) D	(Refer to OGRP5D through OGRP8D.)		
OGRP1D	Output group 1 data (CH A).	DGP No. 1.	GTM.
OGRP2D	Output group 2 data (CH A).	DGP No. 2.	GTM.
OGRP3D	Output group 3 data (CH A).	DGP No. 3.	GTM.
OGRP4D	Output group 4 data (CH A).	DGP No. 4.	GTM.
OGRP5D	Output group 5 data (CH B).	DGP No. 1.	GTM.
OGRP6D	Output group 6 data (CH B).	DGP No. 2.	GTM.
OGRP7D	Output group 7 data (CH B).	DGP No. 3.	GTM.
OGRP8D	Output group 8 data (CH B).	DGP No. 4.	GTM.
OGRP (CH A) T	(Refer to OGRP1T through OGRP4T.)		
OGRP (CH B) T	(Refer to OGRP5T through OGRP8T.)		
OGRP1T	Output group 1 timing (CH A).	DGP No. 1.	GTM.
OGRP2T	Output group 2 timing (CH A).	DGP No. 2.	GTM.
OGRP3T	Output group 3 timing (CH A).	DGP No. 3.	GTM.
OGRP4T	Output group 4 timing (CH A).	DGP No. 4.	GTM.
OGRP5T	Output group 5 timing (CH B).	DGP No. 1.	GTM.

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
OGRP6T	Output group 6 timing (CH B).	DGP No. 2.	GTM.
OGRP7T	Output group 7 timing (CH B).	DGP No. 3.	GTM.
OGRP8T	Output group 8 timing (CH B).	DGP No. 4.	GTM.
OGRP (CH A) TG	(Refer to OGRP1TG through OGRP4TG.)		
OGRP (CH B) TG	(Refer to OGRP5TG through OGRP8TG.)		
OGRP1TG	Output group 1 timing ground (CH A).	DGP No. 1.	Output jack J17.
OGRP2TG	Output group 2 timing ground (CH A).	DGP No. 2.	Output jack J18.
OGRP3TG	Output group 3 timing ground (CH A).	DGP No. 3.	Output jack J19.
OGRP4TG	Output group 4 timing ground (CH A).	DGP No. 4.	Output jack J20.
OGRP5TG	Output group 5 timing ground (CH B).	DGP No. 1.	Output jack J21.
OGRP6TG	Output group 6 timing ground (CH B).	DGP No. 2.	Output jack J22.
OGRP7TG	Output group 7 timing ground (CH B).	DGP No. 3.	Output jack J23.
OGRP8TG	Output group 8 timing ground (CH B).	DGP No. 4.	Output jack J24.
OGRP (CH A) TM	(Refer to OGRP1TM through OGRP4TM.)		
OGRP (CH B) TM	(Refer to OGRP5TM through OGRP8TM.)		
OGRP1TM	Output group 1 timing (CH A).	DGP No. 1.	Output jack J17.
OGRP2TM	Output group 2 timing (CH A).	DGP No. 2.	Output jack J18.
OGRP3TM	Output group 3 timing (CH A).	DGP No. 3.	Output jack J19.
OGRP4TM	Output group 4 timing (CH A).	DGP No. 4.	Output jack J20.
OGRP5TM	Output group 5 timing (CH B).	DGP No. 1.	Output jack J21.
OGRP6TM	Output group 6 timing (CH B).	DGP No. 2.	Output jack J22.
OGRP7TM	Output group 7 timing (CH B).	DGP No. 3.	Output jack J23.
OGRP8TM	Output group 8 timing (CH B).	DGP No. 4.	Output jack J24.
OGRPD (CH A)	(Refer to OGRPD1 through OGRPD4.)		
OGRPD (CH B)	(Refer to OGRPD5 through OGRPD8.)		
OGRPD1	Output group 1 data (CH A).	DGP No. 1.	Output jack J9.
OGRPD2	Output group 2 data (CH A).	DGP No. 2.	Output jack J10.
OGRPD3	Output group 3 data (CH A).	DGP No. 3.	Output jack J11.
OGRPD4	Output group 4 data (CH A).	DGP No. 4.	Output jack J12.
OGRPD5	Output group 5 data (CH B).	DGP No. 1.	Output jack J13.
OGRPD6	Output group 6 data (CH B).	DGP No. 2.	Output jack J14.
OGRPD7	Output group 7 data (CH B).	DGP No. 3.	Output jack J15.
OGRPD8	Output group 8 data (CH B).	DGP No. 4.	Output jack J16.
OGRPG (CH A)	(Refer to OGRPG1 through OGRPG4.)		
OGRPG (CH B)	(Refer to OGRPG5 through OGRPG8.)		
OGRPG1	Output group 1 data ground (CH A).	DGP No. 1.	Output jack J9.
OGRPG2	Output group 2 data ground (CH A).	DGP No. 2.	Output jack J10.
OGRPG3	Output group 3 data ground (CH A).	DGP No. 3.	Output jack J11.
OGRPG4	Output group 4 data ground (CH A).	DGP No. 4.	Output jack J12.
OGRPG5	Output group 5 data ground (CH B).	DGP No. 1.	Output jack J13.
OGRPG6	Output group 6 data ground (CH B).	DGP No. 2.	Output jack J14.
OGRPG7	Output group 7 data ground (CH B).	DGP No. 3.	Output jack J15.
OGRPG8	Output group 8 data ground (CH B).	DGP No. 4.	Output jack J16.
PCMGP1	Pulse code modulation group 1 input.	Input jack J1.	GTM.
PCMGP2	Pulse code modulation group 2 input.	Input jack J2.	GTM.
PCMGP3	Pulse code modulation group 3 input.	Input jack J3.	GTM.
PCMGP4	Pulse code modulation group 4 input.	Input jack J4.	GTM.
PCMGP5	Pulse code modulation group 5 input.	Input jack J5.	GTM.
PCMGP6	Pulse code modulation group 6 input.	Input jack J6.	GTM.
PCMGP7	Pulse code modulation group 7 input.	Input jack J7.	GTM.
PCMGP8	Pulse code modulation group 8 input.	Input jack J8.	GTM.
PCMGP1G	Pulse code modulation group 1 input ground.	Input jack J1.	GTM.
PCMGP2G	Pulse code modulation group 2 input ground.	Input jack J2.	GTM.
PCMGP3G	Pulse code modulation group 3 input ground.	Input jack J3.	GTM.
PCMGP4G	Pulse code modulation group 4 input ground.	Input jack J4.	GTM.
PCMGP5G	Pulse code modulation group 5 input ground.	Input jack J5.	GTM.
PCMGP6G	Pulse code modulation group 6 input ground.	Input jack J6.	GTM.
PCMGP7G	Pulse code modulation group 7 input ground.	Input jack J7.	GTM.
PCMGP8G	Pulse code modulation group 8 input ground.	Input jack J8.	GTM.
PDET	Peak detector.	Front panel.	SG D/R.

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
PRS—	Power on reset.	MO/C.	AD. AVOW. DDOW decoder. DDOW encoder. GTM.
PTT—	Press-to-talk.	RAU.	AVOW.
PWRLT	Cable power lamp test.	AD.	Front panel.
RATL—	Remote analog talk/listen.	RAU.	AVOW.
RAVCALS	Remote analog voice call signal.	AD.	RAU.
RAVCP	Received analog voice cable power.	SG D/R.	21A13T2.
RAVOW1	Received analog voice orderwire.	21A13T2.	AVOW.
RAVOW2	Received analog voice orderwire.	21A13T2.	AVOW.
RBCT01	Receive bit count 1.	TC (D).	. .[1]
RBCT02	Receive bit count 2.	TC (D).	. .[1]
RBCT04	Receive bit count 4.	TC (D).	. .[1]
RCHAN (CH A)	(Refer to RCHAN1 through RCHAN4).		
RCHAN (CH B)	(Refer to RCHAN5 through RCHAN8).		
RCHAN1	Receive channel clock group 1 (CH A).	TC (D).	DGP No. 1.
RCHAN2	Receive channel clock group 2 (CH A).	TC (D).	DGP No. 2.
RCHAN3	Receive channel clock group 3 (CH A).	TC (D).	DGP No. 3.
RCHAN4	Receive channel clock group 4 (CH A).	TC (D).	DGP No. 4.
RCHAN5	Receive channel clock group 5 (CH B).	TC (D).	DGP No. 1.
RCHAN6	Receive channel clock group 6 (CH B).	TC (D).	DGP No. 2.
RCHAN7	Receive channel clock group 7 (CH B).	TC (D).	DGP No. 3.
RCHAN8	Receive channel clock group 8 (CH B).	TC (D).	DGP No. 4.
RCHN (CH A)	(Refer to RCHN1 through RCHN4.)		
RCHN (CH B)	(Refer to RCHN5 through RCHN8.)		
RCHN1	Receive channel clock delete group 1 (CH A).	TC (D).	DGP No. 1.
RCHN2	Receive channel clock delete group 2 (CH A).	TC (D).	DGP No. 2.
RCHN3	Receive channel clock delete group 3 (CH A).	TC (D).	DGP No. 3.
RCHN4	Receive channel clock delete group 4 (CH A).	TC (D).	DGP No. 4.
RCHN5	Receive channel clock delete group 5 (CH B).	TC (D).	DGP No. 1.
RCHN6	Receive channel clock delete group 6 (CH B).	TC (D).	DGP No. 2.
RCHN7	Receive channel clock delete group 7 (CH B).	TC (D).	DGP No. 3.
RCHN8	Receive channel clock delete group 8 (CH B).	TC (D).	DGP No. 4.
RCLK	Receive clock.	TC (D).	DVOW. FS.
RCLK—	Receive clock	TC (D).	DDOW decoder. DGP's. DVOW. FS.
RCOM (CH A)	(Refer to RCOM1 through RCOM4.)		
RCOM (CH B)	(Refer to RCOM5 through RCOM8.)		
RCOM1	Rate compare group 1 (CH A).	DGP No. 1.	MO/C.
RCOM2	Rate compare group 2 (CH A).	DGP No. 2.	MO/C.
RCOM3	Rate compare group 3 (CH A).	DGP No. 3.	MO/C.
RCOM4	Rate compare group 4 (CH A).	DGP No. 4.	MO/C.
RCOM5	Rate compare group 5 (CH B).	DGP No. 1.	MO/C.
RCOM6	Rate compare group 6 (CH B).	DGP No. 2.	MO/C.
RCOM7	Rate compare group 7 (CH B).	DGP No. 3.	MO/C.
RCOM8	Rate compare group 8 (CH B).	DGP No. 4.	MO/C.
RCP	Receive cable power.	Front panel.	21A13T2.
RDAP24—	Receive diagnostic alarm priority.	TC (D).	FS.
RDATA	Receive data.	SG D/R.	FS.
RDEP2	Receive diagnostic enable priority 2.	AD.	TC (D).
RDEP2—	Receive diagnostic enable priority 2.	AD.	TC (D).
RDEP4	Receive diagnostic enable priority 4.	FS.	TC (D).
RDFALT	Receive diagnostic fault.	TC (D).	AD.
RDLTTY	Receive delete.	FS.	DDOW decoder. TC (D).

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
RDTAOW	Receive digital data orderwire.	TC (D).	DDOW decoder.
RDTL—	Remote digital talk/listen.	RAU.	AVOW. DVOW.
RDVCALS	Remote digital voice call signal.	AD.	RAU.
RDVOW	Receive digital voice orderwire clock.	TC (D).	DVOW.
RDVOWC—	Receive digital voice orderwire smooth clock.	TC (D).	DVOW.
REAR	Remote earphone.	AVOW.	RAU.
REF	Reference voltage (2.59v).	Power supply.	AVOW.
RFCET	Receive frame code enable time.	TC (D).	FS.
RFCT01	Receive frame count 1 (binary form).	TC (D).	. .[3]
RFCT02	Receive frame count 2 (binary form).	TC (D).	. .[3]
RFCT04	Receive frame count 4 (binary form).	TC (D).	. .[3]
RFCT08	Receive frame count 8 (binary form).	TC (D).	. .[3]
RFC11—	Receive frame count 11 (12th frame).	TC (D).	. .[3]
RFSYNC—	Receive frame sync.	FS.	TC (D).
RGRPE—	Receive group enable.	TC (D).	. .[3]
RLBMF—	Receive last bit of major frame.	TC (D).	DDOW decoder. FS.
RLFOMF	Receive last frame of major frame.	TC (D).	. .[3]
RMASCLK	Receive master clock.	SG D/R.	DDOW decoder. TC (D).
RMIC	Remote microphone.	RAU.	AVOW.
RMSYNC	Receive major frame sync.	FS.	SG D/R.
RMSYNC—	Receive major frame sync.	FS.	DGP's. TC (D).
RNOCLK	Receive no clock.	TC (D).	AD. SG D/R.
RNOCLK—	Receive no clock.	TC (D).	FS.
RPHF	Receive phase forcing.	SG D/R.	TC (D).
RSCODE	Receive stuff code.	TC (D).	FS.
RSCODE—	Receive stuff code.	TC (D).	FS.
RSREST	Receive stuff request strobe.	TC (D).	. .[3]
RSREST—	Receive stuff request strobe.	TC (D).	FS.
RST (CH A)—	(Refer to RST1— through RST4—.)		
RST (CH B)—	(Refer to RST5— through RST8—.)		
RST1—	Reset strobe group 1 (CH A).	GTM.	DGP No. 1.
RST2—	Reset strobe group 2 (CH A).	GTM.	DGP No. 2.
RST3—	Reset strobe group 3 (CH A).	GTM.	DGP No. 3.
RST4—	Reset strobe group 4 (CH A).	GTM.	DGP No. 4.
RST5—	Reset strobe group 5 (CH B).	GTM.	DGP No. 1.
RST6—	Reset strobe group 6 (CH B).	GTM.	DGP No. 2.
RST7—	Reset strobe group 7 (CH B).	GTM.	DGP No. 3.
RST8—	Reset strobe group 8 (CH B).	GTM.	DGP No. 4.
RTCCT01	TC (D) card test loop 1.	. .[1]	. .[1]
RTCCT02	TC (D) card test loop 2.	. .[1]	. .[1]
RTTYOW	Receive teletype orderwire.	DDOW encoder.	MO/C.
R341BT	Receive bit time 341.	TC (D).	FS.
R341BT—	Receive bit time 341.	TC (D).	FS.
SDATA	Supergroup (SG) data.	FS.	DDOW decoder. DGP's. DVOW.
SGCLPS	Supergroup (SG) cable lamp.	AD.	Front panel. RAU.
SGIN1	Supergroup (SG) input.	Input jack J28.	SG D/R.
SGIN2	Supergroup (SG) input (ground).	Input jack J28.	SG D/R.
SGOUT1	Supergroup (SG) output.	SG D/R.	Output jack J27.
SGOUT2	Supergroup (SG) output (ground).	SG D/R.	Output jack J27.
SGSLPS	Supergroup (SG) sync lamp.	AD.	Front panel. RAU.
SYNC 8	Receive major frame sync level 8.	FS.	AD.
SYNC 8—	Receive major frame sync level 8.	FS.	DDOW decoder. DVOW.

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
TAVCP	Transmit analog voice cable power.	21A13T1.	SG D/R.
TAVOW1	Transmit analog voice orderwire.	AVOW.	21A13T1.
TAVOW2	Transmit analog voice orderwire (ground).	AVOW.	21A13T1.
TBCT01	Transmit bit count 1.	TC (M).	MO/C.
TBCT02	Transmit bit count 2.	TC (M).	MO/C.
TBCT04	Transmit bit count 4.	TC (M).	MO/C.
TCHAN (CH A)	(Refer to TCHAN1 through TCHAN4.)		
TCHAN (CH B)	(Refer to TCHAN5 through TCHAN8.)		
TCHAN1	Transmit channel clock group 1 (CH A).	TC (M).	DGP No. 1.
TCHAN2	Transmit channel clock group 2 (CH A).	TC (M).	DGP No. 2.
TCHAN3	Transmit channel clock group 3 (CH A).	TC (M).	DGP No. 3.
TCHAN4	Transmit channel clock group 4 (CH A).	TC (M).	DGP No. 4.
TCHAN5	Transmit channel clock group 5 (CH B).	TC (M).	DGP No. 1.
TCHAN6	Transmit channel clock group 6 (CH B).	TC (M).	DGP No. 2.
TCHAN7	Transmit channel clock group 7 (CH B).	TC (M).	DGP No. 3.
TCHAN8	Transmit channel clock group 8 (CH B).	TC (M).	DGP No. 4.
TCHN (CH A)	(Refer to TCHN1 through TCHN4.)		
TCHN (CH B)	(Refer to TCHN5 through TCHN8.)		
TCHN1	Transmit channel clock delete group 1 (CH A).	TC (M).	DGP No. 1.
TCHN2	Transmit channel clock delete group 2 (CH A).	TC (M).	DGP No. 2.
TCHN3	Transmit channel clock delete group 3 (CH A).	TC (M).	DGP No. 3.
TCHN4	Transmit channel clock delete group 4 (CH A).	TC (M).	DGP No. 4.
TCHN5	Transmit channel clock delete group 5 (CH B).	TC (M).	DGP No. 1.
TCHN6	Transmit channel clock delete group 6 (CH B).	TC (M).	DGP No. 2.
TCHN7	Transmit channel clock delete group 7 (CH B).	TC (M).	DGP No. 3.
TCHN8	Transmit channel clock delete group 8 (CH B).	TC (M).	DGP No. 4.
TCLK	Transmit clock.	TC (M).	DGP's. DVOW. MO/C.
TCLK—	Transmit clock.	TC (M).	DDOW encoder. MO/C.
TCP	Transmit cable power.	21A13T1.	Front panel.
TDAP24—	Transmit diagnostic alarm priority.	TC (M).	MO/C.
TDEP4	Transmit diagnostic enable priority 4.	MO/C.	TC (M).
TDFALT	Transmit diagnostic fault.	TC (M).	AD.
TDLTTY	Transmit delete.	MO/C.	DDOW encoder. TC (M).
TDTAOW	Transmit digital data orderwire.	TC (M).	DDOW encoder. MO/C.
TDVOW	Transmit digital voice orderwire clock.	TC (M).	DVOW. MO/C.
TDVOWC—	Transmit digital voice orderwire smooth clock.	TC (M).	DVOW.
TFCET	Transmit frame code enable time.	TC (M).	MO/C.
TFCT01	Transmit frame count 1 (binary form).	TC (M).	MO/C.
TFCT02	Transmit frame count 2 (binary form).	TC (M).	MO/C.
TFCT04	Transmit frame count 4 (binary form).	TC (M).	MO/C.
TFCT08	Transmit frame count 8 (binary form).	TC (M).	MO/C.
TFC11—	Transmit frame count 11 (12th frame).	TC (M).	MO/C.
TGRPE—	Transmit group enable.	TC (M).	. .[3]
TLBMF—	Transmit last bit of major frame.	TC (M).	Front panel.
TLFOMF	Transmit last frame of major frame.	TC (M).	SG D/R.
TMASCLK	Transmit master clock.	MO/C.	TC (M).
TNOCLK	Transmit no clock.	TC (M).	. .[3]
TNOCLK—	Transmit no clock.	TC (M).	. .[3]
TSCODE	Transmit stuff code.	TC (M).	MO/C.
TSCODE—	Transmit stuff code.	TC (M).	MO/C.
TSREST	Transmit stuff request strobe.	TC (M).	MO/C.
TSREST—	Transmit stuff request strobe.	TC (M).	. .[3]
TTCCT01	TC (M) card test loop 1.	. .[1]	. .[1]
TTCCT02	TC (M) card test loop 2.	. .[1]	. .[1]

See footnotes at end of table.

Table 1-2. Signal Names and Definitions—Continued

Signal name	Definition	Source	Destination(s)
TTYOWI	Teletype orderwire input.	DDOW encoder.	MO/C.
T341BT	Transmit bit time 341.	TC (M).	..[1]
T341BT–	Transmit bit time 341.	TC (M).	..[1]
XMTERR	Transmit error.	SG D/R.	AD.
48 CHE	48-channel enable.	MO/C.	DGP's. DVOW. TC (D). TC (M).
96 CHE	96-channel enable.	MO/C.	DVOW. TC (D). TC (M).
75CLK	75 Hz clock.	DDOW encoder.	SG D/R.
1.6 KHZ	1.6 kHz output.	MO/C.	AVOW.
6.4 KHZ	6.4 kHz output.	MO/C.	AVOW.
576 KHZ 1	576 kHz output 1.	MO/C.	GTM.
576 KHZ 2	576 kHz output 2.	MO/C.	DGP's.

---

[1] These represent card test loops that have been incorporated to facilitate card level testing. Signal continuity (from output pin to input pin on each respective card) is made through backplane wiring.

[2] Signal originates either at front panel or RAU.

[3] Signal not distributed to another card.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. INTRODUCTION

2-1. General

a. The TD-976/G contains both a multiplexer section and a demultiplexer section. Up to eight separate asynchronous digital bit streams (PCM groups) are applied to the multiplexer section, which multiplexes them together with certain overhead (O/H) data, on a time division basis, into a single 4915.2 kilobits per second (kbps) output supergroup (SG) bit stream. The PCM group inputs have a true data rate of either 288 kbps (6-channel group) or 576 kbps (12-channel group). The O/H data consist of a frame synchronization and stuff pattern, a digital voice orderwire (DVOW) input, and a teletype orderwire input.

b. The frame synchronization and stuff pattern portion of the O/H data in the received SG controls operation of the demultiplexer section. The demultiplexer section decombines the remaining portion of the SG into the original PCM groups (PCM group outputs), a DVOW output, and a teletype orderwire output.

c. The TD-976/G also has monitoring and alarm circuits and a power supply. The monitoring and alarm circuits monitor incoming and outgoing data and provide audible and visual alarm indications when faults occur. The power supply provides all regulated power required by the TD-976/G. Additionally, the power supply provides a constant current source that powers an SG cable system consisting of TD-982/G pulse form restorers interconnected by CX-11230/G cable.

d. Also, one RAU is included with each TD-976/G. The RAU allows for remoting of the TD-976/G front panel alarms and provides for access to all orderwire functions. Teletype information is provided to the TD-976/G only through the RAU.

2-2. Group Level Interfaces

a. General. The TD-976/G PCM group inputs and PCM group outputs are compatible with Multiplexers TD-660/G, TD-204/U, and TD-754/G. The TD-660/G is a multiplexer that encodes either 6 or 12 voice telephone channels into a single PCM output (288 or 576 kbps with a tolerance of ±0.0045 percent). Conversely, in the return direction, the TD-660/G decombines (demultiplexes) a 288 or 576 kbps PCM group signal into either 6 or 12 channels of voice. The TD-204/U and TD-754/G are synchronous multiplexers that combine or decombine two TD-660/G type PCM groups. When used in conjunction with a TD-976/G, the TD-204/U's or TD-754/G's operate with a single TD-660/G and serve as cable drivers and receivers rather than as multiplexers. This cable system (between TD-754/G's or TD-204/U's) can be up to 40 miles in length and uses TD-206/G pluse form restorers.

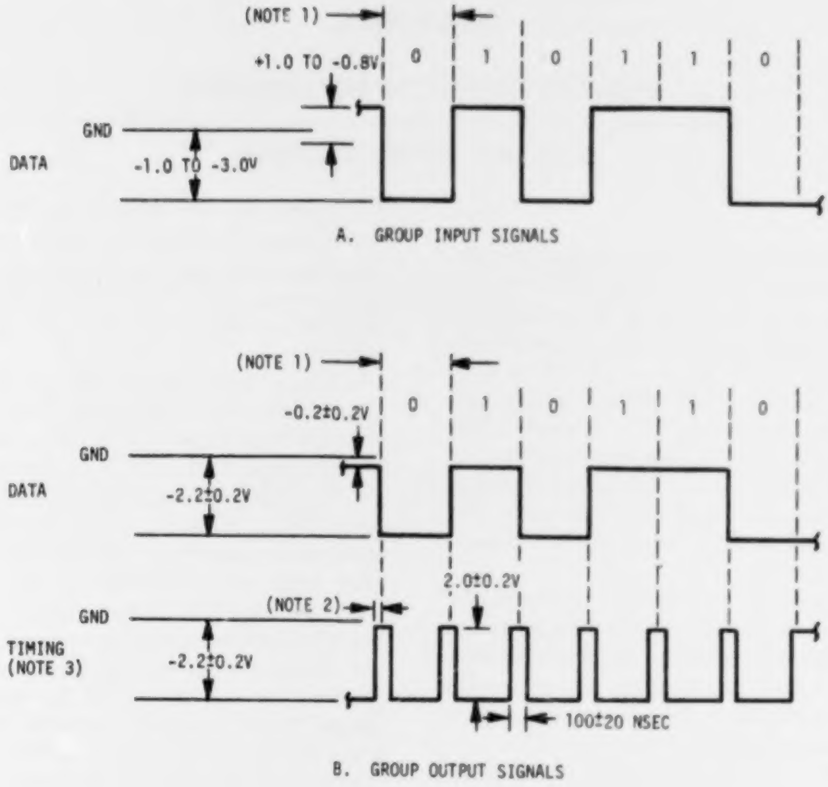
b. Group Input Signals. The TD-976/G PCM group data inputs are in a nonreturn to zero (NRZ) format as shown in A of figure 2-1 (timing is not supplied as an input to the TD-976/G). These inputs may be at either a 6- or 12-channel rate (288 or 576 kbps ± 0.0045 percent). Signal levels for a logic 0 and a logic 1 are as shown in A of figure 2-1. Within the TD-976/G, all digital data are converted at an NRZ transistor-transistor logic (TTL) format (logic 0 is 0 volt and logic 1 is +5 volts) for internal processing.

c. Group Output Signals. Both data and timing are provided by the TD-976/G for each of the output groups. The date outputs are in the NRZ format at the levesl shown in B of figure 2-1. The rate of each group output is the same as was the input rate to the far-end multiplexer. Timing is always provided at a 12-channel rate (nominal 576 kHz). As shown in B of figure 2-1, the positive-going edge of each timing pulse leads the data transition by 10 to 70 nanoseconds. The width of each timing pulse is a nominal 100 nanoseconds and the levels are as shown in B of figure 2-1.

2-3. SG Interface

a. General. SG input/output characteristics of the TD-976/G permit operation over a 0- to 5-mile cable system, using CX-11230/G cable, to another TD-976/G, a TD-1147/TSC multiplexer-demultiplexer, or a AN/GRC-144 radio. If the cable system is longer than 1/2 mile, TD-982/G pulse form restorers are used at 1/2-mile intervals. The signals appearing at the SG input/output connectors of the TD-976/G are a composite consisting of 1/2-baud bipolar SG data, analog voice orderwire (AVOW) data, and a constant dc current that powers the pulse form restorers in the cable system.

b. SG Input/Output. The TD-976/G operates at one of two data rates (HI and LO) as controlled by the DATA RATE switch on MO/C card 21A4. In either case, the SG input/output data stream is at the 4915.2 kbps cable rate and in the 1/2-baud bipolar format



NOTES:

1. DATA PULSEWIDTH IS EITHER A NOMINAL 1.74 USEC (576 KBPS) OR 3.47 USEC (288 KBPS).
2. POSITIVE-GOING EDGES OF TIMING SIGNAL LEAD DATA TRANSITIONS BY 10 TO 70 NSEC.
3. TIMING IS ALWAYS OUTPUTTED AT A NOMINAL 576 KHZ REPETITION RATE. DATA SHOWN IN B ABOVE IS AT 576 KBPS.

EL5NG001

Figure 2-1. Group level signals.

shown in figure 2-2. When there are more than four PCM group inputs to the TD-976/G, the HI data rate is used and the SG rate provides for transmission of 96 channels of data and O/H. In this case, the sum of channel data and O/H rates equals the cable rate of 4915.2 kbps. With four or less PCM group inputs, the LO data rate is used and the SG rate provides for transmission of 48 channels of data and O/H. In this case, the sum of channel data and O/H rates equals a data rate of 2457.6 kbps (1/2 of 4915.2 kbps). Therefore, each bit is transmitted twice in order to maintain the required 4915.2 kbps cable rate. As shown in figure 2-2, logic 1's are alternate positive and negative 1/2-baud pulses whose amplitudes are nominally +0.9 v and −0.9 v with respect to ac zero.

2-4 Orderwire Interfaces

a. General. The TD-976/G processes three types of full-duplex orderwires. Each orderwire has a specific application as listed in (1), (2), and (3) below. The orderwire interfaces associated with the three types of orderwires processed in the TD-976/G are described in *b*, *c*, and *d* below.

(1) *Digital voice orderwire (DVOW).* As described in *b* below, the DVOW circuits provide the capability for verbal communications between the orderwire interfaces at the near-end TD-976/G and the far-end TD-976/G in a given system configuration. This orderwire is commonly known as the system orderwire.

(2) *Digital data orderwire (DDOW).* As described in *c* below, the DDOW circuits provide the capability

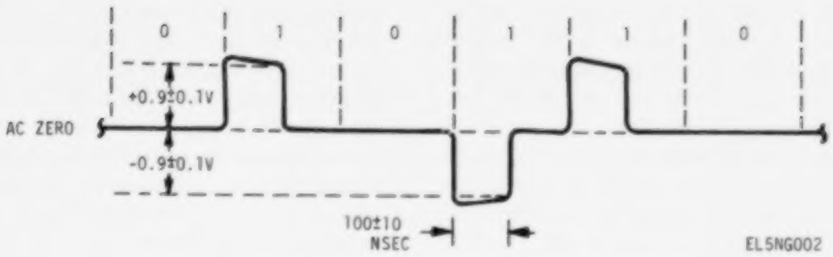


Figure 2-2. ½-baud bipolar format (96 channels of data).

for written communications between teletype instruments at the near-end TD-976/G and the far-end TD-976/G in a given system configuration.

(3) *Analog voice orderwire (AVOW).* As described in *d* below, the AVOW circuits provide the capability for verbal communications between the orderwire interfaces at the near-end TD-976/G and the orderwire interfaces at the down-link cable instrument. As described below, the DDOW and DVOW circuits use the digital circuits in the demultiplex and multiplex functions in the TD-976/G. The AVOW circuits are completely analog and can be used when the digital circuits in the TD-976/G are down. When a cable link contains one or more TD-982/G's, the AVOW provides the orderwire service between the end instruments on the cable link and an AN/PTM-7 telephone test set attached to a TD-982/G. This orderwire is commonly known as the cable orderwire.

b. DVOW.

(1) The DVOW circuits process voice orderwire signals from one or more of the following sources: A handset connected to a connector on the TD-976/G front panel or on the RAU; an external 4-wire source applied to jacks on the front of the RAU; and an external console orderwire panel that is electrically connected through a multiwire cable that is connected to a connector on the RAU.

(2) In the multiplex function, the analog voice signals are digitally encoded and included as part of the O/H data in the SG output. In the demultiplex function, the orderwire signals in the O/H data are decombined from the SG input, converted from digital data into analog voice signals, and applied to the orderwire instruments connected to the DVOW interfaces.

c. DDOW. The DDOW circuits process digital data (TTY) orderwire from a TTY that is connected to jacks on the front of the RAU. There is no DDOW interface on the TD-976/G front panel. This orderwire may be at either a 75-baud or 1200-baud rate. In the multiplex function, the digital data from the TTY are processed from asynchronous digital data into synchronous digital data that are encoded as O/H in the SG output. In the demultiplex function, the orderwire signals in the O/H data are decombined from the SG input, processed back into the original asynchronous digital data format, and applied to the TTY associated with the far-end TD-976/G.

d. AVOW. The AVOW circuits process voice orderwire signals from one or more of the following sources: A handset connected to a connector on the TD-976/G front panel or on the RAU or an external console orderwire panel that is electrically connected through a multiwire cable connected to a connector on the RAU. The analog voice orderwire signals are processed by analog circuits in the TD-976/G and applied as audio signal voltages on the SG cable output. At the receiving equipment (another TD-976/G, a TD-1147/TSC, or an AN/GRC-144 radio), the audio signal voltages are decoupled from the SG cable input and are processed to produce signal levels that are compatible with the orderwire instruments interfaced with the unit.

Section II. SG MESSAGE FORMATS

2-5. General

Since operation of the various sections in the TD-976/G is determined by SG message formats, knowledge of the message formats is required to provide a basis for understanding of multiplexing and demultiplexing operations. This section explains the content and organization of the two SG message formats used in the TD-976/G. A 96-channel message format is used when more than four PCM groups are processed (HI data rate). A 48-channel message format is used when four or less groups are processed (LO data rate).

2-6. Message Formats

a. General. A complete frame of the 96-channel message format is shown in figure 2-3, while figure 2-4 shows a complete major frame of the 48-channel message format. In both cases, the format is to be read from left to right and from the top down. Thus, the top left bit occurs first in time and the lower right bit occurs last in time. A major frame is the largest organized grouping within the SG message format. A major frame is subdivided into frames, which, in turn, are subdivided into minor frames.

b. Minor Frames. In both message formats, a minor frame is 17 bits long, consisting of 16 data bits and one O/H bit. There are always 20 minor frames (identified as minor frames 0 through 19) in each frame. The O/H bits carry frame synchronization and stuffing information, DVOW information, and digital data (teletype) information. At the end of minor frame 19, an additional O/H bit (end-of-frame bit) is inserted. Thus, each frame is always 341 bits long ((17x20) + [illegible]

c. Frames. The number of frames within a major frame varies depending on the message format. In the 96-channel message format, there are always 12 frames (identified as frames 0 through 11) in a major frame, making the major frame 4092 bits long (341x12). In the 48-channel message format, there are always six frames (identified as frames 0 through 5) in a major frame, making the major frame 2046 bits long (341x6). Since the SG cable transmission rate (4915.2 kbps) is the same for each of the message formats, each of the bits (both data and O/H) in the 48-channel message format is transmitted twice.

d. Group Data. Data from the group inputs are inserted into the 16 data bits of each minor frame. In the 96-channel message format, each minor frame includes two data bits from each of the eight PCM data groups. In the 48-channel message format, each minor frame includes four data bits from each of the four PCM data groups. The sequence in which data from each group are inserted for each message format is shown in figures 2-3 and 2-4.

e. O/H Data. The O/H data inserted in the 17th bit of each minor frame and at the end of each frame represent either DVOW information, digital data (teletype) information, frame synchronization and stuffing information, end-of-frame information, or spare O/H bits.

(1) *Digital voice.* In the 96-channel message format, digital voice information in contained on the O/H bits of minor frames 0, 5, 10, and 15. In the 48-channel message format, digital voice information is contained in the O/H bits of minor frames 0, 1, 5, 6, 10, 11, 15, and 16.

(2) *Digital data (teletype).* In both message formats, digital data (teletype) information is contained in the O/H of minor frame 2 of frame 0. Only one bit of digital data is processed during each major frame.

(3) *Frame synchronization and stuff patterns.* In both message formats, 11-bit frame synchronization and stuffing information patterns are contained in the O/H bit positions of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19. These patterns are termed the B pattern (bits B0 through B10) and the A pattern (bits A0 through A10). The A pattern appears in the last frame of each major frame. The B pattern appears in all other frames. The last eight bits of each pattern (B3 through B10 and A3 through A10) contain synchronization information that is inserted by the multiplexer section and decoded by the far-end demultiplexer section to establish frame and major frame synchronization. The entire 11-bit pattern (both B and A patterns) is used to indicate whether or not a stuff condition exists. Stuffing is used to compensate for rate variations between the asynchronous input bit rates and the multiplexer section sampling rates. A general discussion relating to stuffing is contained in section III. The patterns shown on figures 2-3 and 2-4 indicate a no-stuff condition, while their complements would indicate a stuff condition. The pattern in frame 0 indicates a stuff/no-stuff condition for PCM group No. 1, the pattern in frame 1 indicates the condition for PCM group No. 2, and so on. The pattern in the last frame of each major frame indicates a stuff/no-stuff condition for the digital data (teletype).

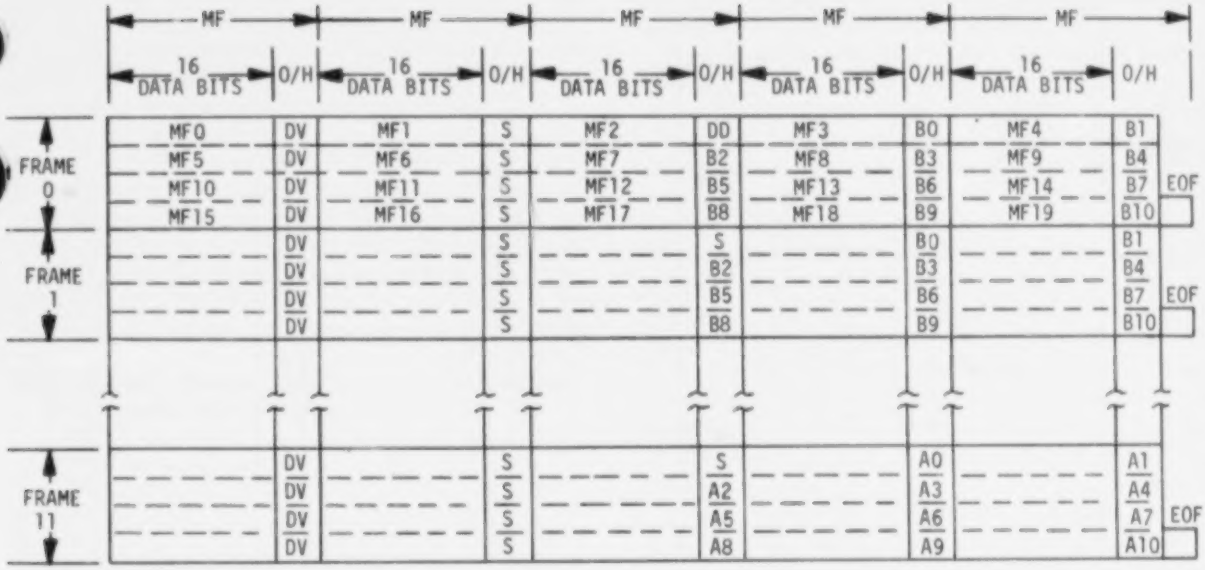
(4) *End-of-frame bits.* In either of 48- or 96-channel message format, an end-of-frame bit is inserted as the last (341st) bit in each transmitted frame. These bit times are used for synchronization purposes within the far-end demultiplexer section.

(5) *Spare O/H bits.* Certain O/H carry no useful information and are termed spares. In the 96-channel message format, the O/H bits in minor frames 1, 6, 11 and 16 of each frame are spares, as is the O/H bit in minor frame 2 of each of frames 1 through 11. In the 48-channel message format, the O/H bit in minor frame 2 of each of frames 1 through 5 is the spare.

2-7. Sampling Rates

a. Internally, the TD-976/G assembles user and O/H data at one of two bit sampling rates: 4915.2 kbps when in HI data rate operation (96-channel operation) and 2457.6 kbps when in LO data rate operation (48-channel operation). For either case, the various elements (group sampling, O/H sampling, etc.) comprising the total assembled rate are listed in figures 2-3 and 2-4. It should be noted that the group and digital data sampling rates are greater than the highest expected user input rates. The difference will be taken care of by stuffing/destuffing (section III).

b. Thus, each of the various elements that make up the assembled data stream can be allocated a portion of the total assembled data rate (various sampling rates). These individual sampling rates can be calculated by dividing the total number of that type of bits in a major frame by the total number of bits in a major frame and then multiplying the result by the appropriate bit sampling rate. For example, the sampling rate


MF
16 DATA BITS
O/H
FRAME 0
FRAME 1
FRAME 11
MF0 MF1 MF2 MF3 MF4
MF5 MF6 MF7 MF8 MF9
MF10 MF11 MF12 MF13 MF14
MF15 MF16 MF17 MF18 MF19
DV
S
DD
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
EOF

NOTES:

1. ABBREVIATIONS

DD = DIGITAL DATA (TELETYPE)
DV = DIGITAL VOICE ORDERWIRE
EOF = END-OF-FRAME BIT
MF = MINOR FRAME
O/H = OVERHEAD
S = SPARE

2. 20 MF IN A FRAME
12 FRAMES IN A MAJOR FRAME

3. 341 BITS IN A FRAME

17 BITS/FRAME
X20 MF/FRAME
340 BITS
+ 1 EOF
341 BITS/FRAME

4. 4092 BITS IN A MAJOR FRAME

341 BITS/FRAME
X 12 FRAMES/MAJOR FRAME
4092 BITS/MAJOR FRAME

5. GROUP DATA SAMPLING SEQUENCE IN A MF (16 BITS)

1 2 3 4 5 6 7 8 1 2 3 4 5 6 7 8

6. FRAME SYNCHRONIZATION AND STUFF PATTERNS (NO-STUFF CONDITION)

	0	1	2	3	4	5	6	7	8	9	10
B PATTERN	0	1	0	0	0	0	0	0	1	1	0
A PATTERN	1	1	1	1	0	1	0	1	1	0	0

7. BIT SAMPLING RATE = 4915.2 KBPS
SG CABLE TRANSMISSION RATE = 4915.2 KBPS

8. APPROXIMATE SAMPLING RATES (KBPS)

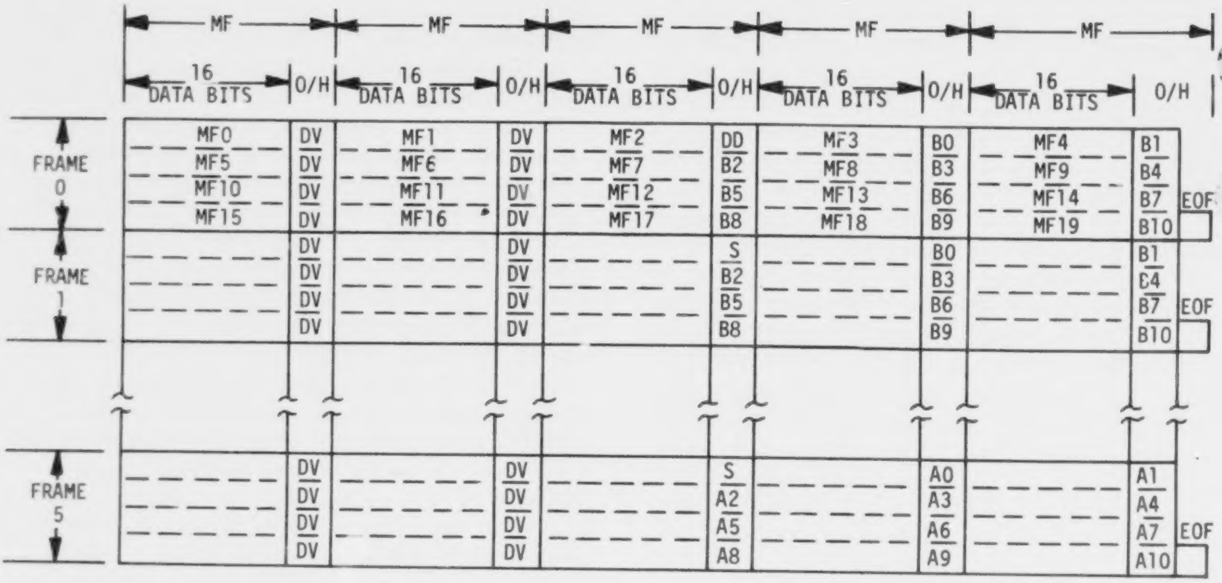
GROUP DATA (4 GROUPS) = 4612.5044
DVOW = 57.6563
DD (TELETYPE) = 1.2012
EOF BIT = 14.4141
SPARES = 70.8692
FRAME SYNCHRONIZATION AND STUFF PATTERNS = 158.5548
4915.2000 KBPS

9. APPROXIMATE INDIVIDUAL GROUP SAMPLING RATE:
576.563 KBPS (4612.5044 KBPS ÷ 8)

EL5NG003

Figure 2-3. 96-channel message format.

for group data in the 96-channel message format is determined as follows. The 3840 group data bits in a major frame (16x20x12) are divided by 4092 (total number of bits in a major frame) and the result is multiplied by the bit sampling rate of 4915.2 kbps, which gives a sampling rate of approximately 4612.5044 kbps for the eight PCM groups. Dividing 4612.5044 kbps by 8 yields a sampling rate of appoximately 576.563 kbps for each of the PCM groups. Sampling rates for the other elements of the SG can be calculated in a like manner.


MF
16 DATA BITS
O/H
FRAME 0
FRAME 1
FRAME 5
MF0
MF5
MF10
MF15
MF1
MF6
MF11
MF16
MF2
MF7
MF12
MF17
MF3
MF8
MF13
MF18
MF4
MF9
MF14
MF19
DV
DD
B2
B5
B8
S
A2
A5
A8
B0
B3
B6
B9
A0
A3
A6
A9
B1
B4
B7
B10
A1
A4
A7
A10
EOF

NOTES:

1. ABBREVIATIONS

DD = DIGITAL DATA (TELETYPE)
DV = DIGITAL VOICE ORDERWIRE
EOF = END-OF-FRAME BIT
MF = MINOR FRAME
O/H = OVERHEAD
S = SPARE

2. 20 MF IN A FRAME
6 FRAMES IN A MAJOR FRAME

3. 341 BITS IN A FRAME

17 BITS/MF
X20 MF/FRAME
340 BITS
+ 1 EOF
341 BITS/FRAME

4. 2046 BITS IN A MAJOR FRAME

341 BITS/FRAME
X 6 FRAMES/MAJOR FRAME
2046 BITS/MAJOR FRAME

5. GROUP DATA SAMPLING SEQUENCE
IN A MF (16 BITS)

1 2 3 4 1 2 3 4 1 2 3 4 1 2 3 4

6. FRAME SYNCHRONIZATION AND STUFF PATTERNS
(NO-STUFF CONDITION)

	0	1	2	3	4	5	6	7	8	9	10
B PATTERN	0	1	0	0	0	0	0	0	1	1	0
A PATTERN	1	1	1	1	0	1	0	1	1	0	0

7. BIT SAMPLING RATE = 2457.6 KBPS
SG CABLE TRANSMISSION RATE = 4915.2 KBPS

8. APPROXIMATE SAMPLING RATES (KBPS)

GROUP DATA (8 GROUPS) = 2306.2522
DVOW = 57.6563
DD (TELETYPE) = 1.2012
EOF BIT = 7.2071
SPARES = 6.0058
FRAME SYNCHRONIZATION AND STUFF PATTERNS = 79.2774
2457.6000 KBPS

9. APPROXIMATE INDIVIDUAL GROUP SAMPLING RATE:
576.563 KBPS (2306.2522 KBPS ÷ 4)

EL5NG004

Figure 2-4. 48-channel message format.

Section III. BASIC EQUIPMENT CONCEPTS

2-8. General

a. The input interfaces established by the TD-976/G with user equipments are asynchronous (user equipments are not phase or frequency locked with internal TD-976/G timing functions). For example, in 96-channel operation, inputs from up to eight users are simultaneously applied to the TD-976/G. Because these user equipments operate under control of independently generated timing signals, their output rates vary (within prescribed tolerances) about established nominal values. In combining or multiplexing these asychronous inputs into a single output SG, the TD-976/G operates under control of internally generated timing signals. The rates of the applied inputs are adjusted with the TD-976/G so that the input data are synchronously inserted into the SG.

b. The asynchronous-to-synchronous conversion performed by the TD-976/G multiplexer section is accomplished by a process termed stuffing. At a receiving TD-976/G demultiplexer, an inverse operation termed destuffing is performed to enable separation of the synchronously combined groups within the received SG into their original single-group asychronous form. The remainder of this section describes the methods by which stuffing and destuffing operations are performed and discusses the range of user rate variation that the TD-976/G can accommodate.

2-9. Input Rate Buffering (Asynchronous-to-Synchronous)

a. Figure 2-5 is a simplified block diagram that shows an input rate buffer, located on a DGP card, for one of the PCM group inputs. The input group data are at a true data rate of either a nominal 288 kbps (6 channels of data) or a nominal 576 kbps (12 channels of data) and are asynchronous with the TD-976/G. The write clock is an extracted clock at a nominal 576 kHz rate synchronized with the incoming input group data. The write clock sequentially advances the write address counter, causing data bits present on the input group data line to be written into seccuessive cell locations of the elastic storage register. This operation is asychronous with internal TD-976/G timing signals. The remainder of this paragraph discusses operation of an input rate buffer on a DGP card. An input rate buffering operation performed on the DDOW encoder card uses a similar operational concept.

b. The elastic storage register is designed so that data may be simultaneously entered (written in) and extracted (read out) under control of independently generated timing signals. However, simultaneous entry and extraction of data in the same register cell location is not permissible. The read function of the elastic storage register is controlled by an address from the read address counter. In turn, the read address counter is advanced by coincidence of a transmit clock (bit sampling rate) and a transmit channel clock (given group's turn to insert a data bit into the SG), both of which are synchronous with TD-976/G internal timing. Each time the read address counter is advanced, the data bit in the next successive cell location of the elastic storage register appears on the group data output line.

c. The number of coincidences of transmit clocks and transmit channel clocks (groups sampling rate of 576.563 kbps) occurs at a rate slightly higher than the nominal 576 kHz write clock rate. Therefore, if the read address counter were allowed to advance at each coincidence of a transmit clock and a transmit channel clock, it would advance upon the write address counter and attempt to read a data bit from a register cell at the same time that the data bit was being written into the cell. This operation is ot permissible because it would introduce bit errors in the group data handling process.

d. To prevent the read address counter from under-

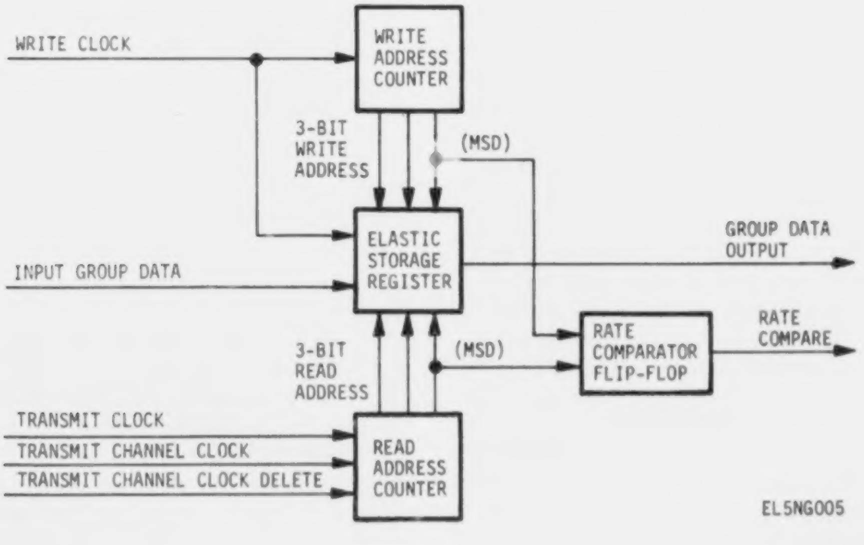


Figure 2-5. Input rate buffer, simplified block diagram.

flowing the storage register, and to maintain a predetermined offset between write and read counter addresses, a stuffing operation is performed by the TD-976/G. Both the read and write address counters provide a 3-bit binary address to the elastic storage register. Thus, each counter recycles after eight counts. The most significant digit of the binary output of the read address counter clocks the rate comparator flip-flop. The rate comparator flip-flop clocks on a positive-going transition, and is therefore clocked once every eight counts of the read address counter (at a count of 4 when the most significant digit (MSD) goes high). When the flip-flop is clocked, it stores the condition of the most significant digit of the binary output of the write address counter. When the offset between the two counters is less than four counts is less than four counts, the rate comparator flip-flop is set and the resulting rate compare signal will cause a stuff action to be accomplished.

e. The common electronics section of the TD-976/G sequentially examines each input rate buffer's rate compare line once each major frame. If a rate compare occurs, the common electronics section acts to generate a transmit channel clock delete signal. This action inhibits the read address counter for one coincidence of a transmit clock and a transmit channel clock, and therefore instantaneously slows the counter by one count. Slowing of the counter, or stuffing, serves to reestablish the desired offset between the write and read address counters and prevents the read address counter from underflowing the elastic storage register. Furthermore, because data are read from the input rate buffer under control of timing signals generated by the TD-976/G, the output data are now synchronized with overall TD-976/G data processing operations.

f. In summar, data and timing inputs asynchronous with the TD-976/G are applied to an input rate buffer. Data are read out of the buffer under control of timing signals generated within the TD-976/G. The read timing signals are therefore synchronous with other TD-976/G operations. The rate of read operations is equalized with the rate of input write operations by a process termed stuffing. Since the read rate is nominally faster than the input write rate, stuffing is accomplished by a periodic process that causes an instantaneous 1-bit slowing of the read operation.

2-10. Stuffing Rate Capabilities

a. General. As described in paragraph 2-9, stuffing is performed to accommodate positive and negative variations about nominal of group input rates not synchronized with the TD-976/G. The frequency with which stuffing operations can be performed, and therefore the amount of group input rate variation the TD-976/G can accommodate, is explained in *b* and *c* below.

b. PCM Group Input Stuffing Ranges. As defined on figures 2-3 and 2-4, the nominal sampling rate for an individual PCM group input is 576.563 kbps. This is 563 bps faster than the expected nominal 576 kbps group input rate. Within the TD-976/G, each PCM group input can be stuffed once per major frame. A major frame is either 4092 or 2046 bits long, depending on whether the TD-976/G is operating at the HI or LO data rate. Therefore, the maximum stuffing rate for one group is approximately 1201 times per second: (1/4092)(4915.2 kbps) or (1/2046)(2457.6 kbps). Since the group sampling rate is 563 bps faster than the nominal group rate, the TD-976/G can accommodate a positive group input rate variation of 563 bps (no stuffing actions performed) and a negative group input rate variation of 638 bps (1201 −563) (maximum stuffing actions performed). Thus, if any minor variations in the internal TD-976/G timing source are ignored, a nominal 576 kbps user group input can vary between 575.362 and 576.563 kbps without introduction of data errors within the TD-976/G.

c. Teletype (DDOW) Input Stuffing. As defined on figures 2-3 and 2-4, the nominal sampling rate for the teletype input is 1201 bps (based on message format, which includes 1 bit of teletype data per major frame). The teletype input is at either a 75-baud or 1200-baud maximum rate (if 75-band input is being used, each bit is sent 16 times (75x16 = 1200)). Therefore, the nominal teletype sampling rate is 1 bps faster than the fastest expected teletype input, and stuffing is used to equalize these rate differences.

2-11. Destuffing and Smoothing

a. Each time the TD-976/G multiplexer section examines the rate compare signal from an input rate buffer and determines whether or not a stuffing action is required, O/H data reflecting this determination are inserted into the output SG at appropriate bit times during the frame in which the determination is made. These O/H data form either a stuff or no-stuff pattern that is recognized in the far-end TD-976/G demultiplex section. When performed, the actual stuffing operation in the multiplexer occurs during the selected input rate buffer's first data sample (read) time of the first minor frame following the frame in which the stuffing pattern is inserted.

b. The far-end demultiplexer is synchronized with the transmitting multiplexer so that when a stuff code for a given input group is received, the demultiplexer can perform the appropriate destuffing and smoothing operations. The destuffing and smoothing operations enable the demultiplexer to output each user group with the same rate variations that existed when that user group was applied to the transmitting multiplexer's input. Smoothing is performed to eliminate

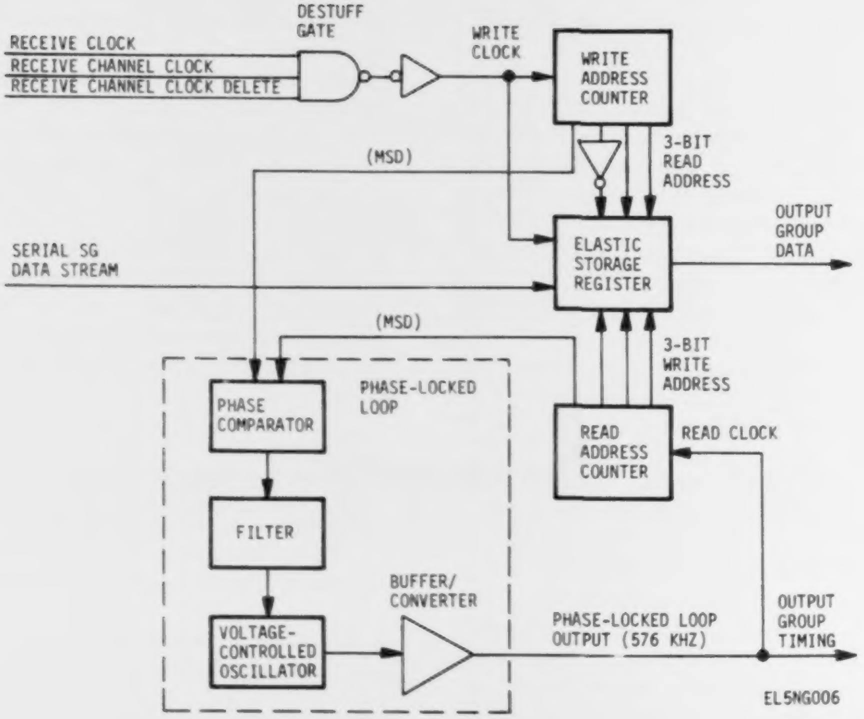

DESTUFF GATE
RECEIVE CLOCK
RECEIVE CHANNEL CLOCK
RECEIVE CHANNEL CLOCK DELETE
WRITE CLOCK
WRITE ADDRESS COUNTER
3-BIT READ ADDRESS
(MSD)
SERIAL SG DATA STREAM
ELASTIC STORAGE REGISTER
OUTPUT GROUP DATA
(MSD)
3-BIT WRITE ADDRESS
PHASE COMPARATOR
PHASE-LOCKED LOOP
READ ADDRESS COUNTER
READ CLOCK
FILTER
BUFFER/ CONVERTER
VOLTAGE-CONTROLLED OSCILLATOR
PHASE-LOCKED LOOP OUTPUT (576 KHZ)
OUTPUT GROUP TIMING
EL5NG006

Figure 2-6. Output rate buffer, simplified block diagram.

the instantaneous 1-bit adjustment in the output timing rate caused by the destuffing operation. Destuffing and smoothing operations within the demultiplexer are performed by an output rate buffer as shown in the simplified block diagram of figure 2-6. In effect, the output rate buffer performs a synchronous-to-asynchronous rate buffering operation that is the complement of that performed by the multiplexer's input rate buffer.

c. Figure 2-6 is a simplified block diagram that shows an output rate buffer, located on a DGP card, for one of the PCM group outputs. The smoothing buffer on the DDOW decoder card is similar except that it does not contain a phase-locked loop because the read clock is a stable derivative of a clock extracted from the incoming SG.

d. In normal operation, each coincidence of a receive clock (extracted clock at bit sampling rate) and a receive channel clock (given group's turn to extract a data bit from the SG) creates a write clock. The write clock sequentially advances the buffer's write address counter, causing a group's data bits from the serial SG data stream to be stored in successive cell locations of the elastic storage register. This write operation is performed sychronously with other demultiplexer functions. Data within the elastic storage register are extracted under control of the read address counter clocked by the output of a voltage-controlled oscillator (VCO) in the phase-locked loop. The 3-bit read address nominally lags the write address by four counts because the 3rd binary bit of the write address is inverted.

e. The independently operating VCO is phase locked to the demultiplexer write clock by a phase comparator and filter. Inputs to the phase comparator are the most significant digits of the write and read address counters. When the two counters are in phase with each other, the 3-bit read address lags the write address by the desired offset of four counts.

f. When a stuffing action is performed in the far-end multiplexer, a corresponding destuffing action must be accomplished in the demultiplexer. The common electronics section of the demultiplexer recognizes the stuff pattern (contained in the O/H data) in the incoming SG and causes a receive channel clock delete signal to be generated at the proper time. This, in turn, inhibits the destuff gate for one coincidence of a receive clock and a receive channel clock. Thus, one write clock is deleted and the write address counter is slowed by one bit time. The instantaneous 1-bit slowing of the write address counter disrupts the phase-locked state existing between the VCO and the write clocks.

g. It is necessary that a phase-locked state be re-established between the write clock and the VCO. In turn, the frequency of the VCO must be slowed consistent with the instantaneous 1-bit slowing of the write clock caused by the destuffing operation. The VCO output, however, serves both as the read clock and the output group timing signal from which output timing to the user is derived. Design characteristics of user equipments are such that rapid excursions in the rate of applied timing signals are unacceptable. For this reason, a gradual reduction in VCO frequency consistent with the instantaneous slowing of the write clock must be performed. Once the gradual frequency reduction (termed smoothing) is accomplished, a phase-locked condition is reestablished between the VCO and the write clock.

h. When a destuffing operation is performed, the phase comparator detects the fact that the positive-going edges of the most significant digits of the write and read address counters are not in phase and the counters are no longer phase locked. The output of the phase comparator is a digital pulse train whose polarity and duty cycle are representative of the magnitude and direction of the detected phase differential. The filter converts and integrates this digital error signal into a corresponding dc correction voltage. Application of the correction voltage to the VCO causes a change in VCO output frequency and a corresponding reduction in duty cycle of the error signal generated by the phase comparator. This closed-loop process continues until the phase comparator ceases to produce an error signal output, indicating that the write clock and the VCO are once again phase locked.

Section IV. OVERALL BLOCK DIAGRAM DISCUSSION

2-12. General

a. Introduction. This section contains the overall block diagram discussion pertaining to the TD-976/G. The discussion is organized as defined in *b* through *f* below. Figure FO-1 is an overall block diagram of the TD-976/G and supports all discussions in this section.

b. Multiplexer Section. The multiplexer section accepts, sequences, and combines various data inputs into a required serial digital data format (output SG). Paragraph 2-13 contains a block diagram discussion of the multiplexer section.

c. Demultiplexer Section. The demultiplexer section receives the serial data SG input and demultiplexes it to its various component parts, and supplies the data to the required destinations. Paragraph 2-14 contains a block diagram discussion of the demultiplexer section.

d. Alarms. Alarm indicators are located on front panel 21A14 (fig. 2-7), on the edges of five of the printed circuit cards, and on RAU 21A15 (fig 2-8). The alarm circuits monitor various signals and functions within the TD-976/G and provide audible and visual indications when the required signals or functions are not detected. Paragraph 2-15 contains a block diagram discussion relating to alarms.

e. Orderwires. Paragraph 2-16 provides a block diagram discussion relating to the following three types of orderwires processed by the TD-976/G.

(1) A digital voice orderwire (DVOW) is digitally encoded and included as part of the O/H data in the SG bit stream. This orderwire is commonly known as the system orderwire.

(2) A digital data orderwire (DDOW) (teletype) is also digitally encoded and included as part of the O/H data in the SG bit stream.

(3) An analog voice orderwire (AVOW) is superimposed on the SG cable signal. This orderwire is commonly known as the cable orderwire.

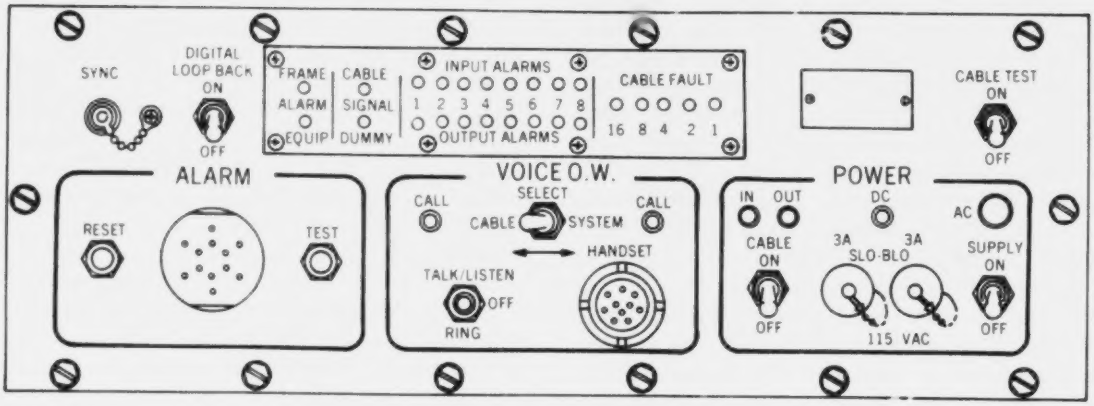
f. Power. Paragraph 2-17 provides a block diagram discussion of power generation and distribution.

2-13. Multiplexer Section

(fig. FO-1, sheet)

a. General. A block diagram of the TD-976/G multiplexer section is shown on sheet 1 of figure FO-1. The multiplexer section accepts, sequences, and combines various data inputs into a required serial digital data format (output SG). The various data inputs accepted and processed by the multiplexer include a DDOW input (either 75- or 1200-baud rate), a DVOW input, and up to eight PCM group inputs. Additionally, the multiplexer generates, and inserts into the SG, certain O/H data that contain frame synchronization and stuffing information.

b. MO/C Card (Oscillators and Data Rate Selection). General timing and SG format makeup will be discussed first in order to estabish a basis for succeeding discussions related to the processing and multiplexing of various data inputs. Basic timing for the multiplexer is created by two oscillators and dividers on MO/C card 21A4. Both outputs of oscillator No. 1 and divider are at a 4915.2 kHz rate and sychronous with each other. The transmit master clock (TMASCLK) establishes the output SG rate and controls operation of TC (M) card 21A5 in its generation of timing signals that control makeup of the output SG format. The digital data clock (DDCLK) is used by DDOW encoder card 21A3 to control processing of teletype data into its input rate buffer. The prime output of ocillator No. 2 is the channel clock (CHAN), at 4608 kHz rate, which is used on the DGP cards to create an extracted 576 kHz clock based on incoming group data. Other outputs of oscillator No. 2 and dividers are 576 kHz, 6.4 kHz, and 1.6 kHz, which are derivatives of the



EL5NG007

Figure 2-7. Front panel 21A14.

4608 kHz output. The functions of these outputs will be covered in later discussions. As defined in paragraph 2-3*b*, the TD-976/G operates at one of two data rates (HI and LO) as controlled by the DATA RATE swith on MO/C card 21A4. When there are more than four PCM group inputs, the DATA RATE switch is placed to HI and the 96-channel enable (96 CHE) signal is generated by the data rate selection circuits. Conversely, when the DATA RATE switch is placed to LO, the 48-channel enable (48 CHE) signal is generated.

c. TC (M) Card (Clock Selection and Counters). TC (M) card 21A5 is free running and generates timing signals that control multiplexer operation in the makeup of the SG format. In addition to the block diagram, figures 2-3 and 2-4, which define the message formats, should also be referred to throughout the remainder of this subparagraph and *d* below. The transmit master clock (TMASCLK) applied to the clock selection circuits creates the transmit clock (TCLK) and its complement (TCLK—). If the TD-976/G is in 96-channel operation, the frequency of the transmit clock is 4915.2 kHz. In turn, if the TD-976/G is in 48-channel operation, the clock selection circuits, in response to the 48-channel enable (48 CHE) signal, perform a divide-by-2 operation and the frequency of the transmit clock is 2457.6 kHz. In either case, the transmit clock establishes the bit sampling rate. On TC (M) card 21A5, the transmit clock (TCLK) drives a counter chain made up of the bit counter, minor frame counter, and frame counter, with each counter's outputs being decoded by its associated decoder. One or more decoded outputs from each counter are fed back to its reset controls, providing the recycle algorithm that causes the counters to count in accordance with the format requirements. The bit counter is clocked at the bit sampling rate by the TCLK and produces a bit 17 output every 17th count (last bit of a minor frame). This, in turn, enables the minor frame counter to advance one count. At the end of minor frame 19 (20th minor frame), transmit bit time 341 (T341BT) (end-of-frame bit) is generated, enabling the frame counter to advance one count. In 96-channel operation, the frame counter will count 12 before recycling (frames 0 through 11). In 48-channel operation, the 48-channel enable (48 CHE) signal causes the frame counter to recycle every six counts (frames 0 through 5). In either case, the transmit last frame of major frame (TLFOMF) signal is active during the last frame of each major frame (either frame 11 or 5). The O/H time gate produces a transmit group enable (TGRPE—) signal that is at a low level except during O/H bit times (bit 17 and 341 times). The bit counter and decoder produces transmit channel clocks (TCHAN - 8 in 96-channel operation and TCHAN1 - 4 in 48-channel operation) that define the time for a given group to in-

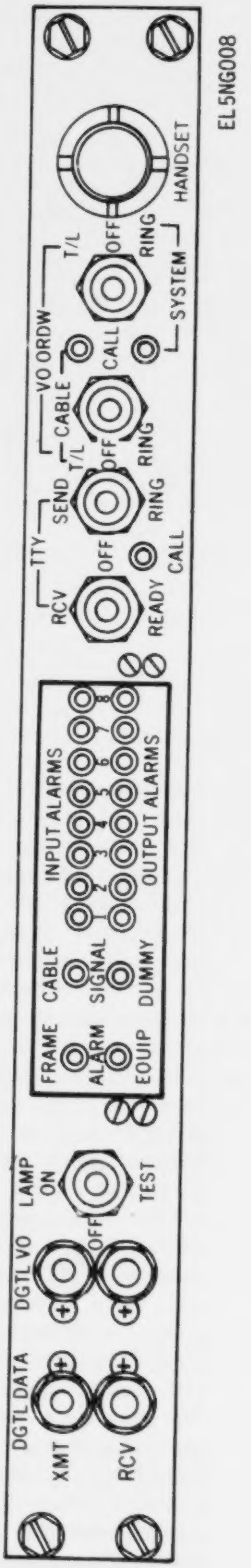

DGTL DATA
XMT
RCV
DGTL VO
OFF
LAMP
ON
TEST
FRAME
ALARM
EQUIP
CABLE
SIGNAL
DUMMY
INPUT ALARMS
1
2
3
4
5
6
7
8
OUTPUT ALARMS
TTY
RCV
READY
OFF
SEND
RING
CALL
T/L
OFF
RING
CABLE
VO ORDW
CALL
T/L
OFF
RING
SYSTEM
HANDSET
EL5NG008

Figure 2-8. RAU 21A15.

sert a bit of data into the SG. The bit counter and decoder also produces an output to the stuff circuits that is active during the time that a stuffing operation could be performed (bit times 1 - 8 minor frame 0 for 96-channel operation and bit times 1 - 4 of minor frame 0 for 48-channel operation).

d. TC (M) Card (Stuff Circuits and Timing Decode Gates). The stuff circuits, in response to minor frame counts, continually produce a transmit stuff code (TSCODE) and its complement (TSCODE—). The TSCODE— will be selected and inserted (by the combiner on MO/C card 21A4) in the O/H portion of the SG unless a stuffing action is to be performed at which time TSCODE will be selected and inserted. Additionally, TSCODE (and its complement TSCODE—) is in one of two forms. Normally, it will be in the form of the B pattern (para 2-6*e*(3)). However, during the last frame of each major frame, it is in the form of the A pattern. During bit 17 time of each minor frame 2, the stuff circuits produce a transmit stuff request strobe (TSREST) that causes the stuff request circuits on MO/C card 21A4 to sample the rate compare for either the teletype input or a designated group input. Also, if a stuffing action is to be performed, the stuff circuits generate a transmit channel clock delete (TCHN1 - 8) that is routed to the appropriate group input rate buffer to cause the actual stuffing operation to be accomplished. The timing decode gates create the various O/H time slots required for digital data, DVOW, and the frame synchronization and stuff patterns. The transmit frame code enable time (TFCET) signal is active during those bit times when the frame synchronization and stuff pattern is transmitted (bit 17 times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19). The transmit digital data orderwire (TDTAOW) signal is active only during bit 17 time of minor frame 2 of frame 0. The transmit DVOW clock (TDVOW), which represents the bit times when DVOW information is transmitted, is active during bit 17 times of minor frames 0, 5, 10, and 15 when in 96-channel operation. In 48-channel operation, TDVOW is active during bit 17 times of minor frames 0, 1, 5, 6, 10, 11, 15, and 16. The transmit DVOW smooth clock (TDVOWC—) is used by DVOW card 21A11 during 48-channel operation to ensure that the CVSD encoder has a smooth clock. This signal is active during bit 17 times of minor frames 0, 5, 10, and 15 and bit 9 times of minor frames 3, 8, 13, and 18.

e. GTM Card (Line Receivers and Activity Pattern Generator). The line receivers, of which there are eight, convert the incoming PCM group inputs (NRZ format, where a logic 1 is approximately 0 volt and a logic 0 is approximately −2 volts) to TTL levels (NRZ format, where a logic 1 is approximately +5 volts and a logic 0 is approximately 0 volt). Additionally, a reset strobe (RST—) is generated every time a positive-going data transition occurs. The activity pattern generator is clocked by the 576 kHz output 1 (576 KHZ 1) and generates two activity patterns (APAT 1 and APAT 2). Each activity pattern is 7 bits long (1011000) (last bit in time shown on left) and is repetitive. APAT 2 lags APAT 1 by three bit times.

f. DGP Card (Input Section, No Stuffing). Each DGP card contains two identical input sections, allowing it to process inputs from two groups. For simplicity, a block diagram is shown only for the input section associated with group input 1. The basic function of the input section is to perform an input rate buffering action; that is conversion of the asynchronous input group data to a data output that is synchronous with the TD-976/G timing. Refer to paragraph 2-9 for a general discussion of input rate buffering. The timing extractor divider is clocked by the 4608 kHz channel clock (CHAN) and reset by the reset strobe (RST—) to produce a 576 kHz extracted clock that is synchronous (within an eighth of a bit time) with the input group data. Normally, when a given input section is active (card-mounted switch placed to ON), the input group data and the extracted clock are routed through the input selector as the data and write clock. GTM card 21A2 (*m* below) sequentially examines the input group data lines for the presence of traffic (activity). If there is no traffic and the input section is active, AD card 21A1 will generate a high-level input good status (IGS—) signal, causing the input selector to select the dummy pattern and 576 KHZ 2 inputs as the data and write clock. If a given input section is inactive (card-mounted switch placed to OFF), the input selector will select the activity pattern and 576 KHZ 2 inputs as the data and write clock. The dummy pattern is the complement of the activity pattern. The write clock clocks data into the elastic storage register and advances the write address counter. The 3-bit write address determines the elastic storage register cell into which the data will be entered. If the data are at a 288 kbps rate (6 channels of data), each bit is entered into two successive cells of the elastic storage register and will subsequently be transmitted as 2 bits in the SG. The 3-bit read address determines the elastic storage register cell from which the data will be extracted. Each coincidence of a transmit clock (TCLK) and a transmit channel clock (TCHAN) causes the read address counter to advance one count. If a stuffing operation is to be performed (*g* below), the read address counter will be inhibited for one coincidence of a TCLK and a TCHAN.

g. DGP Card (Input Section, Stuffing). Both the read and write address counters provide a 3-bit binary address to the elastic storage register. Thus, each counter recycles after eight counts. The most significant digit of the binary output of the read address counter clocks the rate comparator flip-flop. The rate comparator flip-flop clocks on a positive-going transition, and is therefore clocked once every eight counts of the read address counter. When the flip-flop is clocked, it stores the condition of the most significant digit of the binary output of the write address counter. If the offset between the two counters is less than the desired four counts, the rate comparator flip-flop will be set, resulting in an active rate compare (RCOM) signal. The stuff request circuits on MO/C card 21A4 sequentially scan the rate compare lines (group 1 during frame 0, group 2 during frame 1, and so on). If a stuffing action is to be performed (a rate comparator flip-flop is set), the level of the no stuff output signal applied to TC (M) card 21A5 is such that a low-level transmit channel clock delete (TCHN) signal is generated and applied to the related DGP card at the appropriate time. The TCHN signal inhibits the read address counter for one coincidence of a TCLK and a TCHAN. Specifically, the low-level TCHN signal occurs during the first bit times (1 - 8 to 1 - 4) of minor frame 0 of the frame following the frame in which the given rate compare line was scanned.

h. MO/C Card (Stuff Request and Combiner Circuits). The stuff request circuits sequentially scan the rate compare (RCOM) lines from the DGP cards and the receive teletype orderwire (RTTYOW) line from DDOW encoder card 21A3 to determine if a stuff action is or is not to be performed. The scan sequence is the RCOM1 line during frame 0, RCOM2 line during frame 1, and so on. The RTTYOW line is scanned during the last frame of each major frame. The 96- and 48-channel enable (96 CHE and 48 CHE) signals, together with the transmit frame counts (TFCT01, 02, 04, and 08) and transmit frame count 11 (TFC11—) signals, control the scan sequence. Each scan period begins when a transmit stuff request strobe (TSREST) and a transmit clock (TCLK—) occur together. Timing is such that the stuff and no stuff line outputs of the stuff request circuits assume their states for the group being scanned at the start of minor frame 3. If the rate compare line for the group being scaned is active (stuffing action required), the stuff line will be at a high level and the no stuff line will be at a low level. If no stuffing action is requested, the level of the stuff line will be low and the level of the no stuff line will be high. The combiner circuits combine the teletype orderwire input (TTOWI), the DVOW input (DVOWI), the group data inputs (GRP 1 - 8), and the transmit stuff code (either TSCODE or TSCODE—) into a single serial SG nonreturn to zero output (NRZOUT). The transmit digital data orderwire (TDTAOW) signal, which occurs only at bit 17 time of minor frame 2 of frame 0, allows the combiner circuits to insert the teletype orderwire input (TTYOWI) into the SG at this time. The transmit DVOW clock (TDVOW) allows the combiner circuits to insert the DVOW input (DVOWI) into the SG at the proper times. In 96-channel operation, TDVOW is active during bit 17 times of minor frames 0, 5, 10, and 15. In 48-channel operation, TDVOW is active during bit 17 times of minor frames 0, 1, 5, 6, 10, 11, 15, and 16. The transmit group enable (TGRPE—) signal is active during all group data bit times and enables the combiner to insert group data (GRP 1 - 8) into the SG. Transmit bit counts (TBCT01, 02, and 04) control the sequence of data insertion for the various groups. The transmit frame code enable time (TFCET) signal is active during those 11 O/H bit times when the frame synchronization and stuffing pattern is inserted (B or A pattern). If a stuffing action is to be transmitted, the stuff line from the stuff request circuits enables TSCODE to be inserted into the SG. Otherwise, TSCODE— is inserted.

i. DVOW Card (Encoder). The encoder portion of DVOW card 21A11 encodes analog voice inputs into a digital form for inclusion into the SG. The digital voice microphone (DVMIC) input from AVOW card 21A10 is generated by a handset connected to the front panel (local microphone) or to either the RAU or an external orderwire control panel (remote microphone). The digital voice extension input (DVEXI) is accessed solely through the RAU and provides for entry of a second externally generated voice input. Both inputs (DVMIC and DVEXI) may be applied concurrently, in which case the talkers share the circuit much like a party line. The digital voice ring signal (DVRNGS) is a 1600 Hz analog input used to ring a far-end user. The input circuits perform an impedance matching, summing, and amplification function and supply an analog input to the continuously variable slope delta (CVSD) encoder. The timing selection circuits provide the timing input to the CVSD encoder. In 96-channel operation, the transmit DVOW clock (TDVOW) is selected as the timing input. In 48-channel operation, the transmit DVOW smooth clock (TDVOWC—) is selected. The CVSD encoder converts the analog inputs into a digital DVOWI signal that is supplied to the combiner on MO/C card 21A4 for insertion into the SG (*h* above).

j. DDOW Encoder Card (Input Circuits, Timing Extractor, and Clock Generator). Asynchronous digital data (teletype), inputted at the RAU, is processed by DDOW encoder card 21A3 to produce the synchronous teletype orderwire input (TTYOWI) applied to the combiner circuits for insertion into the SG. The teletype input may be at either a 75- or 1200-baud rate. Selection of the particular rate is accomplished by positioning jumper switches in the input circuits on DDOW encoder card 21A3 and on the RAU. An optical coupler converts the 130-volt, 75-baud teletype input to levels compatible with DDOW card 21A3. If selected, the 1200-baud teletype input, which is a low-level signal current, is applied directly to the input circuits, where a level shift to TTL levels is performed. The input circuits are enabled by the digital data send (DDSD—) signal and, depending on positioning of a jumper switch, select the data and timing to be routed to the timing extractor. Data bits are read into and stored in the timing extractor for detection of a multibit teletype character. When a character is detected, a reset signal is generated and applied to the clock generator. Data bits are continually read out of the first stage of the storage device in the timing extractor and applied to the input rate buffer. The clock generator is clocked by the 4915.2 kHz digital data clock (DDCLK). One portion of the clock generator is free running and produces the 1200 Hz write clock (divide-by-4096 operation). The other portion of the clock generator is reset by the output of the timing extractor and produces 1200 and 75 Hz outputs (divide-by-4096 and 65,536 operations) that are synchronized with the incoming teletype bits.

k. DDOW Encoder Card (Input Rate Buffer and Ring/Ready Code Generator). The input rate buffer functions in a manner similar to that of the input rate buffer on the DGP cards (*f* and *g* above). The write address counter is advanced and data (either from the timing extractor or ring/ready code generator) are clocked into the elastic storage register at a nominal 1200 Hz rate. Coincidences of transmit clocks (TCLK—) and transmit digital data orderwire (TDTAOW) signals occur at a nominal 1201 Hz rate (digital data sampling rate). Each coincidence, unless inhibited by a transmit delete (TDLTTY) signal, creates a read clock that advances the read address counter. Initially, the write address counter is preset five counts ahead of the read address counter. Since the read address counter is being clocked at a nominal 1201 Hz rate, it tends to advance on the write address counter, which is being clocked at a nominal 1200 Hz rate. The rate comparator continually compares the 3-bit write address with the 3-bit read address. When the read address counter has advanced to within four counts of the write address counter, the rate comparator generates the receive teletype orderwire (RTTYOW) signal, which is processed through the stuff request circuits on MO/C card 21A4. The resulting transmit delete (TDLTTY) signal will inhibit the next read clock from being created (stuff action performed), thereby slowing down the read address counter. The ring/ready code generator, in response to either a digital data ring (DDRG—) or a digital data ready (DDRY—) signal, will generate a 7-bit repetitive ring/ready code. This code is used either to ring or to signal a ready condition to a far-end teletype.

l. SG D/R Card (Driver Section). In normal operation, the digital loop selector routes the nonreturn to zero output (NRZOUT) (SG in TTL format) and the 4915.2 kHz transmit master clock (TMASCLK) to the NRZ-to-bipolar converter and line drivers as the data and timing inputs. Here, the data are converted to the ½-baud bipolar format for transmission over the cable system as the SG output (SGOUT1 and 2). When the DIGITAL LOOP BACK switch on the front panel is placed to ON, the resulting loopback (LOOP—) signal causes the selector to select the ½-baud polar data and extracted timing from the receiver section as the data and timing inputs. If there is no data activity at the output of the line drivers, the transmit error (XMTERR) signal will be active, causing the CABLE SIGNAL alarm indicator to light. Refer to paragraph 2-15 for a discussion relating to alarms. The transmit analog voice cable power (TAVCP) input, which consists of dc cable power and AVOW information, also is included to make up the SG output. When the CABLE TEST switch on the front panel is placed to ON, the resulting cable fault normal (CFNRM—) signal enables the SG interrupter, which performs a divide-by-16 operation of the 75 Hz clock (75CLK). The resulting 4.69 Hz output causes the SG output to turn on and off at a 4.69 Hz rate as required for cable testing. Refer to section XVI for a discussion relating to cable testing.

m. GTM Card (Input Group Data). GTM card 21A2 sequentially examines the eight input group data lines (for traffic) and the eight output group data lines (for traffic and dummy pattern). The scan interval generator controls the length of time that each group data line is examined (scan interval) and the advancing of the address counter, which, in turn, sequences the group data and timing selectors. The duration of the scan interval is approximately 10 milli-seconds after which time the scan interval generator times out and resets itself. As part of the resetting process, a group frame monitor strobe (GFMST) is generated and sent to AD card 21A1, allowing it to store the status for that group. The group frame scan address bits (GF1, 2, 4, 8, and 8-) inform the AD card as to which group is being examined. The input group data lines are sequentially connected to the group data traffic monitor, where they are examined for the presence of traffic (activity). If there is activity on the line, the good status (GS) signal is active. In turn, AD card 21A1 monitors the good status (GS) and group idle (IDLE) lines. If the group being monitored is active (not idle) and the good status (GS) signal is missing, the appropriate INPUT ALARMS indicators on the front panel and the RAU light. Refer to paragraph 2-14*k* for a discussion relating to the output group data lines. Refer to paragraph 2-15 for a discussion relating to alarms.

2-14. Demultiplexer Section

(fig. FO-1, sheet 2).

a. General. A block diagram of the TD-976/G demultiplexer section is shown on sheet 2 of figure FO-1. The demultiplexer section receives the serial digital data SG input and demultiplexes it to its various component parts, and supplies the data to the required destinations. The various demultiplexed data outputs are a DDOW output (either 75- or 1200-baud rate), a DVOW output, and up to eight PCM group outputs.

b. SG D/R Card (Receiver Section). The serial SG input (SGIN1 and 2) is converted from a ½-baud bipolar format to a ½-baud polar format, and 4915.2 kHz timing is extracted based on data transitions. Normally, the digital loop selector selects these inputs to become its data and timing outputs. However, if the DIGITAL LOOP BACK switch is placed to ON, the NRZ output (NRZOUT) and transmit master clock (TMASCLK) from the multiplexer section are selected. The NRZ data retime circuits convert the ½-baud polar data to full-width NRZ data that are outputted as receive data (RDATA). The receive master clock (RMASCLK) is always outputted at a 4915.2 kHz rate. In 96-channel operation, one bit time of RDATA is equal to one cycle of RMASCLK. However, in 48-channel operation, one bit time of RDATA (true data rate is 2457.6 kbps) is equal to two cycles of RMASCLK. In this situation, the receive phase forcing (RPHF) signal ensures that the clock selection circuits on TC (D) card 21A5 are synchronized with true RDATA bit times.

c. FS Card (Frame Sync Detection and Maintenance Circuits). The frame sync detection circuits examine the receive data (RDATA) for the frame sync pattern (B or A pattern or its complement) that was inserted by the far-end multiplexer for each frame (para 2-13*h*). To accomplish frame sync pattern detection, RDATA is shifted into a shift register at the rate of receive clock (RCLK—). When a pattern, or its complement, is detected, a major frame sync decode and/or frame sync decode is generated and supplied to the frame sync maintenance circuits. Additionally, the serial SG data (SDATA) is outputted from the frame sync detection circuits to DGP cards 21A6, DDOW decoder card 21A8, and DVOW card 21A11. Timing is such that when a major frame decode and/or frame sync decode is decoded at bit 340 time of a frame, bit 341 is present on the SDATA line. The frame sync maintenance circuits consist of two 4-stage up/down confidence counters (a frame sync confidence counter and a major frame sync confidence counter), where a maximum count represents a no-confidence condition. In a no-confidence condition, the receive frame sync (RFSYNC—) signal inhibits operation of the bit and minor frame counters on TC (D) card 21A5, while the receive major frame sync (RMSYNC—) signal inhibits operation of the frame counter. A frame sync decode enables the frame sync confidence counter, at bit 341 time (last bit of a frame), to decrement one count. This action removes RFSYNC— and allows the bit and minor frame counters to operate. In turn, a major frame sync decode enables the major frame sync confidence counter, at bit 341 time of last frame of a major frame, to decrement one count. This action removes RMSYNC— and allows the frame counter to operate. Based on frame/major frame sync decodes, the confidence counters continue either to decrement or increment. A minimum count in the confidence counters represents maximum confidence. When the count in the major frame sync confidence counter advances to or past a count of 8, the receive major frame sync level 8 (SYNC8 and SYNC8—) signals are active. In summary, the frame sync detection and maintenance circuits ensure that the demultiplexer section operates in synchronism with the far-end multiplexer section.

d. TC (D) Card (Clock Selection and Counters). The TC (D) card is the same type as the TC (M) card. The major difference in operation is that while the TC (M) card is free running, the TC (D) card is synchronized with the incoming SG format by means of the receive frame sync (RFSYNC—) and receive major frame sync (RMSYNC—) signals from the sync maintenance circuits. In addition to the block diagram, figures 2-3 and 2-4, which define the message formats, should also be referred to throughout the remainder of this subparagraph and *e* below. The receive master clock (RMASCLK) (extracted from the incoming SG at a 4915.2 kHz rate and synchronized with data transitions) is applied to the clock selection circuits to create the receive clock (RCLK) and its complement (RCLK—). If RMASCLK is not present, the receive no clock (RNOCLK and RNOCLK—) signals are active. If the TD-976/G is in 96-channel operation, the frequency of the receive clock is 4915.2 kHz. In turn, if the TD-976/G is in 48-channel operation, the clock selection circuits, in response to the 48-channel enable (48 CHE) signal, perform a divide-by-2 operation and the frequency of the receive clock is 2457.6 kHz. The receive phase forcing (RPHF) signal ensures that the divide-by-2 operation is synchronized with true data bit times (*b* above). In either case, the receive clock establishes the bit sampling rate for the demultiplexer section. On TC (D) card 21A5, the receive clock (RCLK) drives a counter chain made up of the bit counter, minor frame counter, and frame counter, with each counter's outputs being decoded by its associated decoder. One or more decoded outputs from each counter are fed back to its reset controls, providing the recycle algorithm that causes the counters to count in accordance with the format requirements. Until frame sync is initially established, the bit and minor frame counters are held in a reset state by RFSYNC—. The frame counter is held in a reset state by RMSYNC— until major frame sync is initially established. The counter chain is released to start counting at a time so that the various outputs of the TC (D) card are properly aligned with the data and O/H bits appearing on the SDATA line. The bit counter is clocked at the bit sampling rate by the RCLK and produces a bit 17 output every 17th count (last bit of a minor frame). This, in turn, enables the minor frame counter to advance one count. At the end of minor frame 19 (20th minor frame), receive bit time 341 (R341BT and R341BT—) is generated, enabling the frame counter to advance one count. In 96-channel operation, the frame counter will count 12 before recycling (frames 0 through 11). In 48-channel operation, the 48-channel enable (48 CHE) signal causes the frame counter to recycle every six counts (frames 0 through 5). In either case, coincidence of receive last frame of major frame (RLFOMF) and R341BT produces the recieve last bit of major frame (RLBMF—) signal during the last bit time of each major frame. The O/H time gate produces an output during all O/H bit times. The bit counter and decoder produces receive channel clocks (RCHAN1 - 8 in 96-channel operation and RCHAN1 - 4 in 48-channel operation) that define the time for a given group to extract a bit of data from the SDATA line. The bit counter and decoder also produces an output to the destuff circuits that is active during the time that a destuffing action could be performed (bit times 1 - 8 of minor frame 0 for 96-channel operation and bit times 1 - 4 of minor frame 0 for 48-channel operation).

e. TC (D) Card (Destuff Circuits and Timing Decode Gates). The destuff circuits, in response to minor frame counts, continually produce a receive stuff code (RSCODE) and its complement (RSCODE—) in one of two forms. Normally, they are in the form of the B pattern (para 2-6*e*(3)); however, during the last frame of each major frame, they are in the form of the A pattern. During bit 17 time of each minor frame 2, the destuff circuits produce a receive stuff request strobe (RSREST—) that resets the destuff detection circuits on FS card 21A7. Also, if a destuffing action is to be performed, the destuff circuits generate a receive channel clock delete (RCHN1 - 8) signal that is routed to the appropriate destuff gate on a DGP card to cause the actual destuffing operation to be accomplished. The timing decode gates create the various O/H time slots related to the times when specific O/H bits appear on the SDATA line. The receive frame code enable time (RFCET) signal is active during those bit times when the frame synchronization and stuff pattern is on the SDATA line (bit 17 times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19). The receive digital data orderwire (RDTAOW) signal is active only during bit 17 times of minor frame 2 of frame 0. The receive DVOW clock (RDVOW), which represents the bit times when DVOW information is received, is active during bit 17 times of minor frames 0, 5, 10, and 15 when in 96-channel operation. In 48-channel operation, RDVOW is active during bit 17 times of minor frames 0, 1, 5, 6, 10, 11, 15, and 16. The receive DVOW smooth clock (RDVOWC—) is used by DVOW card 21A11 during 48-channel operation to ensure that the DVSD decoder has a smooth clock. This signal is active during bit 17 times of minor frames 0, 5, 10, and 15 and during bit 9 times of minor frames 3, 8, 13, and 18.

f. FS Card (Destuff Detection Circuits). These circuits examine the incoming SG and determine if a stuff code action was transmitted by the far-end multiplexer. The circuits are reset by the receive stuff request strobe (RSREST—) at bit 17 time of each minor frame 2. The locally generated receive stuff code (RSCODE) is compared with the SDATA— line, and the RSCODE— is compared with the SDATA line. The receive frame code enable time (RFCET) signal is active during the 11 O/H bit times of each minor frame when the frame synchronization and stuff pattern appears on the SDATA and SDATA— lines. The destuff detection circuits, in response to the above inputs, count the number of detected bits that represent a stuff code action transmitted by the far-end multiplexer. If at least 6 bits of the 11-bit frame synchronization and stuff pattern are recognized as containing a stuff code action, the receive delete (RDLTTY) signal is generated. This, in turn, will cause a destuff action to be initiated in the demultiplexer section (*h* below).

g. DGP Card (Output Section, No Destuffing). Each DGP card contains two identical output sections, allowing it to process outputs to two groups. For simplicity, a block diagram is shown only for the output section associated with group 1. The basic function of each output section is to extract data for a given group from the incoming SG and perform appropriate destuffing and smoothing operations in order to output smooth group data and timing signals at a rate identical to that accepted by the corresponding input rate buffer at the far-end multiplexer. Refer to paragraph 2-11 for a general discussion of destuffing and smoothing. Normally, the SDATA and the output of the destuff gate are routed through the output selector as the data and write clock. Each coincidence of a receive clock (RCLK—) (extracted clock at bit sampling rate) and a receive channel clock (RCHAN) (given group's turn to extract a data bit from the SG) results in a write clock. The write clocks, which correspond in time to the bit positions in the SG containing data for this group, clock these data bits into the elastic storage register and advance the write address counter. The 3-bit write address determines the elastic storage register cell into which the data bit will be entered. Data within the elastic storage register are extracted under control of the read address counter clocked by the output of the phase-locked loop (nominal 576 kHz rate). The 3-bit read address determines which elastic storage register cell will be connected to the output logic. The write clocks do not occur at uniform intervals (especially if a destuffing action (*h* below) is performed) However, the output of the phase-locked loop, which is also used to create output group timing, must be a smooth clock that is acceptable to all group interfacing equipments. The phases of the 4th bit of the write and read addresses are compared by the phase-locked loop. If they are not in phase, the phase-locked loop performs a gradual correction so that its output represents the average frequency of the write clocks. In the event the demultiplexer section is unable to acquire major frame sync (RMSYNC— is active) or a given output section is inactive (card-mounted switch is placed to OFF), the activity pattern (APAT) and the 576 KHZ 2 signal are routed through the output selector as the data and write clock. This enables the phase-locked loop to continue operation. The output logic converts the data and timing outputs of the output rate buffer to levels compatible with the interfacing equipments. Also GTM card 21A2 sequentially examines the output group data lines for the presence of activity and a dummy pattern (*k* below).

h. DGP Card (Output Section, Destuffing). Periodically, write clocks will be inhibited as a result of destuffing operations. If a destuffing operation is to be performed, the destuff detection circuits of FS card 21A7 will detect this fact and generate a receive delete (RDLTTY) signal that is routed to the destuff circuits on TC (D) card 21A5. In turn, a low-level receive channel clock delete (RCHN) signal is generated and applied to the destuff gate on the related DGP card at the appropriate time and inhibits the creation of one write clock. Specifically, the low-level RCHN signal occurs during the first bit times (1 - 8 or 1 - 4) of minor frame 0 in the frame following the frame in which the destuff action was detected.

i. DVOW Card (Decoder). The decoder portion of DVOW card 21A11 extracts the digital DVOW information from the incoming SG and decodes the digital information into an analog voice form. The timing selection circuits provide the clocks to the input data buffer and the CVSD decoder. The receive DVOW clock (RDVOW), which represents the bit times when DVOW information is on the SDATA line, is always used to create the clock to the input data buffer. This allows the input data buffer to extract the DVOW information from the incoming SG. In 96-channel operation, RDVOW also creates the clock to the CVSD decoder. In 48-channel operation, the receive DVOW smooth clock (RDVOWC—) creates the clock to the CVSD decoder. The CVSD decoder decodes the input digital data into an analog voice form that is routed through amplifiers in the output circuits. The resulting digital voice earphone (DVEAR) output is processed through AVOW card 21A10 to handsets connected either to the front panel (local earphone) or to the RAU or an external orderwire control panel (remote earphone). Additionally, the digital voice extension output (DVEXO) is routed through the RAU to a remotely connected handset. The ring detector circuits monitor the output of the CVSD decoder for the presence of a 1600 Hz ring signal. When a ring signal is detected, the digital voice call (DVCAL—) signal is generated, which, after being processed through AD card 21A1, causes the VOICE O.W. SYSTEM CALL indicator on the front panel and the VO ORDW SYSTEM CALL indicator on the RAU to light and the audible alarms on the front panel and external orderwire control panel to sound. The local digital talk/listen (LDTL—) or remote digital talk/listen (RDTL—) signal resets the ring detector circuits.

j. DDOW Decoder Card. This card extracts the DDOW data from the incoming SG, performs appropriate destuffing and smoothing operations, and outputs the data (at either a 75- or 1200-baud rate), in the proper format, to the RAU, which provides the interface with the teletype. The digital data 75-baud enable (D75EN) or digital data 1200-baud enable (D12EN) signal controls the output circuits as to the rate and format of the data outputs. The smoothing buffer functions in a manner similar to that of the output rate buffer on the DGP card (*g* above). Coincidences of receive clocks (RCLK—) and receive digital data orderwire (RDTAOW) signals occur at a nominal 1201 Hz rate (digital data sampling rate). Each coincidence, unless inhibited by a receive delete (RDLTTY) signal (destuffing action), creates a write clock that advances the write address counter and clocks a data bit from the SDATA line into the elastic storage register. Thus, write clocks occur at an average 1200 Hz rate (due to destuffing actions), but not at uniform intervals, and correspond in time to the bit positions in the SG containing DDOW information. The 4915.2 kHz receive master clock (RMASCLK) is divided by 4096 to produce a 1200 Hz read clock that advances the read address counter. During initial power on, the power on reset (PRS—) signal causes the counters to be preset so that the read address counter lags the write address counter by four counts. Thereafter, this offset of four counts will be maintained since each counter is being clocked at a 1200 Hz rate. If the major frame sync confidence counter advances to or past a count of 8, the receive major frame sync level 8 (SYNC 8—) signal is active and holds the smoothing buffer counters in their preset states. If the smoothing buffer is not being used (TTY switches on RAU are placed to OFF, and a call is not being received), the resync circuit functions to periodically preset the counters and maintain the desired four-count offset. The ring/ready pattern detector and counter examines the data output of the smoothing buffer for the presence of a 7-bit ring/ready pattern (0100111, last bit in time shown on left).

When this pattern is detected and counted eight times, the call circuits are set and produce the digital data call (DDCAL—) signal.

k. GTM Card (Output Group Data). GTM card 21A2 (fig. FO-1, sheet 1) sequentially examines the output group data lines for traffic and a dummy pattern. Operation of the scan interval generator, address counter, and group data and timing selectors is as described in paragraph 2-13*m*. The output group data lines are sequentially connected to the group data traffic monitor, where they are examined for the presence of traffic (activity). If there is no activity on the line, the good status (GS) signal will not be present, and AD card 21A1 causes the appropriate OUTPUT ALARMS indicators on the front panel and the RAU to light. The dummy pattern detector and counter concurrently is examining the selected output group data line for the presence of a 7-bit dummy pattern. When this pattern is detected and counted eight times, the dummy sync (DS) signal is present, and after processing by AD card 21A1, causes the DUMMY SIGNAL alarm indicators on the front panel and the RAU to light.

2-15. Alarms

a. General. Alarm indicators are located on front panel 21A14 (fig. 2-7) and on the edges of five of the printed circuit cards (MO/C 21A4, (TC (M) 21A5, TC (D) 21A5, FS 21A7, and SG D/R 21A9). The front panel alarm indicators are also duplicated on RAU 21A15 (fig. 2-8). An audible alarm is also mounted on the front panel. The alarm circuits monitor various signals and functions within the TD-976/G and provide audible and visual indications and control signals when the required signals or functions are not detected. The alarm discussions are divided into eight major areas as follows:

(1) *INPUT/OUTPUT ALARMS.* These alarms monitor for loss of traffic (activity) on each of the PCM group input and output lines (*b* and *c* below).

(2) *CABLE SIGNAL.* This alarm monitors for loss of traffic (activity) at the SG output of the multiplexer section (*d* below).

(3) *DUMMY SIGNAL.* This alarm monitors for the presence of a dummy pattern in any of the PCM group outputs (*e* below).

(4) *EQUIP ALARM.* This alarm monitors the status of various operational aspects of the TD 976/G. When this alarm indicator is lit, one or more of the alarm indicators on the edges of the printed circuit cards will also be lit (*f* below).

(5) *FRAME ALARM.* This alarm monitors for loss of frame/major frame synchronization within the demultiplexer section (*f* below).

(6) *Alarm clear circuits.* These circuits force a good condition (clear) into the status storage for the input and/or output groups and dummy storage during initial power on or when certain TD-976/G faults occur. This action prevents the DUMMY SIGNAL ALARM and INPUT/OUTPUT ALARMS indicators from lighting (*g* below).

(7) *Audible alarm modulator/driver.* These circuits cause the audible ALARM horn on the front panel to sound in one of two ways. Orderwire calls (para 2-16) will cause a continuous sound, while various alarm functions (*h* below) cause the horn to produce an alternating on-off beeping sound.

(8) *Alarm test driver.* The alarm test driver drives the front panel and RAU indicators when an alarm test is initiated (*i* below).

b. INPUT ALARMS (fig. FO-1, sheet 3). As explained in paragraph 2-13*m*, GTM card 21A2 sequentially examines the eight input group data lines for the presence of traffic (activity). If activity is present, the good status (GS) signal generated by GTM card 21A2. The status for each input group is stored in the status storage (input groups) section of AD card 21A1. The group frame monitor strobe (GFMST) allows the status to be entered through the input gates into storage, while the group frame scan address bit (GF1, GF2, and GF4) direct where the status will be stored (one of eight locations). If a given group is inactive (card-mounted switch on DGP card is placed to OFF), the resulting high-level group idle (IDLE) signal from GTM card 21A2 forces a good status condition to be stored for that group. If the status stored for a given group is not good (group is active but there is no traffic at its input), it will enable the associated input alarm driver, which, in turn, will cause the related INPUT ALARMS indicators on front panel 21A14 and RAU 21A15 to light. The input good status (IGS—) signal is routed to the associated DGP card, where it will cause a dummy pattern to be inserted in the SG for that group. Additionally, an output from the input alarm drivers is routed through the group input traffic gates, causing the audible alarm modulator/driver to drive the audible ALARM horn on front panel 21A14. In this instance, the horn will produce an alternating on-off beeping sound. Sounding of the horn is terminated when the ALARM RESET switch is pressed, which creates the audible alarm reset switch (AARSSW) signal that resets the audible alarm modulator/driver.

c. OUTPUT ALARMS (fig. FO-1, sheet 3). As explained in paragraph 2-14*k*, GTM card 21A2 sequentially examines the eight output group data lines for the presence of traffic (activity) and a dummy pattern. If activity is present, the good status (GS) signal is generated by GTM card 21A2. The status for each output group is stored in the status storage (output groups) section of AD card 21A1. The group frame monitor strobe (GFMST) allows the status to be entered through the input gates into storage, while the group frame scan address bits (GF1, GF2, and GF4) direct where the status will be stored (one of eight locations). If a given group is inactive (card-mounted switch on DGP card is placed to OFF), the resulting high-level group idle (IDLE) signal from GTM card 21A2 forces a good status condition to be stored for that group. If the status stored for a given group is not good (group is active but there is no traffic at its output), it will enable the associated output alarm driver, which, in turn, will cause the related OUTPUT ALARMS indicators on front panel 21A14 and RAU 21A15 to light. The audible ALARM horn does not sound for a group output alarm condition.

d. CABLE SIGNAL (fig. FO-1, sheet 3). As explained in paragraph 2-13*l*, the transmit error (XMTERR) signal is active whenever there is no data activity at the SG output of the driver section of SG D/R card 21A9. The XMTERR signal is processed by the cable output traffic gates to create the SG cable lamp (SGCLPS) signal, which causes the CABLE SIGNAL indicators on front panel 21A14 and RAU 21A15 to light. Additionally, the audible alarm modulator/driver is enabled and causes the audible ALARM horn to produce an alternating on-off beeping sound. Sounding of the horn is terminated when the ALARM RESET switch is pressed, which creates the audible alarm reset switch (AARSSW) signal that resets the audible alarm modulator/driver.

e. DUMMY SIGNAL (fig. FO-1, sheet 3). As explained in paragraph 2-14*k*, GTM card 21A2 sequentially examines the eight output group data lines for the presence of traffic (activity) and a dummy pattern. If a dummy pattern is detected and counted eight times for any group, the dummy sync (DS) signal is generated by GTM card 21A2 and the status is stored in the dummy storage section of AD card 21A1. The group frame monitor strobe (GFMST) allows the status to be entered through the input gates into storage, while the group frame scan address bits (GF1, GF2, and GF4) direct where the status will be stored (one of eight locations). If a dummy status is stored for any group, it will be routed through the dummy combiner gates and driver, creating the dummy lamp (DMLPS) signal, which will cause the DUMMY SIGNAL indicators on front panel 21A14 and RAU 21A15 to light. The audible ALARM horn does not sound for a dummy alarm condition.

f. EQUIP ALARM and FRAME ALARM (figs. FO-1 and FO-2). Figure FO-2 is a simplified diagram of the EQUIP ALARM and FRAME ALARM circuits and should be used in conjunction with the block diagram in figure FO-1 throughout the following discussion. The "SYMPTOM" column of the chart on figure FO-2 lists the various functions monitored by the EQUIP ALARM and FRAME ALARM circuits and indicates, by a filled-in circle, which alarm indicators will light if a given function is missing.

(1) The diagnostic detector circuits on MO/C card 21A4 monitor for the presence of the 576 KHZ 1 signal and that stuff requests are occurring. If either function is missing, the transmit diagnostic enable priority 4 (TDEP4) signal is generated. If TC (M) card 21A5 is operating (TLFOMF activity monitor not timed out), the transmit diagnostic alarm priority (TDAP24—) signal is created. In turn, this causes the diagnostic indicator on MO/C card 21A4 to light and creates the transmit diagnostic fault (TDFALT) signal. The TDFALT signal is routed through the diagnostic fault gates on AD card 21A1 and causes the EQUIP ALARM indicator on the front panel to light. Additionally, the TDFALT signal clears the status storage for the input groups (this action inhibits the lighting of any INPUT ALARMS indicators) and causes the audible ALARM horn to produce an alternating on-off beeping sound.

(2) The TLFOMF activity monitor checks that the counter chain on TC (M) card 21A5 is operating. If the counter chain is not operating (T341BT and/or TLFOMF signals missing), the TLFOMF activity monitor will time out, inhibiting U17-3 and enabling U17-6. This causes the diagnostic indicator on TC (M) card 21A5 to light and creates the TDFALT signal. As explained in (1) above, the TDFALT signal causes the EQUIP ALARM indicator to light, clears the status storage for the input groups, and causes the audible ALARM horn to produce an alternating on-off beeping sound.

(3) The clock traffic detector on TC (D) card 21A5 monitors for the presence of the receive master clock (RMASCLK) produced by SG D/R card 21A9. If RMASCLK is missing, the clock traffic detector times out and produces the receive no clock signals (RNOCLK, RNOCLK—). In turn, the RNOCLK— signal presets the frame sync confidence counter, in the frame sync maintenance circuits, to a no-confidence condition, which inhibits operation of the counter chain on TC (D) card 21A5 (para 2-14*c* and *d*). The RNOCLK signal causes the diagnostic indicator on SG D/R card 21A9 to light and also is routed through the sync/RNOCLK gates on AD card 21A1 to produce the receive diagnostic enable priority 2 signal (RDEP2, RDEP2—) and the SG sync lamp (SGSLPS) signal. The SGSLPS signal causes the FRAME ALARM indicator on the front panel to light. The RDEP2 signal is routed to the diagnostic detector on TC (D) card 21A5, where it produces the receive diagnostic fault (RDFALT) and receive diagnostic alarm priority (RDAP24—) signals. The RDAP24— signal causes the diagnostic indicator on FS card 21A7 to light. The RDFALT signal is routed through the diagnostic fault gates on AD card 21A1, causing the EQUIP ALARM indicator on the

front panel to light. Additionally, the RDFALT signal clears the status storage for the output groups and dummy storage (this action inhibits the lighting of the DUMMY SIGNAL and any OUTPUT ALARMS indicators) and causes the audible ALARM horn to produce an alternating on-off beeping sound.

(4) The destuff request activity monitor checks that destuff requests are occurring (receive delete (RDLTTY) signals occurring). If this function is missing, the receive diagnostic enable priority 4 (RDEP4) signal is generated. If TC (D) card 21A5 is operating (RLFOMF activity monitor not timed out), the receive diagnostic alarm priority (RDAP24—) signal is created. In turn, this causes the diagnostic indicator on FS card 21A7 to light and creates the receive diagnostic fault (RDFALT) signal. As explained in (3) above, the RDFALT signal causes the EQUIP ALARM indicator to light, clears the status storage for the output groups and dummy storage, and causes the audible ALARM horn to produce an alternating on-off beeping sound.

(5) The receive major frame sync level 8 (SYNC8) signal is active whenever the four-stage major frame sync confidence counter, in the frame sync maintenance circuits, has incremented eight or more counts from its maximum confidence condition (para 2-14c). The SYNC8 signal is routed through the sync/RNOCLK gates on AD card 21A1 to produce the receive diagnostic enable priority 2 signals (RDEP2, RDEP2—) and the SG sync lamp (SGSLPS) signal. As explained in (3) above, the SGSLPS signal causes the FRAME ALARM indicator on the front panel to light and the RDEP2 signal creates the RDFALT and RDAP24— signals. In turn, the RDAP24— signal causes the diagnostic indicator on FS card 21A7 to light and the RDFALT signal causes the EQUIP ALARM indicator to light, clears the status storage for the output groups and dummy storage, and causes the audible ALARM horn to produce an alternating on-off beeping sound.

(6) The RLFOMF activity monitor checks that the counter chain on TC (D) card 21A5 is operating. If the counter chain is not operating (R341BT and/or RLFOMF signals missing), the RLFOMF activity monitor will time out, inhibiting U17-3 and enabling U17-6. This causes the diagnostic indicator on TC (D) card 21A5 to light and creates the RDFALT signal. As explained in (3) above, the RDFALT signal causes the EQUIP ALARM indicator to light, clears the status storage for the output groups and dummy storage, and causes the audible ALARM horn to produce an alternating on-off beeping sound.

g. Alarm Clear Circuits (figs. FO-1, sheet 3, and FO-2). During initial power on, the power on reset (PRS—) signal causes the alarm clear circuits to clear the status storage for the input groups and output groups and dummy storage (this action inhibits the DUMMY SIGNAL and INPUT/OUTPUT ALARMS indicators from lighting). The group frame monitor terminal count (GFMTC—) signal, which occurs after GTM card 21A2 has completed one sequential scan of all input and output group data lines, resets the alarm clear circuits. Additionally, a transmit diagnostic fault (TDFALT) or a receive diagnostic fault (RDFALT) signal will cause portions of storage to be cleared. The TDFALT signal clears the status storage for the input groups, while the RDFALT signal clears the status storage for the output groups and dummy storage.

h. Audible Alarm Modulator/Driver (fig. FO-1, sheet 3). The audible alarm modulator/driver produces the audible alarm (AALRM—) signal that drives the audible ALARM horn on the front panel. Orderwire calls (DDCAL—, DVCAL—, or AVCAL—) create a constant AALRM— signal, causing the horn to produce a continuous sound. The audible alarm modulator/driver also produces an alternating on-off AALRM— signal that causes the horn to produce a beeping sound whenever there is a change in status of any of the following:

(1) Any group input.
(2) XMTERR.
(3) TDFALT.
(4) RDFALT.

Pressing of the ALARM RESET switch on the front panel resets the audible alarm modulator/driver and silences the beeping sound of the horn.

i. Alarm Test Driver (fig. FO-1, sheet 3). An alarm test, which checks out the indicators and ALARM Horn on the front panel and the indicators on the RAU, can be initiated either by the ALARM TEST switch on the front panel or the LAMP switch on the RAU. Either the internal alarm test (INAT) or external alarm test (EXAT) signal will activate the alarm test driver, causing the various indicators to light and the audible ALARM horn to produce an alternating on-off beeping sound.

2-16. Orderwires

(fig. FO-1)

a. General. This paragraph contains the overall block diagram discussion related to the three types of orderwires processed by the TD-976/G. The overall functional application of the orderwires is discussed in paragraph 2-4. The block diagram discussions for the orderwires are discussed in the following sequence.

(1) DVOW in *b* below.
(2) DDOW in *c* below.
(3) AVOW in *d* below.

b. DVOW. The DVOW circuits on AVOW card 21A10 (sheet 3) provide the interface between handsets connected to the front panel, the RAU, or an external orderwire control panel and the common DVOW card 21A11.

(1) A DVOW call is initiated from the front panel when the VOICE O.W. SELECT switch is placed to SYSTEM and the VOICE O.W. TALK/LISTEN-OFF-RING switch is placed to RING. Similarly, a DVOW call is initiated from the RAU when the VO ORDW SYSTEM T/L-OFF-RING switch is placed to RING. Either of these actions creates the digital voice ring (DVRNG—) signal that enables the ring generator on AVOW card 21A10 to process its 1.6 kHz input into a digital voice ring signal (DVRNGS) for calling a far-end TD-976/G. DVRNGS is encoded by DVOW card 21A11 into digital data that are multiplexed into the outgoing SG (para 2-13*i*).

(2) After a ring has been initiated, the VOICE O.W. TALK/LISTEN-OFF-RING switch on the front panel is placed to TALK/LISTEN. This creates the local digital talk/listen (LDTL—) signal that allows the handset connected to the front panel to interface with the DVOW circuits on AVOW card 21A10. Similarly, placing the VO ORDW SYSTEM T/L-OFF-RING switch on the RAU to T/L creates the remote digital talk/listen (TDTL—) signal that allows the handset connected to the RAU to interface with the DVOW circuits. The LDTL— and/or RDTL— signals enable specific portions of the DVOW circuits to process the local microphone (LMIC) and/or remote microphone (RMIC) signal into the digital voice microphone (DVMIC) output that is routed to DVOW card 21A11. DVOW card 21A11 encodes DVMIC into digital data that are multiplexed into the outgoing SG (para 2-13*i*). The returning decoded digital voice earphone (DVEAR) (para 2-14*i*) is processed by the DVOW circuits to produce the local earphone (LEAR) and/or remote earphone (REAR) signal.

(3) The RAU contains a multipin connector that provides for connection to an external orderwire control panel to which handset(s) may also be connected. The interface for these handset(s) is controlled by the RAU in the same manner as for the handset connected to the RAU. The press-to-talk (PTT—) signal enables the DVOW circuits to process audio signals applied as the common bus (CMBUS) input.

(4) When a TD-976/G is rung by a far-end TD-976/G as a prelude to a DVOW call being conducted, the ring detector circuits on DVOW card 21A11 detect this condition and generate a digital voice call (DVCAL—) signal. The DVCAL— signal is applied to the orderwire control circuits on AD card 21A1, causing the following three events to occur.

(*a*) The digital voice call signal (DVCALS) is produced, which causes VOICE O.W. SYSTEM CALL indicator on the front panel to light.

(*b*) The remote digital voice call signal (RDVCALS) is produced, which causes the VO ORDW SYSTEM CALL indicator on the RAU to light.

(*c*) The console audible (CNSAUD—) signal is generated and applied to the audible alarm modulator/driver, which, in turn, produces the audible alarm (AALRM—) signal that causes the audible ALARM horn on the front panel to sound. The CNSAUD— signal is also routed to the external orderwire control panel.

(5) The audible ALARM horn is silenced and the CALL indicators are turned off when the DVCAL— signal is removed from the orderwire control circuits. This is accomplished by application of either an LDTL— or RDTL— signal to the ring detector circuits on DVOW card 21A11 (sheet 2). LDTL— is generated when the front panel VOICE O.W. SELECT switch is placed to SYSTEM and the VOICE O.W. TALK/LISTEN-OFF-RING switch is placed to TALK/LISTEN. RDTL— is generated when the VO ORDW SYSTEM T/L-OFF-RING switch on the RAU is placed to T/L. At this time, the appropriate front panel or RAU switches are in positions that enable the DVOW circuits for two-way audio transmissions.

(6) Additionally, the RAU has two jacks that provide an interface between an external 4-wire, 600-ohm orderwire source and DVOW card 21A11. The DGTL VO XMT jack (sheet 1) is a direct connection for a digital voice extension input (DVEXI). The DGTL VO RCV jack (sheet 2) is a direct connection for a digital voice extension output (DVEXO).

c. DDOW. A typical operational sequence for making a TTY call and subsequent TTY data transmission is described in (1) through (3) below. The DGTL DATA XMT and DGTL DATA RCV jacks on the front of the RAU provide the means for connecting a teletype to the TD-976/G.

(1) A DDOW call is initiated when the TTY SEND-OFF-RING switch on the RAU (sheet 1) is placed to RING, which applies the digital data ring (DDRG—) signal to the ring/ready code generator on DDOW encoder card 21A3. DDRG— enables the ring/ready code generator to output a 7-bit repetitive ring/ready code that is processed through the input rate buffer and combined in the outgoing SG to ring a far-end TD-976/G. The DDRG— signal is also applied as an inhibit input to the resync circuit on DDOW decoder card 21A8 (sheet 2).

(2) The far-end TD-976/G acknowledges the transmitted ring and indicates its readiness to receive TTY data by having its TTY RCV-OFF-READY switch placed to READY. This causes the far-end TD-976/G to generate a 7-bit repetitive ring/ready code that is multiplexed into its outgoing SG. The ring/ready pattern detector and counter on DDOW decoder card 21A8 (sheet 2) detects the ring/ready pattern in the incoming SG and sets the call circuits, producing the digital data call (DDCAL—) signal. DDCAL— is applied to the orderwire control circuits on AD card 21A1 (sheet 3), causing the following two events to oc-

cur.

(*a*) The digital data call signal (DDCALS) is produced, which causes the TTY CALL indicator on the RAU to light.

(*b*) The console audible (CNSAUD) signal is generated and applied to the audible alarm modulator/driver, which, in turn, produces the audible alarm (AALRM—) signal that causes the audible ALARM horn on the front panel to sound. The CNSAUD— signal is also routed to the external orderwire control panel.

(3) Transmission of TTY data is then initiated from the near-end TD-976/G by having its TTY SEND-OFF-RING switch on the RAU placed to SEND (sheet 1), which creates the digital data send (DDSD—) signal. DDSD— enables DDOW encoder card 21A3 to process TTY data for multiplexing into the outgoing SG. DDSD— also inhibits the resync circuit on DDOW decoder card 21A8 (sheet 2) and resets the call circuits. Resetting of the call circuits removes the DDCAL— signal, which turns off the TTY CALL indicator and silences the audible ALARM horn.

d. AVOW. The AVOW circuits on AVOW card 21A10 (sheet 3) provide the interface between handsets connected to the front panel, the RAU, or an external orderwire control panel and the orderwire transformers.

(1) An AVOW call is initiated from the front panel when the VOICE O.W. SELECT switch is placed to CABLE and the VOICE O.W. TALK/LISTEN-OFF-RING switch is placed to RING. Similarly, an AVOW call is initiated from the RAU when the VO ORDW CABLE T/L-OFF-RING switch is placed to RING. Either of these actions creates the analog voice ring (AVRNG—) signal that enables the ring generator on AVOW card 21A10. The 1.6 kHz output of the ring generator is processed through the AVOW circuits and orderwire transformer 21A13T1 and is superimposed on the outgoing SG to ring a far-end TD-976/G.

(2) After a ring has been initiated, the VOICE O.W. TALK/LISTEN-OFF-RING switch on the front panel is placed to TALK/LISTEN. This creates the local analog talk/listen (LATL—) signal that allows the handset connected to the front panel to interface with the AVOW circuits on AVOW card 21A10. Similarly, placing the VO ORDW CABLE T/L-OFF-RING switch on the RAU to T/L creates the remote analog talk/listen (RATL—) signal that allows the handset connected to the RAU to interface with the AVOW circuits. The LATL— and/or RATL— signal enables specific portions of the AVOW circuits to process the LMIC and/or RMIC input for application to the outgoing SG through orderwire transformer 21A13T1. Orderwire transformer 21A13T2 extracts AVOW information from the incoming SG, and the AVOW circuits process this information to produce the LEAR and/or REAR output.

(3) The RAU contains a multipin connector that provides for connection to an external orderwire control panel to which handset(s) may also be connected. The interface for these handset(s) is controlled by the RAU in the same manner as for the handset connected to the RAU. The press-to-talk (PTT—) signal enables the AVOW circuits to process audio signals applied as the common bus (CMBUS) input.

(4) When a TD-976/G is rung by a far-end TD-976/G as a prelude to an AVOW call being conducted, the AVOW circuits detect this condition and generate an analog voice call (AVCAL—) signal. The AVCAL— signal is applied to the orderwire control circuits on AD card 21A1, causing the following three events to occur.

(*a*) The analog voice call signal (AVCALS) is produced, which causes the VOICE O.W. CABLE CALL indicator on the front panel to light.

(*b*) The remote analog voice call signal (RAVCALS) is produced, which causes the VO ORDW CABLE CALL indicator on the RAU to light.

(*c*) The console audible (CNSAUD—) signal is generated and applied to the audible alarm modulator/driver, which, in turn, produces the audible alarm (AALRM—) signal that causes the audible ALARM horn on the front panel to sound. The CNSAUD— signal is also routed to the external orderwire control panel.

(5) The audible ALARM horn is silenced and the CALL indicators are turned off when the AVCAL— signal is removed from the orderwire control circuits. This is accomplished by application of either a LATL— or RATL— signal to the AVOW circuits.

2-17. Power

(fig. FO-1, sheet 3)

a. AC power (115 v, 50 or 60 Hz) is applied through the POWER SUPPLY switch on front panel 21A14 to power supply 21A12. The POWER AC indicator is lit whenever ac power is applied to the power supply. Power supply 21A12 produces the regulated dc output voltages (+5, +12, −12, and −4.4) required to operate the TD-976/G cards and assemblies. The POWER DC indicator on the front panel is lit when the power supply is operating properly. Refer to section XV for information regarding the power supply and distribution of its output voltages.

b. Power supply 21A12 also contains a constant current regulator that produces a 45-milliampere constant current to power the TD-982/G pulse form restorers in the SG cable system. Refer to section XVI for information relating to cable power distribution.

c. A cable test capability is also included in the TD-976/G to confirm that the SG cable system is operating properly and, if the cable system is not operating properly, to identify which TD-982/G is malfunctioning. The spike filter, the CABLE TEST switch and CABLE FAULT detection indicators on front panel 21A14, the clamp on SG D/R card 21A9, and the cable fault circuits on AVOW card 21A10 are associated with the cable test function. Refer to section XVI for a discussion of cable testing and to section XVII for information relating to the cable fault circuits on AVOW card 21A10.

Section V. MASTER OSCILLATOR/COMBINER (MO/C) CARD 21A4

2-18. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the MO/C card. There is one MO/C card (21A4) in the TD-976/G. Two crystal oscillators on the MO/C card create the basic frequencies from which multiplexer section rate timing and SG message formatting signals are derived. The stuff request circuits detect stuff/no stuff requirements, causing the multiplexer section to transmit appropriate codes and, if required, perform stuff actions. The combiner circuits sequentially gate various group data and O/H information as required to assemble minor frames, frames, and major frames of the SG message format. The block diagram discussion in paragraph 2-19 is based on the MO/C card block diagram in figure 2-9. The theory of operation in paragraph 2-20 is based on the MO/C card schematic diagram in figure FO-3.

2-19. Block Diagram Discussion

(fig. 2-9)

a. General. The block diagram discussion is divided into seven functional circuit descriptions as follows:

(1) Oscillator No. 1 and its divider (*b* below) create a basic 9830.4 kHz frequency and divide it by 2 into identical 4915.2 kHz transmit master clock and digital data clock signals.

(2) Oscillator No. 2 and its dividers (*c* below) create a basic 4608 kHz frequency and divide it down into five timing signal outputs.

(3) The combiner circuits (*d* below) gate group data and various O/H information bits to sequentially assemble them in the SG message format.

(4) The stuff request circuits (*e* below) monitor the rate compare signals from the DGP cards and the receive teletype orderwire signal from the DDOW encoder card for stuff requirements. Detected stuff and no stuff signals control whether a stuff or a no stuff code pattern is gated into SG data by the combiner circuits and if the multiplexer section performs a stuff operation.

(5) The data rate selection circuits (*f* below) provide for switch selection of a high (4915.2 kbps) or low (2457.6 kbps) data sampling rate for 96- or 48-channel operation, respectively.

(6) The diagnostic detector circuits (*g* below) monitor stuff request activity and a 576 kHz output signal. The circuits activate a diagnostic fault signal when stuff request or 576 kHz signal transitions do not occur regularly.

(7) The power on circuits (*h* below) produce a negative pulse when equipment power is turned on. This pulse initializes functional circuits on various circuit cards.

b. Oscillator No. 1 and Divider. Crystal oscillator No. 1 (Y2) creates a 9830.4 kHz signal. Divider U20, a flip-flop, divides the oscillator output frequency by 2. Inverters U27 invert the 4915.2 kHz output of U20 into identical transmit master clock (TMASCLK) and digital data clock (DDCLK) signals for off-card use.

c. Oscillator No. 2 and Dividers.

(1) Crystal oscillator No. 2 (Y1) creates a 4608 kHz signal. Inverter U27 inverts Y1's output to a divider circuit and to inverter U35. U35 restores the signal to a 4608 kHz channel clock (CHAN) for use by DGP cards.

(2) Divider U21, a binary counter, divides its 4608 kHz input clock by 8. The inverters (U28) restore the counter's single output into identical 576 KHZ 1 and 576 KHZ 2 signals. The 576 KHZ 2 signal goes off card; the 576 KHZ 1 signal also goes off card, to the diagnostic detector circuits and to a divide-by-45 circuit.

(3) The divide-by-45 circuit divides its 576 KHZ 1 input clock by 45. Its binary counter (U15) and two flip-flops (U20 and U16) are interconnected through gates to perform the divide-by-45 operation. A 12.8 kilopulses per second (kpps) output drives divider U26.

(4) Divider U26, a binary counter, performs divide-by-2 and divide-by-8 operations and produces 6.4 KHZ and 1.6 KHZ square wave outputs.

d. Combiner Circuits.

(1) Six gates and two inverters make up the gating circuit. Stuff and no stuff signals control two AND gates (U22) for transfer of transmit stuff code (TSCODE) or its complement (TSCODE—) to retime flip-flop U17. A transmit frame code enable time (TFCET) signal lets the selected (stuff or no stuff) gate operate at bit 17 times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, and 19. An AND gate (U29) monitors digital voice orderwire input (DVOWI) and digital voice orderwire clock (TDVOW) signals. TDVOW times the passage of a DVOWI bit through the gate at bit 17 times of minor frames 0, 5, 10, and 15 (96-channel operation) and 1, 6, 11, and 16 (48-channel operation). Another AND gate (U25) monitors teletype orderwire input (TTYOWI)

and transmit digital data orderwire clock (TDTAOW) inputs. TDTAOW times the passage of a TTYOWI bit through the gate only at bit 17 time of minor frame 2 in frame 0 of each major frame. One OR gate and two inverters restore the four AND gates' outputs to a second OR gate (U23), which inverts its four input signals onto a common line to retime flip-flop U17.

(2) Data selector U34 sequentially multiplexes group data bits through gate U23 as required for 96- or 48-channel operation. A transmit group enable (TRGPE—) and transmit bit count (TCT01, 02, 04) signals control U34. All three bit count inputs increment repeatedly to sequentially select GRP 1 through GRP 8 data bits twice during each minor frame in 96-channel operation. The most significant bit count signal (TBCT04) stays low during 48-channel operation, and the remaining two bit count signals select GRP 1 through GRP 4 data bits four times during each minor frame. TGRPE— goes high and inhibits the data selector during O/H bit times (bit 17 of each minor frame and end-of-frame bit 341).

(3) Retime flip-flop U17 retimes and restores group data and O/H bits received from the gating circuit. Transmit clock (TCLK) positive transitions serially clock the data and overhead bits through U17 onto the nonreturn of zero output (NRZOUT) line for application to SG D/R card 21A9.

e. Stuff Request Circuits.

(1) Six gates, two inverters, and an 8-bit multiplexer make up the rate compare selector and gating circuit. Multiplexer U30 selectively passes rate compare (RCOM) signals and a receive teletype orderwire (RTTYOW) signal to the stuff request line as required for 96- or 48-channel operation. Four transmit frame count (TFCT01, 02, 04, 08) binary signals control U30. Multiplexer U30 monitors RCOM1 through RCOM4, RCOM7, and RCOM8 inputs directly; it monitors RCOM5, RCOM6, and RTTYOW inputs from gating circuits. Two AND gates (U25 and U18) pass RCOM5 and RCOM6 signals while 96 CHE is high during 96-channel operation. Input frame count timing is such that U30 sequentially outputs RCOM1 through RCOM8 during frames 0 through 7, and then stops in response to a TFCT08 inhibit high. A 48 CHE high during 48-channel operation lets another AND gate (U25) pass an RTTYOW signal to U30. The multiplexer selects RTTYOW for output during frame 5, the last (6th) frame in 48-channel operation. At the same time, a 96 CHE low inhibits AND gates U25 and U18 so that multiplexer U30 can only select RCOM1 through RCOM4 during frames 0 through 3 of a major frame. The multiplexer's selected signals are inverted through output OR gate U23 to stuff request storage flip-flop U16. Additionally, OR gate U23 inverts a gated RTTYOW signal during frame 11, the last (12th) frame of a major frame in 96-channel operation. A fourth AND gate (U23) passes the RTTYOW signal to U23 in response to an active transmit frame count 11 (TFC11—) low.

(2) AND gate U29 blocks stuff request levels into flip-flop U16 in response to TCLK— and transmit stuff request strobe (TSREST) inputs during bit 17 time of minor frame 2 of each frame. The entered level stays in the flip-flop through bit 16 time of minor frame 2 in the next frame. The flip-flop's stuff and no stuff outputs control selection of TSCODE and TSCODE— patterns for insertion in SG data. A stuff high selects TSCODE (11-bit A or B frame synchronization and stuff pattern) when a stuff code is to be transmitted. In turn, a no stuff high selects TSCODE— for insertion into the SG when a no stuff code is to be transmitted. In either case, the applicable pattern's bits are sequentially inserted at bit 17 times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19 of a frame. The A pattern is inserted in the above minor frames of the last (12th or 6th) frame in 96- or 84-channel operation. The B pattern is inserted in the above minor frames of all other frames. Additionally, when the stuff line is low, the TDLTTY signal applied to the TC (M) and DDOW encoder cards enable a stuff operation to be accomplished within the multiplexer section.

f. Data Rate Selection Circuits. These circuits provide for switch selection of a high (96-channel) or low (48-channel) data sampling rate. Placing DATA RATE switch S1 to HI applies ground to inverter U24-10 and +5 v to inverter U35-6 for 96 CHE high and 48 CHE low outputs, respectively. Placing S1 to LOW reverses the inverters' outputs to 96 CHE low and 48 CHE high. A 96 CHE high selects a 4915.2 kbps data sampling rate; a 48 CHE high selects a 2457.6 kbps data sampling rate. The two outputs also enable and inhibit various on-card and off-card circuits for 96- and 48-channel operation.

g. Diagnostic Detector Circuits.

(1) The 576 KHZ 1 activity monitor, a one-shot, monitors the 576 KHZ 1 square wave produced by divider U21,U28. Each signal positive transition triggers one-shot U16 into a normal duty cycle. Successive positive transitions keep U16 retriggered and its output high. However, when the transitions do not occur regularly, U16 times out and its output goes low. The low goes high through gate U18-8, creating the transmit diagnostic enable priority 4 (TDEP4) signal to TC (M) card 21A5. The TC (M) card returns a TDAP24— low that lights MO/C card diagnostic indicator DS1. The TC (M) card also produces a transmit diagnostic fault (TDFALT) output that activates alarm and clear circuits on AD card 21A1. The overall response to an MO/C card TDEP4 output is described in paragraph 2-15*f*(1).

(2) The stuff request activity monitor consists of flip-flop U17, one-shot U19, and gates U23 and U25.

One-shot U19 holds its output high provided flip-flop U17 retriggers it each time a stuff request occurs (high at its J-K inputs). Gate U25 clocks U17 set by gating TCLK— pulses when coinciding TFCT04 and TFCT08 lows enable a conditioning high from gate U23. When stuff requests do not occur at a normal rate, one-shot U19 times out and the TDEP4 output goes high.

h. Power On Circuits. The power on circuits have an RC network that switches transistor Q1 on and Q2 off when equipment power is turned on. Power turn-on applies a VR1 regulated dc voltage to the RC network, and its capacitor charges rapidly while holding Q1 switched on. Upon charging to the regulated dc level, a capacitor negative-side low siwtches Q1 off and Q2 on, respectively. While Q2 was switched off, its collector high inverted through inverter U27 and created the power on reset (PRS—) output. The short-duration PRS— low presets and/or initializes circuits on several cards.

2-20. Theory of Operation
(fig. FO-30

a. General. This paragraph describes the detailed operation of the circuits on MO/C card 21A4. The theory of operation is divided into the seven functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Oscillator No. 1 and divider (*b* below)
(2) Oscillator No. 2 and dividers (*c* below)
(3) Combine circuits (*d* below)
(4) Stuff request circuits (*e* below)
(5) Data rate selection circuits (*f* below)
(6) Diagnostic detector circuits (*g* below)
(7) Power on circuits (*h* below)

NOTE

The sheet number references in *b* through *h* below refer to figure FO-3.

b. Oscillator No. 1 and Divider.

(1) Crystal oscillator No. 1 (Y2, sheet 4) generates the basic 9830.4 kHz frequency from which HI and LO rate timing signals are derived for multiplexer section operation. The oscillator's pin Y2-3 output goes through jumper plug P2 (sheet 3) and inverter U27-6 to clock input pin U20-12 of divider flip-flop U20. Jumper plug P2 remains permanently plugged into J1 and J2 on an operational MO/C card. (P2 has been incorporated on the card to facilitate injection of external clock signals for rate variation tolerance tests of the TDF-976/G.)

(2) Oscillator No. 1's output divider circuits consist of three inverters (U27) and flip-flop U20-10. U27-6 inverts the oscillator's 9830.4 kHz output to the flip-flop and also to inverter U29-11, which restores the basic frequency to card edge test point TP6. Flip-flop U20-10 has hardwired +5v pullup and ground J-K inputs that make it toggle in response to positive transitions at clock pin U20-12. The continuous toggling action divides the clock input by 2, providing a 49.15.2 kHz square wave at pin U20-10. U27-12 and U27-10 invert the output of U20-10 to identical transmit master clock (TMASCLK) and digital data clock (DDCLK) outputs, respectively. TC (M) card 21A5 selects TMASCLK for HI rate assembling (multiplexing) of various data into the SG message format for 96-channel operation or divides it by 2 for 48-channel operation. DDOW encoder card 21A3 uses DDCLK to control processing of TTY data through its input rate buffer.

c. Oscillator No. 2 and Dividers.

(1) Crystal oscillator No. 2 (Y1, sheet 4) generates a 4608 kHz output that goes through backplane jumper MOCT03 and inverter U27-8 (sheet 3) to inverter U35-8 and to counter U21 (sheet 4). Inverter U35-8 provides the 4608 kHz CHAN output to the DGP cards, where it is used to create extracted 576 kHz clocks that are synchonized with the incoming group data.

(2) Binary counter U21 (sheet 4) has all of its input pins, except clock pin U21-2, hardwired to +5v pullup resistors and therefore operates continuously. Incrementing at a 4608 kHz clock rate, the counter produces a 576 kHz square wave at its 2^3 output pin U21-12. This output inverts through U28-6 and U28-8 to identical 576 KHZ 1 and 576 KHZ 2 outputs, respectively. The 576 KHZ 2 signal times the processing of activity patterns and dummy patterns by the DGP cards. The 576 KHZ 1 signal controls operation of the activity pattern generator on GTM card 21A2. The 576 KHZ 1 signal also is monitored by an activity monitor one-shot (*g*(1) below) and increments a divide-by-45 circuit.

(3) A divide-by-45 circuit progressively divides its 576 KHZ 1 input to a 12.8 kpps output. Up binary counter U15 (sheet 4), flip-flops U20-6 and U16-9, gates U18-11 and U22-12, and inverter U24-2 make up the circuit. Hardwired +5v pullup highs at the MR, CET, and CEP pins of counter U15 and at the S and R pins of flip-flops U20-6 and U16-9 let the divide-by-45 circuit operate continuously. The circuit counts 45 and presets itself repeatedly to produce the 12.8 kpps output. This output increments dual divider U26 ((4) below). The circuit sequences from each preset state through one 45-count sequence as follows:

(*a*) U15 counts 1 through 15 (0000 to 1110), and then puts its pins U15-15 TC output high during count 16 (1111).

(*b*) The TC high, applied directly to count 16 flip-flop's J pin U20-2 and inverted by U27-2 to K pin U20-3, lets the next 576 KHZ 1 positive transition toggle the flip-flop set. The resulting pin U20-6 high conditions gate U18-11.

(*c*) U15's second count 1 puts TC low-high to the

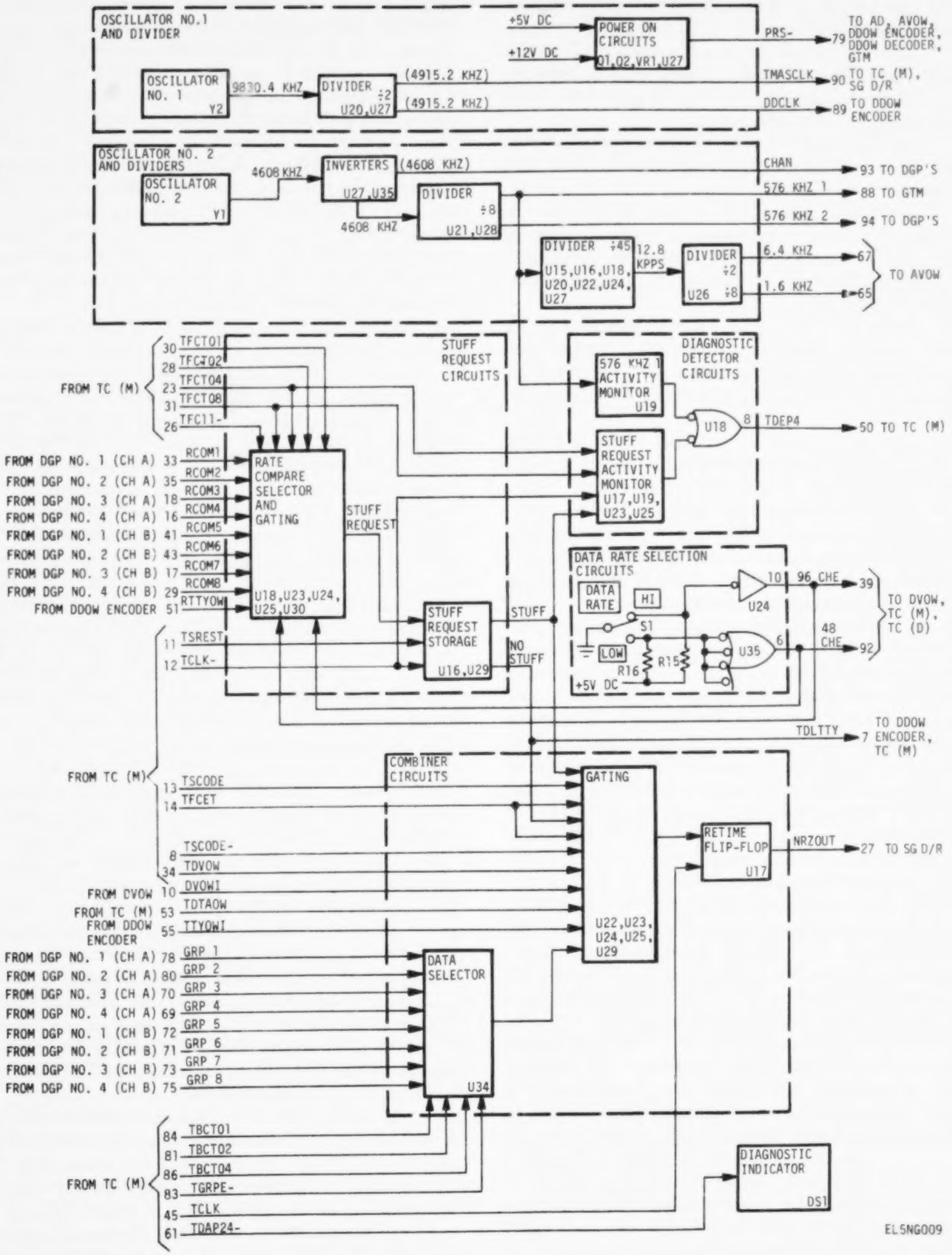

OSCILLATOR NO.1 AND DIVIDER
+5V DC
+12V DC
POWER ON CIRCUITS
Q1,Q2,VR1,U27
PRS-
79
TO AD, AVOW, DDOW ENCODER, DDOW DECODER, GTM
OSCILLATOR NO. 1
Y2
9830.4 KHZ
DIVIDER ÷2
U20,U27
(4915.2 KHZ)
TMASCLK
90
TO TC (M), SG D/R
(4915.2 KHZ)
DDCLK
89
TO DDOW ENCODER
OSCILLATOR NO. 2 AND DIVIDERS
OSCILLATOR NO. 2
Y1
4608 KHZ
INVERTERS
U27,U35
(4608 KHZ)
CHAN
93 TO DGP'S
DIVIDER ÷8
U21,U28
4608 KHZ
576 KHZ 1
88 TO GTM
576 KHZ 2
94 TO DGP'S
DIVIDER ÷45
U15,U16,U18, U20,U22,U24, U27
12.8 KPPS
DIVIDER ÷2
U26 ÷8
6.4 KHZ
67
1.6 KHZ
65
TO AVOW
FROM TC (M)
30 TFCT01
28 TFCT02
23 TFCT04
31 TFCT08
26 TFC11-
STUFF REQUEST CIRCUITS
DIAGNOSTIC DETECTOR CIRCUITS
576 KHZ 1 ACTIVITY MONITOR
U19
U18
8
TDEP4
50 TO TC (M)
STUFF REQUEST ACTIVITY MONITOR U17,U19, U23,U25
FROM DGP NO. 1 (CH A) 33 RCOM1
FROM DGP NO. 2 (CH A) 35 RCOM2
FROM DGP NO. 3 (CH A) 18 RCOM3
FROM DGP NO. 4 (CH A) 16 RCOM4
FROM DGP NO. 1 (CH B) 41 RCOM5
FROM DGP NO. 2 (CH B) 43 RCOM6
FROM DGP NO. 3 (CH B) 17 RCOM7
FROM DGP NO. 4 (CH B) 29 RCOM8
FROM DDOW ENCODER 51 RTTYOW
RATE COMPARE SELECTOR AND GATING
U18,U23,U24, U25,U30
STUFF REQUEST
DATA RATE SELECTION CIRCUITS
DATA RATE
HI
S1
LOW
R16
R15
+5V DC
U24
10
96 CHE
39
U35
6
48 CHE
92
TO DVOW, TC (M), TC (D)
11 TSREST
12 TCLK-
STUFF REQUEST STORAGE
U16,U29
STUFF
NO STUFF
TDLTTY
7 TO DDOW ENCODER, TC (M)
FROM TC (M)
COMBINER CIRCUITS
13 TSCODE
14 TFCET
8 TSCODE-
34 TDVOW
FROM DVOW 10 DVOWI
FROM TC (M) 53 TDTAOW
FROM DDOW ENCODER 55 TTYOWI
GATING
U22,U23, U24,U25, U29
RETIME FLIP-FLOP
U17
NRZOUT
27 TO SG D/R
FROM DGP NO. 1 (CH A) 78 GRP 1
FROM DGP NO. 2 (CH A) 80 GRP 2
FROM DGP NO. 3 (CH A) 70 GRP 3
FROM DGP NO. 4 (CH A) 69 GRP 4
FROM DGP NO. 1 (CH B) 72 GRP 5
FROM DGP NO. 2 (CH B) 71 GRP 6
FROM DGP NO. 3 (CH B) 73 GRP 7
FROM DGP NO. 4 (CH B) 75 GRP 8
DATA SELECTOR
U34
FROM TC (M)
84 TBCT01
81 TBCT02
86 TBCT04
83 TGRPE-
45 TCLK
61 TDAP24-
DIAGNOSTIC INDICATOR
DS1
EL5NG009

Figure 2-9. MO/C card 21A4, block diagram.

J-K pins of U20 so that it cannot toggle during the second series of 15 counts.

(*d*) U15 counts to 16 and puts its TC output high again. This (second) TC high enables gate pin U18-11 low to count 32 flip-flop's K pin U16-13 and also puts U20's J-K pins high-low.

(*e*) The next 576 KHZ 1 positive transition toggles flip-flops U20 and U16 reset. A pin U16-9 high conditions gate U22-12.

(*f*) U15's third count 1 puts TC low-high to U20's J-K pins so that it cannot be toggled set during the next 13 counts. The pin U20-6 low holds gate U18-11 inhibited and U16's K pin high so that it cannot be toggled set.

(*g*) U15 counts to 13 (1100) and puts its 2^2 (pin U15-12) output high; its 2^3 (pin U15-11) output is already high at that time. These two highs and the count 32 high from U16-9 enable gate pin U22-12 count 45 low.

(*h*) The count 45 low conditions counter PE pin U15-9 and also goes high through U24-2 to U16's J pin. The next 576 KHZ 1 positive transition toggles U16 set and also presets U15 to count 1 (0000).

(*i*) Pin U16-9 is now low and inhibits gate U22-15 so that it cannot be enabled until counter U15 cycles through another 45-count (1-16, 1-16, 1-13) sequence as described in (*a*) through (*h*) above.

(4) Dual divider U26, a binary counter, generates 1.6 KHZ and 6.4 KHZ square waves to AVOW card 21A10. The AVOW card uses 1.6 KHZ to generate a 1600 Hz tone ring signal; it uses 6.4 KHZ to control timing of cable fault circuits. Each 12.8 kpps pulse from inverter U24-2 ((2 above) lets a 576 KHZ 1 positive transition increment counter U26. The counter divides its 12.8 kpps count enable trickle input by 2 for a 6.4 KHZ squre wave output at 2^0 pin U26-14. The counter also divides the CET input by 8 for a 1.6 KHZ square wave output at 2^2 pin U16-12.

d. Combiner Circuits (sheet 3).

(1) Four AND gates (U29-6, U25-11, U22-6, U22-8), two inverters (U24-6, U24-12), and two OR gates (U23-12, U29-3) make up the gating circuit that assembles various O/H and group data onto a common line to retime flip-flop U17-7 ((3 below). Gate timing is such that each O/H bit is inserted (gated) into its assigned O/H (bit 17) location of the SG message format (figs. 2-3 and 2-4). Between O/H bits, data selector U34 sequentially multiplexes data bits for four or eight groups through gate U23-12 for insertion in their assigned bit locations of the SG message format.

(*a*) Gate U29-6 monitors a digital voice orderwire input (DVOWI) from DVOW card 21A11 and a transmit digital voice orderwire clock (TDVOW) from TC (M) card 21A5. TDVOW goes high and lets the gate invert a DVOWI bit only during bit 17 times of minor frames 0, 5, 10, and 15 for insertion of four DVOW bits per frame in 96-channel operation. Additionally, TDVOW goes high during bit 17 times of minor frames 1, 6, 11, and 16 for insertion of eight DVOW bits per frame in 48-channel operation. The inverted DVOWI output at U29-6 is restored through inverter U24-6 and inverted again through gate U23-12.

(*b*) Gate 25-11 monitors a teletype orderwire input (TTYOWI) from DDOW encoder card 21A3 and a transmit digital data orderwire (TDTAOW) from TC (M) card 21A5. TDTAOW goes high only during bit 17 time of minor frame 2 in frame 0 in a major frame. Each TDTAOW high lets gate U25-11 invert one TDVOW bit. Inverter U24-12 restores the gated bit for inversion through gate U23-12.

(*c*) Gates U22-8 and U22-6 separately monitor one or two complementary transmit stuff code (TSCODE and TSCODE—) inputs, one of two complementary transmit delete (TDLTTY and TDLTTY—) inputs, and a common transmit frame code enable time (TFCET) input. TC (M) card 21A5 provides the TSCODE and TFCET inputs. Stuff request storage flip-flop U16-6 provides the TDLTTY (stuff and no stuff) inputs. TSCODE is an 11-bit B0 through B10 pattern (10111111001) for use in frames 0 through 10 (96-channel operation) or 0 through 4 (48-channel operation) of a major frame. TSCODE is an 11-bit A0 through A10 pattern (00001010011) for use in the last (12th or 6th) frame of a major frame. TFCET goes high only during bit 17 times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19. When TDLTTY— is high at gate pin U22-11 (stuffing required), each TFCET high lets gate U22-8 invert a TSCODE bit to gate U29-3. Conversely, when TDLTTY is high at gate pin U22-4 (no stuffing required), each TFCET high lets gate U22-6 invert a TSCODE— bit to gate U29-3. In either case, gate U29-3 restores each code bit for inversion through gate U23-12. During data bit 1 through 16 times of each minor frame, gate U23-12 also inverts group data bits applied to it by data selector U34.

(2) Data selector U34 is an 8-bit multiplexer. DGP cards 21A6 No. 1 through No. 4 provide A channel GRP 1 through GRP 4 data to the I0 through I3 data input pins of U34. In 96-channel operation, the four DGP cards also provide B channel GRP 5 through GRP 8 data to the I4 through I7 data input pins of U34. Transmit group enable (TGRPE—) and three transmit bit count (TBCT01, 02, 04) inputs from TC (M) card 21A5 control data selector U34.

(*a*) While U34 is enabled in 96-channel operation, its three select inputs repeatedly increment in binary order. These inputs sequentially select GRP 1 through GRP 8 inputs twice during each minor frame for serial output through pin U34-15 to gate U23-12.

(*b*) While U34 is enabled in 48-channel operation, TBCT04 stays low and only the TBCT01 and TBCT02 select inputs repeatedly increment in binary order. These two inputs sequentially select GRP 1 through GRP 4 inputs four times during each minor frame for serial output to gate U23-12.

(*c*) In either 96- or 48-channel operation, TGRPE— goes high during O/H bit times (bit 17 and bit 341 times). The TGRPE— high inhibits the data selector and holds its pin U34-15 output low while O/H bits are being passed through gate U23-12.

(3) Retime flip-flop U17-7 receives inverted group data and O/H bits in SG message format sequence at its J-K inputs. Positive transitions of transmit clock (TCLK) from the TC (M) card serially clock the data and O/H bits through the flip-flop. The flip-flop restores the data and O/H bits to their true logic levels at NRZOUT pin U17-7. NRZOUT goes to SG D/R card 21A9 for conversion to bipolar format and output on a transmission line.

e. Stuff Request Circuits (sheet 2).

(1) Four AND gates (U18-6, U23-9, U25-3, U25-8), two OR gates (U18-3, U23-4), two inverters (U24-4, U24-8), and an 8-bit multiplexer (30) make up the rate compare selector and gating circuit. Data inputs to the circuit include the rate compare (RCOM1 through RCOM8) signals from DGP cards 21A6 and a receive teletype orderwire (RTTYOW) signal from DDOW encoder card 21A3. Transmit frame count (TFCT01, 02, 04, 08) binary signals and the transmit frame count 11 (TFC11—) gate signal from TC (M) card 21A5 and on-card created 96 CHE and 48 CHE levels control the operation of the circuit. The rate compare selector and gating circuit scans all the RCOM and RTTYOW inputs once during every major frame to determine whether or not a stuffing operation is required on any DGP card or on the DDOW encoder card. The circuit provides scanned RCOM1 through RCOM 8 samples to stuff request storage flip-flop U16-6 ((2 below) during frames 0 through 7; it provides an RTTYOW sample during the last frame of a major frame.

(*a*) Multiplexer U30 monitors RCOM and RTTYOW signals applied directly or throught gating circuits to its data input pins. RCOM1 through RCOM8 levels appear at data inputs I0 through I7, respectively. A gated RTTYOW level appears at data input I5, but only in 48-channel operation. Incrementing TFCT01, TFCT02, and TFCT04 binary frame count at select inputs S0, S1, and S2 sequentially selects I0 through I7 (RCOM1 through RCOM8) inputs for output at pin U30-15. The samples invert through gate U23-4 to the J-K inputs of flip-flop U16-6, where each sampled level can be temporarily stored. A TFCT08 low at enable pin U30-10 lets the multiplexer operate during frames 0 through 7. TFCT08 goes high at the start of frame 8 and inhibits U30 during frames 8 through 11.

(*b*) Separate gating circuits control application of RCOM5, RCOM6, and RTTYOW inputs to U30 and also RTTYOW thorugh gate U23-4 to flip-flop U16-6. Gates U25-3 andU18-6 monitor RCOM5 and RCOM6 inputs, and a common 96 CHE input from inverter U24-10. Placing DATA RATE switch S1 to HI puts 96 CHE high and lets the two gates invert their RCOM levels. U25-3 inverts RCOM5; inverter U24-4 restores it to the multiplexer's I4 pin U30-5. U18-6 inverts RCOM6; gate U18-3 restores it to the multiplexer's I5 pin U30-6. Placing S1 to LOW puts 96 CHE low (inhibits U18-6 and U25-3) and 48 CHE high (conditions gate U25-8) for 48-channel operation. The 48 CHE high lets gate U25-8 invert RTTYOW during frame 5, the last (6th) frame of a major frame in 48-channel operation. Gate U23-9 provides the RTTYOW sample during frame 11, the last (12th) frame of a major frame in 96-channel operation. Inverter U24-8 inverts RTTYOW to gate pin U23-10. TFC11— (a low during frame 11) at gate pin U23-11 lets the gate restore its RTTYOW input; gate U23-4 inverts it to flip-flop U16-6.

(2) Gate U29-8 and flip-flop U16-6 make up the stuff request storage circuit. A transmit stuff request strobe (TSREST) high during bit 17 time of minor frame 2 in a frame lets U29-8 gate and invert one TCLK— pulse. The positive transition of TCLK at flip-flop pin U16-4 clocks the applied J-K level into the flip-flop. The clocked-in level remains in the flip-flop through bit 16 time of minor frame 2 of the next frame. Operating in this manner, flip-flop U16-6 sequentially stores (set for a no-stuff; reset for a stuff) each RCOM1 through RCOM8 and then RTTYOW sample from one frame to another. The flip-flop provides complementary pin U16-6 no stuff and pin U16-7 stuff output, respectively. The no stuff line controls TSCODE— gate U22-6 (*d*(1)(*c*) above) and routes transmit delete (TDLTTY) to DDOW encoder card 21A3 and TC (M) card 21A5. When TDLTTY is low (U16 reset), TC (M) card 21A5 or DDOW encoder card 21A3, as appropriate, will initiate a stuff action within the multiplexer section. The stuff line controls TSCODE gate U22-8 and also provides periodic highs to stuff request activity flip-flop U17-10 (*g*(2) below).

(*a*) When an active (high; stuff requested) RCOM or TTYOW input is scanned, its sample appears at a low at flip-flop U16's J-K inputs. Coinciding TSREST and TCLK— highs subsequently enable a ½-clock period duration negative pulse at gate pin U29-8. The pulse's trailing edge clocks the J-K pins low into U16-6, putting its no stuff and stuff outputs low and high, respectively. The no stuff low inhibits TSCODE— gate U22-6 (sheet 3). The stuff high lets TSCODE gate U22-8 pass the 11-bit A or B TSCODE pattern for insertion into the NRZOUT data stream. The applicable pattern bits are serially inserted at O/H bit times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19 in the same frame. The flip-flop's pin

U16-7 stuff high also lets a gated clock positive transition set stuff request activity monitor flip-flop U17-10.

(*b*) When an inactive (low; no stuff requested) RCOM or RTTYOW input is scanned, its sample appears as a high at flip-flop U16-6's J-K's inputs. The trailing edge of the next gated clock pulse (during bit 17 time of minor frame 2) sets the flip-flop. In this no-stuffing-required condition, a pin U16-7 stuff low lets a gated clock positive transition reset flip-flop U17-10. The stuff low also inhibits TSCODES gate U22-8. However, the pin U16-6 no stuff high lets TSCODE— gate U22-6 pass the 11-bit A or B TSCODE— pattern. The applicable pattern bits are inserted in the O/H bit time slots ((*a*) above).

f. Data Rate Selection Circuits. (sheet 2). These circuits consist of DATA RATE switch S1, inverters U24-10 and U35-6, and +5v pullup resistors R15 and R16. The circuits provide a means for manually selecting a high (4915.2 kbps) or low (2457.6 kbps) data sampling rate for 96- or 48-channel operation, respectively.

(1) Placing switch S1 to HI grounds pin S1-1, sending a low through backplane jumper MOCT02 to inverter U24-10; the inverter puts out a 96 CHE high. At the same time, R16 puts pin S1-3's output line through backplane jumper MOCT01 to inverter U35-6; the inverter puts out a 48 CHE low. On card, the 48 CHE low inhibits RTTYOW monitor gate U25-8 (*e*(1)(*b*) above) while the 96 CHE high conditions RCOM5 and RCOM6 monitor gates U25-3 and U18-6. Both outputs also go off card to TC (M), TC (D), and DVOW cards, which must operate at the same rate as the MO/C card.

(2) Placing switch S1 to LOW grounds in pin S1-3 and lets R15 put pin S1-1 high. Placing S1 to LOW also reverses inverter U24-10 and U35-6 output polarities. Now a 48 CHE high conditions RTTYOW monitor gate U25-8 while a 96 CHE low inhibits the RCOM5 and RCOM6 monitor gates U25-3 and U18-6. These two gates are not required in 48-channel operation since only RCOM1 through RCOM4 signals must be scanned. Conversely, gate U25-8 must operate so that RTTYOW can be scanned during frame 5, the last (6th) frame of a major frame in 48-channel operation.

g. Diagnostic Detector Circuits. Two detector circuits monitor the card's 576 KHZ 1 clock and stuff request activity. Each detector has a one-shot (U19, sheet 2) that is triggered by positive transitions of the signal it is monitoring. The one-shots provide high to gate U18-8 while transitions occur regularly at their trigger inputs. When either one-shot's input triggers stop, the one-shot times out, and its output goes low to gate U18-8 and puts TDEP4 high to TC (M) card 21A5. The TC (M) card's diagnostic detector returns a TDAP24— low, which lights MO/C card's diagnostic indicator DS1 (sheet 1). The TC (M) card also produces a TDFALT output that activates alarm and clear circuits on AD card 21A1. The interconnection and relationship of the MO/C, TC (M), and AD cards' diagnostic circuits are shown in figure FO-2. The overall response to a TDEP4 output from the MO/C card is described in paragraph 2-15*f*(1).

(1) One-shot U19-5 monitors 576 KHZ 1 from U28-6 (*c*(2) above). Recurring 576 KHZ 1 positive transitions keep the one-shot retriggered and its pin U19-5 output high.

(2) One-shot U19-13 holds its pin output high provided flip-flop U17-10 retriggers it with a positive transition each time a stuff request occurs (stuff high J-K input from stuff request storage flip-flop U16-6). Gate U25-6 clocks flip-flop U17-10 set by gating TCLK— pulses when coinciding TFCT04 and TFCT08 lows enable a conditioning high from gate U23-7. The U17-10 clock/set action occurs at the start of a frame that follows the frame during which a stuff request was generated.

h. Power On Circuits. (sheet 4). The power on circuits consist of transistors Q1 and Q2, voltage regulator diode VR1, inverter U27-4, and related RC components. The circuit generates a short-duration power on reset (PRS—) pulse upon equipment power turn-on. The PRS pulse presets and/or initializes various circuits on AD, AVOW, GTM, DDOW encoder, and DDOW decoder cards.

(1) Power turn-on raises +12 v at zener current limiting resistor R27. VR1 regulates the R27, R29 junction voltage at +6.2 v. Application of this voltage through R29 rapidly charges capacitor C14. As C14 charges, its initially high ground side differentiates to ground (goes low) through resistor R30. C14's initial high switches Q1 on, putting its collector low to the base of Q2, and holds Q2 switched off. A Q2 collector +5 v pullup (R32) high goes low through inverter U27-4 (leading edge of PRS— pulse).

(2) C14's differentiation to ground through R30 switches Q1 off. A Q1 collector +5 v pullup (R28) high switches Q2 on and puts its collector low. This low switches inverter U27-4's output high (trailing edge of PRS— pulse). R33 couples the PRS— high back to the base of Q2 and holds Q2 switched on until equipment power is switched off or interrupted.

Section VI. TIMING AND CONTROL (TC) CARD 21A5

2-21. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on a TC card. There are two TC cards (21A5) in the TD-976/G. The cards, which are designated TC (M) and TC (D), are used in the TD-976/G's multiplexer section and demultiplexer section, respectively. A TC (M) card generates timing and gating signals that control multiplexing operations for assembling group data, digital voice, digital teletype, and stuff code information contained in the SG message format (figs. 2-3 and 2-4). A TC (D) card similarly generates timing and gating signals that control demultiplexing operations for extracting group data, digital voice, digital teletype, and destuff code information contained in the received SG message format. The block diagram discussion in paragraph 2-22 is based on the TC card block diagram in figure FO-4. The theory of operation in paragraph 2-23 is based on the TC card schematic diagram in figure FO-5.

2-22. Block Diagram Discussion

(fig. FO-4)

a. General. TC (M) and TC (D) cards operate similarly, except that the counters on the TC (M) card are free running, while those on the TC (D) card are controlled by frame and major frame sync signals from FS card 21A7. These sync signals inhibit bit, minor frame, and frame counters until frame and major frame sync patterns are decoded from incoming SG data. The three counters are then allowed to start, in turn, and operate in synchronization with the incoming SG data. Because of the functional similarities between the two cards, only the TC (M) card functions are discussed in *b* through *h* below, and signal mnemonics preceded by T (transmit) in figure FO-4 are used. Functional differences between TC (M) and TC (D) cards are discussed in *i* below, using the signal mnemonics preceded by R (receive) in figure FO-4. The block diagram discussion is divided into seven functional circuit descriptions as follows:

(1) The clock selection circuits (*b* below) select the appropriate transmit clock for timing 96- or 48-channel data multiplexing operations. The selected clock is distributed to on-card counters and to associated cards for control of data processing operations.

(2) The bit counter and decoder (*c* below) sequentially creates the 17 time slots for insertion of data and overhead (O/H) bits into a minor frame. The counter operates at a 4915.2 or 2457.6 kHz rate for 96- or 48-channel operation, respectively.

(3) The minor frame counter and decoder (*d* below) generates and decodes minor frame count signals. The frame count decodes selectively control timing decode gates whose outputs determine insertion times for various O/H data.

(4) The frame counter and decoder (*e* below) generates and decodes frame count signals. The frame count decodes control formatting of O/H stuff patterns and restarts the card's counter chain for each new major frame.

(5) The stuff/destuff circuits (*f* below) generate 11-bit pattern, timing, and gating signals for stuffing and destuffing operations performed in multiplexer and demultiplexer sections.

(6) The timing decode gates (*g* below) decode the bit time slots for insertion or extraction of digital voice, stuff/destuff code, and digital teletype O/H data.

(7) The diagnostic detector (*h* below) lights an on-card diagnostic indicator and a front panel EQUIP ALARM indicator when the card's counter chain is not operating properly.

b. Clock Selection Circuits. MO/C card 21A4 supplies a 4915.2 kHz transmit master clock (TMASCLK) signal to clock traffic detector U22, rate select gates U1, U9, and divided-by-2 flip-flop U8. The clock traffic detector, a one-shot, monitors TMASCLK whose positive transitions renew its duty cycle. While kept retriggered, U22 lets a rate select gate pass the selected transmit clock (TCLK) (either 4915.2 or 2457.6 kHz). If the TMASCLK transitions stop, U22 times out and inhibits the rate select gate. A 96-channel enable (96 CHE) high lets the rate select gates pass the 4915.2 kHz TMASCLK as complementary TCLK and TCLK—— signals for 96-channel operation. A 48 CHE high lets flip-flop U8 operate and divide TMASCLK by 2 to provide complementary 2457.6 kHz outputs for 48-channel operation. In either case, the selected TCLK establishes the bit insertion rate for formatting a transmit SG data message.

c. Bit Counter and Decoder.

(1) Data bit counter U10 sequentially generates 16 binary counts representing the 16 group data bit times in each minor frame. The binary count outputs control several bit count decode gates and a bit count decoder. The selected TCLK from the rate select gates increments counter U10. The terminal count output of U10, which goes high only at count 16, lets the next TCLK set bit 17 flip-flop U11. The bit 17 high (representing the O/H bit time in each minor frame) inverts through O/H time gate U19-7 to preset counter U10 back to zero and let a clock reset flip-flop U11. These actions initialize U10 and U11 for another bit 1 through 16 and then bit 17 count sequence.

(2) The bit count gates decode various bit times for control of timing decode gates, a stuff/destuff decoder, and the bit count decoder. A TBCT04 control gate determines the TCHAN decode range of the bit

count decoder in response to a 48 CHE signal. A 48 CHE low lets TBCT04 pass through for addressing TCHAN1 through TCHAN8 outputs for 96-channel operation. A 48 CHE high inhibits the gate and holds TBCT04 low, which limits the bit count decoder range to TCHAN1 through TCHAN4 for 48-channel operation. A bit 9 gate decodes bit 9 time highs to DVOW smooth clock gates. These highs are used to evenly space the eight-per-frame DVOW bit sampling times during 48-channel operation. A stuff/destuff decoder enable gate decodes bit times during which a stuffing operation may be performed. This gate provides an enable low to stuff/destuff decoder U25 only during minor frame 0 bit times 1 through 8 for 96-channel operation or bit times 1 through 4 for 48-channel operation.

(3) The bit count decoder produces transmit channel clock group (TCHAN) outputs to the four DGP cards. Each TCHAN high denotes a specific group's turn to supply a data bit for input to the SG. Addressing inputs TBCT01 and TBCT02 from bit counter U10, TBCT04 from the bit count decode gates, and TGRPE— from U20-6 control the bit count decoder. These addressing inputs sequentially produce TCHAN1 through TCHAN8 outputs twice during each minor frame for 96-channel operation. The inputs sequentially produce TCHAN1 through TCHAN4 four times during each minor frame for 48-channel operation. TGRPE— goes high during O/H bit times (each bit 17 and bit 341 time), causing the bit count decoder to put all TCHAN outputs low during these bit times.

d. Minor Frame Counter and Decoder.

(1) Minor frame counter U4, U11 is enabled at the end of each minor frame by the bit 17 output of the bit 17 flip-flop. The next TCLK (first bit time of next minor frame) increments the minor frame counter one count. Thus, the minor frame counter counts 20 minor frames, generating minor frame 0 through 19 counts in binary form for control of the minor frame count decoder and the stuff code generator. The minor frame counter is preset back to zero at the start of each frame by the action of bit 341 flip-flop U2 ((3 below).

(2) The minor frame count decoder selectively decodes 14 minor frame counts in response to binary frame count inputs from counter U4, U11.

(3) Coinciding bit 17 and minor frame 19 signals enable bit 341 flip-flop U2 so that the next TCLK will set it, producing bit 341 (end-of-frame bit), which denotes end of frame. The complementary bit 341 outputs preset the minor frame counter directly and preset the data bit counter and its bit 17 flip-flop through O/H time gate U19-7. One of the bit 341 outputs is also applied to the frame counter and decoder (*e* below).

e. Frame Counter and Decoder.

(1) Frame counter U15 is enabled at the end of each frame by bit 341. The next TCLK (first bit time of next frame) increments the frame counter one count. Thus, U15 generates frame counts 0 through 11 (96-channel operation) or 0 through 5 (48-channel operation) in binary format on four output lines. The frame counter is preset to zero after the last frame of each major frame ends by coincidence of a bit 341 and TLFOMF. The counter's four binary form frame count outputs control on-card decoder circuits and gates. The outputs also go to MO/C card 21A4, where they are used in controlling the stuff request circuits.

(2) Last frame of major frame gates U16 decode TLFOMF highs. In 96-channel operation, TLFOMF is decoded during frame count 11 (12th frame). In 48-channel operation, 48 CHE is active and causes TLFOMF to be decoded during frame count 5 (sixth frame). In either case, the TLFOMF output forces the stuff code generator to change its 11-bit TSCODE output to an A pattern during the last frame of each major frame. Coincidence of a bit 341 and TLFOMF (last bit time in a major frame) presets the frame counter back to zero.

f. Stuff/Destuff Circuits.

(1) The stuff code generator, whose inputs consist of minor frame counts, hardwired grounds, and +5 v pullups, continually produces a transmit stuff code (TSCODE) and its complement (TSCODE—). TSCODE—— will be selected and inserted in 11 designated O/H bit positions of each frame in the SG by MO/C card 21A4 unless a stuffing action is to be transmitted, at which time TSCODE will be selected and inserted. The 11 designated O/H bit positions are those in minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19. Additionally, TSCODE (and its complement TSCODE—) is in one of two forms. Normally, it will be in the form of the B pattern (para 2-6*e*(3)) (TSCODE—— is 01000000110). However, during the last frame of each major frame, TLFOMF causes the stuff code generator to produce the A pattern (TSCODE— is 11110101100). Also, frame and major frame synchronization information is contained within the last 8 bits of TSCODE and TSCODE—.

(2) Stuff/destuff decoder U25 generates a transmit channel clock delete group (TCHN) output when enabled by a TDLTTY low (stuff action to be accomplished). U25 is enabled only during those bit times when a stuff operation may be performed on a DGP card (bit times 1 through 8 of minor frame 0 for 96-channel operation or bit times 1 through 4 of minor frame 0 for 48-channel operation). The frame counts direct which TCHN line will be active (low) to accomplish the stuff action.

(3) The stuff request strobe gate is enabled at bit 17 time of each minor frame 2 and produces the stuff request strobe (TSREST). TSREST is applied to MO/C card 21A4, causing its stuff request circuits to sample the rate compare for either the teletype input or a des-

ignated group input. RSREST— on a TC (D) card is applied to FS card 21A7 to reset its destuff detection circuits.

g. Timing Decode Gates.

(1) The DVOW time decoder generates transmit digital voice orderwire clock (TDVOW) highs. TDVOW highs coincide with SG message format O/H bit times assigned for digital voice orderwire (DVOW) insertion (figs. 2-3 and 2-4). In 96-channel operation, the decoder is enabled during the O/H (bit 17) times of minor frames 0, 5, 10, and 15. In 48-channel operation, 48 CHE allows the decoder to be enabled also during bit 17 times of minor frames 1, 6, 11, and 16.

(2) The DVOW smooth clock gates generate digital voice orderwire smooth clock (TDVOWC—) lows. These gates put TDVOWC— low during bit 17 times of minor frames 0, 5, 10, and 15 and bit 9 times of minor frames 3, 8, 13, and 18. The lows evenly space the eight-per-frame DVOW bit sampling times during 48-channel operation.

(3) Frame code enable time gate U13 generates TFCET highs during those O/H bit times assigned for insertion of the 11-bit frame synchronization and stuff pattern. U13 is enabled during bit 17 times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19.

(4) The DDOW time decode gates generate a transmit digital data orderwire (TDTAOW) high only at bit 17 time of minor frame 2 in frame 0 of each major frame. Four coinciding lows from frame counter U15 (frame 0) and TSREST— (bit 17 time of minor frame 2) enable the DDOW time decode gates.

h. Diagnostic Detector. The diagnostic detector monitors the TC card counter chain's TLFCMF and bit 341 detect outputs. When these outputs do not occur regularly, the detector lights diagnostic indicators on the card and on the front panel and also sounds an audible alarm. The TC (M) and TC (D) cards' diagnostic detector functions are described in paragraph 2-15*f*.

i. TC (D) Card Operational Differences. The principal difference between the TC (M) and TC (D) cards is the operation of their counter chains. The TC (M) card's three counters (bit, minor frame, and frame) are free running. The TC (D) card's counters operate only after FS card 21A7 decodes frame and major frame sync patterns and removes counter inhibit levels.

(1) Initially or after loss of frame sync, the FS card holds data bit and minor frame counters reset and the bit 17 and bit 341 flip-flops cleared with an RFSYNC— low. Upon detecting an incoming frame sync pattern, the FS card puts RFSYNC— high so that the two counters and two flip-flops can operate.

(2) Initially or after loss of major frame sync, the FS card holds the frame counter reset with an RMSYNC— low. Upon detecting an incoming major frame sync pattern, the FS card puts RMSYNC— high so that the frame counter can operate.

(3) A 48 CHE high releases divide-by-2 flip-flop U8 for 48-channel operation as on the TC (M) card. Additionally, the receive phase forcing (RPHF) low insures that operation of the flip-flop is synchronized with true data bit times of the incoming SG.

2-23. Theory of Operation

(fig. FO-5)

a. General. This paragraph describes the detailed operation of the circuits on TC (M) card 21A5. Operational differences between circuits on the TC (M) card and corresponding circuits on a TC (D) card are detailed in *i* below. The TC (M) card theory of operation is divided into the seven functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Clock selection circuits (*b* below)
(2) Bit counter and decoder (*c* below)
(3) Minor frame counter and decoder (*d* below)
(4) Frame counter and decoder (*e* below)
(5) Stuff/destuff circuits (*f* below)
(6) Timing decode gates (*g* below)
(7) Diagnostic detector (*h* below)

NOTE

The sheet number references in *b* through *h* below refer to figure FO-5.

b. Clock Selection Circuits (sheet 2). Clock input inverter U24-2, clock traffic detector U22-5, divide-by-2 flip-flop U8-9, and three rate select gates (U9-6, U1-6, U1-8) make up the clock selection circuits. The circuits select and provide the appropriate 96-channel (4915.2 kHz) or 48-channel (2457.6 kHz) transmit clock (TCLK) to on-card counters and to MO/C card 21A4, all DGP cards 21A6, and DVOW card 21A11. The clock's complement is used by MO/C card 21A4 and DDOW encoder card 21A8.

(1) MO/C card 21A4 supplies a transmit master clock (TMASCLK) and a 96-channel enable (96 CHE) or 48-channel enable (48 CHE) signal to the clock selection circuits. Inverter U24-2 inverts the received 4915.2 kHz TMASCLK to flip-flop clock pin U8-12 and to rate select gate U9-6. Clock traffic detector one-shot U22-5 monitors the received TMASCLK. The one-shot conditions final rate select gate U1-8 with a TNOCLK— high (card pins 12 to 19 backplane jumper) only while TMASCLK cycles occur regularly. Successive clock positive transitions keep the one-shot retriggered and its pin U22-5 TNOCLK— output high.

(2) During 96-channel operation, a 96 CHE high at pin U9-4 lets the gate pass and restore the 4915.2 kHz clock at pin U9-6. Gate U1-6 inverts the clock again to a transmit clock (TCLK—) output. TCLK— is distributed to various other circuit cards, where it is used to time data processing functions. Gate U1-8 restores TCLK— to TCLK, which goes directly to on-card bit, minor frame, and frame counters and to var-

ious other circuit cards, where it is used to time data processing functions.

(3) During 48-channel operation, a 96 CHE low inhibits passage of the received 4915.2 kHz TMASCLK through rate select gate U9-6. A 48 CHE high applied to pin U8-15 lets divide-by-2 flip-flop U8-9 operate. With a pullup high at J pin U8-14 and a ground at K pin U8-13, the flip-flop toggles in response to each TMASCLK— positive transition at its clock pin U8-12. The toggling action divides the 4915.2 kHz TMASCLK— by 2 for a pin U8-9 2457.6 kHz clock output. This output inverts to TCLK— at gate pin U1-6, and then restores to TCLK at gate pin U1-8.

c. *Bit Counter and Decoder.*

(1) Data bit counter U10 (sheet 3) is clocked at the TCLK rate (4915.2 kHz or 2457.6 kHz) and sequentially generates 4-bit binary count outputs 0000 through 1111. The 16 bit counts correspond with the 16 data bit positions in each minor frame. The counter's 2^0 (pin U10-14) and 2^1 (pin U10-13) outputs go directly to bit counter decoder U26 and bit 9 decode gate U19-12 ((3)(*c*) below). The counter's 2^2 (pin U10-12) output goes directly to bit 9 decode gate U19-12 and also inverts through U20-4 to TBCT04 control gate U19-4 ((3)(*a*) below). The counter's 2^3 (pin U10-11) output inverts through U20-2 to bit 9 decode gate U19-12 and to stuff/destuff decoder enable gate U21-6 ((3)(*b*) below). The counter's terminal count (pin U10-15) output, which goes high for one clock period at count 16, lets the next TCLK positive transition toggle bit 17 flip-flop U11-6 set. Also, counter U10 cycles back to a count of 0000 at bit 17 time. Each bit 17 high from U11-6 or bit 341 high from U2-6 (*d*(2) below) going low through U19-7 maintains counter U10 preset to 0000.

(2) Bit 17 flip-flop U11-6 produces complementary count 17 (bit 17) outputs during the bit period that immediately follows counter U10's binary count 1111 (16). The flip-flop's pin U11-6 bit 17 high lets the next TCLK positive transition increment minor frame counter U4 (*d*(1) below). The bit 17 high also goes low through U19-7 and holds bit counter U10 preset to 0000 during data bit 1 time. Flip-flop U11-6 is reset by the next TCLK after bit 17 because of the lows now applied to its J-K input pins (U10-15 is low and U19-7 is low).

(3) Three bit count gates decode various bit times for control of timing decode gates, a stuff/destuff decoder, and the bit count decoder.

(*a*) TBCT04 control gate U19-4 (sheet 3) controls the decode range of bit count decoder U26 in response to the 48 CHE input. U19-4 determines how many counts U26 decodes and the number of times it repeats them for each minor frame. In 96-channel operation, 48 CHE is low and enables U19-4 so that it restores bit counter U10's inverted 2^2 count from inverter U20-4 to decoder pin U26-1. This 2^2 (TBCT04) count and the 2^0 and 2^1 (TBCT01 and TBCT02) count inputs from U10 sequentially address U26, allowing it to decode counts 1 through 8 twice in each minor frame. In 48-channel operation, 48 CHE is high and inhibits U19-4, holding its TBCT04 output low. With TBCT04 held low, counter U10's 2^0 and 2^1 outputs sequentially address U26, allowing it to decode counts 1 through 4 times in each minor frame.

(*b*) Gates U9-8 (sheet 3) and U21-6 (sheet 4) make up the stuff/destuff decoder enable gate. U21-6, when enabled, provides one of the two lows required to enable stuff/destuff decoder U25. In 96-channel operation, U21-6 is low during bit times 1 through 8 of minor frame 0 of each frame. In 48-channel operation, U21-6 is low during bit times 1 through 4 of minor frame 0 of each frame. These specific bit times are the only times a stuff/destuff action, if necessary, can be accomplished. Table 2-1 lists the times when each input pin of U21-6 is high.

(*c*) Bit 9 gate U19-12 (sheet 3) provides a high to the DVOW smooth clock gates (*g*(2) below) during bit 9 time of each minor frame. The gate monitors 2^0, 2^1, and 2^2 count outputs from bit counter U10 and a 2^3 output through inverter U20-2. When all inputs are low (at bit 9 time), the gate puts its output pin U19-12 high.

(4) Bit count decoder U26 (sheet 3) sequentially decodes transmit channel clock group (TCHAN—) outputs as counter U10 and flip-flop U11-6 repeatedly cycle through their bit 1 through 16 and then bit 17 sequence. In 96-channel operation, U26 decodes TCHAN1— through TCHAN8—, in turn, two times for each minor frame; in 48-channel operation, it decodes TCHAN1— through TCHAN4—, in turn, four times for each minor frame. Eight inverters (U27 and U24) restore the decoder's outputs to TCHAN1 through TCHAN8 highs that go to corresponding group data input sections on DGP cards No. 1 through No. 4. Each TCHAN output denotes the time for a specific group to provide a data bit for insertion into the SG. Binary address inputs TBCT01, TBCT02, and TBCT04, and TGRPE— control decoder U26. In either 96- or 48-channel operation, TGRPE—— is high during all O/H bit times. This high puts the input addresses for U26 above the normal TCHAN1 through TCHAN8 decode range. As a result, all TCHAN outputs stay low while O/H bits are being inserted into the SG.

d. *Minor Frame Counter and Decoder.*

(1) Four-bit up binary counter U4 and flip-flop U11-10 (sheet 4) make up the minor frame counter that counts minor frames 0 through 19 (20 minor frames). Counter U4 is enabled at the end of each minor frame by the bit 17 high from U11-6 to its input pin U4-10. The next positive transition of TCLK (first bit time of next minor frame) increments counter U4

Table 2-1. Gate U21-6 Enables Times

Input pin	96-channel operation	48-channel operation
U21-1	Minor frame 0	Minor frame 0
U21-2	Bits 1 through 16	Bits 1 through 16
U21-4	Continuous	Bits 1 through 4 and 9 through 12
U21-5	Bits 1 through 8	Bits 1 through 8

one count. Counter U4 sequentially generates binary 0000 through 1111 (minor frames 0 through 15) count outputs. At binary 1111, the counter's TC pin U4-15 output goes high to flip-flop J input pin U11-14. The J input high lets the next TCLK positive transition toggle the flip-flop set and put its pin U11-10 (binary 2^4) output high. The same TCLK positive transition simultaneously clocks counter U4 to 0000 and puts it TC output low to flip-flop J input pin U11-14. Since the flip-flop cannot be toggled while its J-K inputs are low-high, it remains set and holds its 2^4 output high. With 2^4 high, minor frame counter U4, U10 sequentially provides binary 00001 through 11001 (minor frames 16 through 19) count outputs. The counter's sequential count outputs go to several minor frame count decoders whose outputs selectively enable various timing decode gates. One decoder (U7, sheet 5) sends a conditioning low to bit 341 flip-flop U2-6 (sheet 6) upon decoding minor frame 19. The conditioning low subsequently lets coinciding bit 17 and TCLK highs toggle the flip-flop set and puts its T341BT— output low. T341BT— presets counter U4 to 0000 and also lets a TCLK positive transition toggle flip-flop U11-10 reset. This preset/toggle action initializes minor frame counter U4, U10 for another minor frame count sequence.

(2) Bit 341 flip-flop U2-6 (sheet 6) generates complementary T341BT outputs immediately after bit 17 time that follows minor frame 19. Decoder U7 ((3)(*b*) below) holds flip-flop J2 input pin U2-5 low during minor frame 19. This low and +5 v pullup highs at JK pin U2-1 and J1 pin U2-4 condition the flip-flop for toggling at bit 341 time. A bit 17 high subsequently applied to J3 pin U2-12 lets the next TCLK positive transition set the flip-flop. The resulting pin U2-6 T341BT high performs the following on-card functions.

(*a*) The leading edge of T341BT clocks diagnostic detector flip-flop U8-6. The clocking action sets the flip-flop when T341BT represents the end-of-frame (EOF) bit for the last minor frame (19) in the last frame (5 or 11) of a major frame (TLFOMF high at the flip-flop's J-K input pins).

(*b*) T341BT at frame counter CET pin U15-10 lets the next TCLK positive transition increment counter U15 once. However, if the counter is at frame count 5 (48-channel operation) or frame count 11 (96-channel operation), T341BT and a TLFOMF high from gate U16-8 put gate pin U9-3 low. This low presets frame counter U15 to 0000 (frame count 0).

(*c*) T341BT goes low through gate U19-7 (sheet 3) and maintains bit counter U10 preset and conditions TDVOW time decoder gate U13-7 (sheet 5).

(*d*) T341BT is inverted through gate U19-7 (sheet 3) and restored to an inverter pin U20-6 TGRPE— high. This high holds all TCHAN outputs high while an EOF bit is being inserted in the SG data stream.

(*e*) T341BT— (pin U2-8 output) presets minor frame counter U4 (sheet 4) to 0000 and also lets a TCLK positive transition toggle flip-flop U11-10 reset.

(*f*) Returned to the bit 341 flip-flop's K2 input pin U2-10 (sheet 6), T341BT— lets the next TCLK positive transition toggle the flip-flop reset.

(3) Two decoders (U28, U7), three gates (U14-6, U14-8, U21-8), and two inverters (U20-12, U20-8) make up the minor frame count decoder (sheet 5). The minor frame count decodes selectively enable various timing decode gates (*g* below) to time the insertion of overhead information according to 96- and 48-channel message format (figs. 2-3 and 2-4).

(*a*) One-of-16 decoder U27 decodes minor frame counts in the binary order of its 2^0 through 2^3 address inputs. Minor frame counter U4 (sheet 4) increments the inputs from 0000 to 1111. A decoder enable pin U28-19 2^4 low from flip-flop U11-10 (sheet 4) lets decoder U28 (sheet 5) operate during counter U4's first 16-count sequence (minor frames 0 through 15). While thus enabled, U28 provides minor frame count 0, 1, 2, 3, 5, 6, 8, 10, 11, 13, and 15 decode lows, in turn to output gates and inverters. The 2^4 count input to enable pin U28-19 goes high at minor frame count 16 and inhibits decoder U28 while decoder U7 decodes higher minor frame counts. Decoder U28's address and enable inputs, corresponding minor frame count decodes, and affected output gates and inverters are listed in table 2-2.

(*b*) One-of-10 decoder U7 decodes minor frame counts 16, 18, and 19 in the binary order of its address inputs. Inputs 2^0, 2^1, and 2^2 come from counter U4 (sheet 4); a $\overline{2^4}$ input comes from flip-flop $\overline{Q}$ pin U11-9. While counter U4 cycles through its first 16-count sequence, decoder U28 (sheet 5) operates, but the $\overline{2^4}$ high raises decoder U7's address inputs above count 15, and therefore U7 does not decode any of its assigned out-

Table 2-2. Minor Frame Decoder Inputs and Outputs

Decoder U28 inputs and pins					Decoder U7 inputs and pins				Active (decode) output pin	Minor frame count decoded	Output gate or inverter pin high
2^0 -23	2^1 -22	2^2 -21	2^3 -20	EN -19	2^0 -15	2^1 -14	2^2 -1	$\overline{2^4}$ -2			
0	0	0	0	0	0	0	0	1	U28-1	0	U21-8, U20-8
1	0	0	0	0	1	0	0	1	U28-2	1	U14-6
0	1	0	0	0	0	1	0	1	U28-3	2	U20-12
1	1	0	0	0	1	1	0	1	U28-4	3	U14-8
0	0	1	0	0	0	0	1	1			
1	0	1	0	0	1	0	1	1	U28-6	5	U21-8
0	1	1	0	0	0	1	1	1	U28-7	6	U14-6
1	1	1	0	0	1	1	1	1			
0	0	0	1	0	0	0	0	1	U28-9	8	U14-8
1	0	0	1	0	1	0	0	1			
0	1	0	1	0	0	1	0	1	U28-11	10	U21-8
1	1	0	1	0	1	1	0	1	U28-13	11	U14-6
0	0	1	1	0	0	0	1	1			
1	0	1	1	0	1	0	1	1	U28-15	13	U14-8
0	1	1	1	0	0	1	1	1			
1	1	1	1	0	1	1	1	1	U28-17	15	U21-8
0	0	0	0	1	0	0	0	0	U7-13	16	U14-6
1	0	0	0	1	1	0	0	0			
0	1	0	0	1	0	1	0	0	U7-11	18	U14-8
1	1	0	0	1	1	1	0	0	U7-10	19	Direct to U2-5

puts. However, at count 16, $\overline{2^4}$ goes low, decoder U28 stops operating, and decoder U7 starts decoding in response to its in-range address inputs. U7's minor frame count 16 and 18 decode lows go to output gates U14-6 and U14-8, respectively, and its count 19 output decode low goes to bit 341 flip-flop U2-6 ((2) above). Decoder U7's address inputs, corresponding minor frame count decodes, and affected output gates are listed in table 2-2.

(*c*) Minor frame count decode output inverters and gates invert decoded lows to highs for application to timing decode gates. The inverters (U20-8, U20-12) and gates (U14-6, U14-8, U21-8) are listed in table 2-2, along with the active (high) outputs each one provides.

e. Frame Counter and Decoder (sheet 6).

(1) Frame counter U15 sequentially generates 4-bit binary frame count outputs TFCT01, TFCT02, TFCT04, and TFCT08. These outputs go to MO/C card 21A4 and to three on-card decode circuits. Except when the counter is being preset, each T341BT high from flip-flop U2-6 (*d*(2)(*b*) above) lets a TCLK positive transition increment counter U15 once. The counter repeatedly increments 12 times to provide frame count 0 through 11 outputs for 96-channel operation. The counter repeatedly increments six times to provide frame count 0 through 5 outputs for 48-channel operation. Gate U9-3 presets frame counter U15 to 0000 each time its TLFOMF and T341BT inputs (pins U9-1 and U9-2) are high. Last frame of major frame gates U16 ((2) below) decode and provide TLFOMF to gate U9-3. Bit 341 flip-flop U2-6 provides the T341BT input (*d*(2)(*b*) above) to gate U9-3.

(2) Last frame of major frame gates (U16-6, U16-8, U16-12) decode frame 5 or 11 in 48- or 96-channel operation, respectively. Gate U16-8 TLFOMF output is high during the last frame of each major frame and lets a TCLK positive transition set diagnostic detector flip-flop U8-6 (*h* below) and causes stuff code generator U18 (*f*(1) below) to generate the A pattern form of the frame synchronization and stuff code. TLFOMF also goes to a front panel SYNC jack.

(*a*) Gate U16-6 monitors the TFCT01, TFCT02, and TFCT08 binary count outputs of frame counter U15. When these three signals go high at frame count 11 (1101), U16-6 outputs a TFC11— (12th frame) low to MO/C card 21A4 and to gate pin U16-9. The gate inverts TFC11— to an output pin U16-8 TLFOMF high. A T341BT high subsequently coincides with the TLFOMF high and presets frame counter U15 to 0000 ((1) above).

(*b*) Gate U16-12 assumes TLFOMF decode control for 48-channel operation. This gate monitors the TFCT01 and TFCT04 outputs of U15 and the 48 CHE signal from MO/C card 21A4. The 48 CHE high at pin U16-13 conditions the gate to respond to coinciding TFCT01 and TFCT04 highs at pins U16-1 and U16-2, respectively. Each coincidence of the latter two inputs at frame count 5 (binary count 1010) puts output pin U16-12 low. This low inverts to a TLFOMF high at gate pin U16-8.

f. Stuff/Destuff Circuits.

(1) Stuff code generator U18 (sheet 4) is an 8-bit multiplexer. It generates the stuff code A and B pat-

terns and their complements for insertion by MO/C card 21A4 into the SG message format. TLFOMF from the last frame of major frame gates (*e*(2) above) and the 2^0 and 2^4 levels from the minor frame counter (*d*(1) above) select U18's output pattern bits. The minor frame counter provides three data input levels (data 0, 3, and 6) through gate U17-11 and inverter U27-12. The minor frame counter also controls U18's enable times by means of gate U13-9. Hardwired grounds and +5 v pullups provide the five remaining data input levels. The stuff code generator's input enable, select, data, and output pattern levels are listed in table 2-3 under their respective minor frame times. Although the stuff code generator is enabled (low at enable pin U18-10) to supply data bit outputs during minor frame times 0 through 15, 18, and 19, only 11 of the data bits are ultimately used as A or B pattern bits. A TFCET signal from frame code enable time gate U13-12 (*g*(3) below) selectively gates only the desired pattern bits through combiner circuits on MO/C card 21A4 for insertion in the SG data stream. TFCET highs coincide with overhead bit (bit 17) times for minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19 only. A or B pattern bits 0 through 10 are sequentially inserted into the O/H bit locations of designated minor frames. The bit 0 through 10 B pattern (10111111001) is inserted during frames 0 through 10 in 96-channel operation and frames 0 through 4 in 48-channel operation. The bit 0 through 10 A pattern (00001010011) is inserted during last frame 11 in 96-channel operation and last frame 5 in 48-channel operation. The A and B patterns described above and listed in table 2-3 are those for TSCODE (stuff action to be transmitted). Their complements appear at pin U18-14 as TSCODE— and are selected by MO/C card 21A4 when a no stuff action is to be transmitted.

Table 2-3. Stuff Code Generator Operating Logic Levels

Minor frames.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
TFCET at pin U13-12 (output to MO/C 21A4).	0	0	0	1	1	0	0	1	1	1	0	0	1	1	1	0	0	1	1	1
Enable in at pin U18-10 ($\overline{2^1}$ or 2^4 from U13-9).	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Select at S1 pin U18-11 (2^4 from FF U11-10).	0	0	0	0	0	0	0*	0	0	0	0	0	0	0	0	0	1	1	1	1
TLFOMF at S2 pin U18-12 (during last frame only).	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
TLFOMF at S2 pin U18-12 (during all other frames).	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Select at S3 pin U18-3 (2^0 from counter U4-14).	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Data 0 in at I0 pin U18-1 ($\overline{2^3}$ or 2^3 from U17-11).	1	1	1	1	0*	0	0	0	1*	1 (See note 1)	1	1	1*	1	1*	1	1	1	1	1
Data 1 in at I1 pin U18-2 (hardwired ground).	0	0	0	0	0	0	0	0	0	0 (See note 1)	0	0	0	0	0	0	0	0	0*	0
Data 2 in at I2 pin U18-3 (hardwired ground).	0	0	0	0	*0*	0	0	0	*0*	0 (See note 2)	0	0	*0*	0	*0*	0	0	0	0	0
Data 3 in at I3 pin U18-4 ($\overline{2^3}$ or 2^3 from U17-11).	1	1	1	1	0	0	0	0	1	1 (See note 2)	1	1	1	1	1	1	1	1	*1*	1
Data 4 in at I4 pin U18-5 (hardwired +5 v pullup).	1	1	1	1*	1	1	1	1*	1	1* (See note 1)	1	1	1	1*	1	1	1	1	1	1

See notes at end of table.

Table 2-3. Stuff Code Generator Operating Logic Levels—Continued

Minor frames.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Data 5 in at I5 pin U18-6 (hardwired + 5 v pullup).	1	1	1	1	1	1	1	1	1	1 (See note 1)	1	1	1	1	1	1	1	1	1	1*
Data 6 in at I6 pin U18-7 ($\overline{2^1}$ from inverter U27-12).	1	1	0	*0*	1	1	0	*0*	1	*1* (See note 2)	0	0	1	*1*	0	0	1	1	0	0
Data 7 in at I7 pin U18-9 (hardwired + 5 v pullup).	1	1	1	1	1	1	1	1	1	1 (See note 2)	1	1	1	1	1	1	1	1	1	*1*
Pattern bit number.				0	1			2	3	4			5	6	7			8	9	10
A pattern at Z pin U18-15 (during last frame only).				0	0			0	0	1 (See note 3)			0	1	0			0†	1	1
B pattern at Z pin U18-15 (during all other frames).				1	0			1	1	1 (See note 3)			1	1	1			0†	0	1

Notes:

1. 1* or 0* denotes B pattern bit level decoded.
2. *1* or *0* denotes A pattern bit level decoded.
3. 0† denotes that U18 is not enabled during minor frame 17; U18-15 is automatically 0.

(2) Stuff/destuff decoder U25 (sheet 4) generates transmit channel clock delete group (TCHN1 through TCHN8) lows in response to DLTTY lows from MO/C card 21A4. Gate U21-6 (*c*(3)(*b*) above) conditions input pin U25-18 only at bit times during which a stuff/destuff operation may be performed on a DGP card. The pin U25-18 conditioning level is a low only during minor frame 0 bit times 1 through 8 in 96-channel operation or during minor frame 0 bit times 1 through 4 in 48-channel operation. If DLTTY is low at pin U25-19 when a conditioning low is applied, the output TCHN line corresponding to the frame count at the four address pins of U25 will be put low.

(3) Stuff request strobe gate U13-4 (sheet 5) and inverter U24-6 (sheet 6) decode complementary transmit stuff request strobe (TSREST and TSREST—) outputs. Coinciding bit 17— (pin U11-7) and minor frame count 2— (decoder pin U28-3) lows put pin U13-4 TSREST high. Inverter U24-6 complements the high to a TSREST— low. TSREST goes to MO/C card 21A4's stuff request circuit in the transmit TC (M) application. TSREST— controls DDOW time decode gates U23 (*g*(4) below); TSREST— also goes to FS card 21A7's destuff detection circuit in the receive TC (D) application.

g. Timing Decode Gates.

(1) DVOW time decoder U6-8, U13-7 (sheet 5) generates transmit digital voice orderwire clock (DVOW) highs at the SG message format overhead bit times assigned for digital voice orderwire (DVOW) bit entry (figs. 2-3 and 2-4). One-half of U6 inverts minor frame time 0, 5, 10, and 15 decode highs from gate U21-8 (table 2-2) during 96- and 48-channel operation. During 48-channel operation, a 48 CHE high at input pin U6-9 also lets the second half of U6 invert minor frame time 1, 6, 11, and 16 highs from gate U14-6 (table 2-2). U6's output minor frame time lows go to gate pin U13-6. Each low lets a bit 17 low at pin U13-5 enable a TDVOW high at pin U13-7. Gate U19-7 (sheet 3) provides the bit 17 lows.

(2) DVOW smooth clock gates U6-6 (sheet 5) generate transmit digital voice orderwire smooth clock (TDVOWC—) lows to the input section of DVOW card 21A11. The smooth clock is used to evenly space the eight-per-frame DVOW bit sampling times during 48-channel operation. Gate U21-8 provides minor frame time 0, 5, 10, and 15 decode highs (table 2-2) to input pin U6-4. Bit 17 highs from flip-flop U11-6 (sheet 3) enable output pin U6-6 TDVOWC— lows (sheet 5) at bit 17 times of minor frames 0, 5, 10, and 15. Gate U14-8 provides minor frame time 3, 8, 13, and 18 decode highs (table 2-2) to input pin U6-2. Bit 9 highs from gate U19-12 (sheet 3) enable output pin U6-6 TDVOWC— lows (sheet 5) at bit 9 times of minor

frames 3, 8, 13, and 18.

(3) Frame code enable time gate U13-12 (sheet 5) generates TFCET lows during bit 17 times of those minor frames assigned for frame synchronization and stuff pattern bits. All the minor frame time decode highs from gates U14-6 and U21-8 and inverter U20-12 (table 2-2) inhibit gate U13-12. As a result, the gate can respond to an input pin U13-15 bit 17 low only when all its minor frame time decode inputs are lows. The coinciding lows let bit 17 lows enable TFCET highs during O/H bit times of minor frames 3, 4, 7, 8, 9, 12, 13, 14, 17, 18, and 19. MO/C card 21A4 sequentially inserts A pattern bits (A0 through A10) during the O/H bit times of designated minor frames during the last frame of each major frame, and inserts B pattern bits (BO through B10) at the corresponding O/H bit times of all other frames.

(4) DDOW time decoder U23 (sheet 6) generates a transmit digital data orderwire (TDTAOW) high only during bit 17 time of minor frame 2 in frame 0 of each major frame. Coinciding frame count TFCT01, TFCT02, TFCT04, and TFCT08 lows from frame counter U15 (*e*(1) above) enable gate pin U23-12 high only during the first frame (frame 0) of each major frame. Inverter U23-9 inverts this high to a conditioning low at gate pin U23-2. At bit 17 time of minor frame 2, gate U13-4 (*f*(3) above) puts the inverter pin U24-6 TSREST— output low. Applied at pin U23-3, TSREST enables a pin U23-4 TDTAOW output high. Each TDTAOW high lets one TCLK— clock increment DDOW card 21A11's read address counter and transfer a TTYOWI data bit to MO/C card 21A4 for insertion in the outgoing SG data stream.

h. Diagnostic Detector. The diagnostic detector consists of flip-flop U8-6 (sheet 6), TLFOMF activity monitor one-shot U22-13 (sheet 2), TDAP24— and TDFALT detect gates U19 and U17, and diagnostic indicator light emitting diode (LED) DS1. Each T341BT positive transition clocks flip-flop U8-6, and when TLFOMF is high, U8-6 is set (end of each major frame's last frame). The next T341BT high (frame 0) clocks the flip-flop reset again. Recurring positive transitions from flip-flop pin U8-6 retrigger one-shot U22-13 and keep its pin U22-13 and U22-4 outputs high and low, respectively. The high conditions gate U17-3 (through backplane jumper TTCCT02) for control of TDFALT and TDAP24— outputs by a TDEP4 input from MO/C card 21A4. The low inhibits gate U17-6 (through backplane jumper TTCCT01) to hold diagnostic indicator DS1 turned off. When T341BT and TLFOMF pulses do not occur and regularly set and reset flip-flop U8-6, one-shot U22-13 times out and reverses its output polarities. Now a pin U22-13 low inhibits gate U17-3, while a pin U22-4 high and a +5 v pullup high enables gate pin U17-6 low. This low lights diagnostic indicator DS1 and puts the gate pin U17-8 TDFALT output high to AD card 21A1. The TC (M) and TC (D) cards' diagnostic detector circuits are included in the EQUIP and FRAME ALARM circuits simplified diagram in figure FO-2. Overall operation of the alarm circuits is described in paragraph 2-15*f*.

i. TC (M) and TC (D) Card Operational Differences. The principal difference between TC cards 21A5 used in multiplexer (M) and demultiplexer (D) sections is the operation of their bit, minor frame, and frame counters. The three counters are free running on the TC (M) card; however, FS card generated frame and major frame sync signals control the three counters on the TC (D) card. Also, the diagnostic detector on the TC (D) card monitors more signals than does the diagnostic detector on the TC (M) card. FS card 21A7 holds RFSYNC— low until it decodes the first incoming frame sync pattern. This decode decrements a confidence counter one count and puts RFSYNC— high. The confidence counter subsequently decrements or increments as other anticipated frame sync patterns are decoded or missed. When enough patterns are missed to increment the counter to its maximum count, RFSYNC— goes low again. The FS card also holds RMSYNC— low until it decodes the first incoming major frame sync pattern. This decode decrements another confidence counter, which puts RMSYNC— high. Both confidence counters operate similarly.

(1) An RFSYNC— low from FS card 21A7 holds data bit counter U10 (*c*(1) above) reset and bit 17 flip-flop U11-6 (*c*(2) above) cleared. When the first frame sync pattern is decoded, RFSYNC— goes high and lets U10 and U11-6 operate.

(2) The RFSYNC— low also holds minor frame counter U4, U11-10 (*d*(1) above) reset. Upon going high, RFSYNC— releases counter U4, U11-10, which starts incrementing in response to coinciding bit 17 and RCLK high inputs.

(3) The RFSYNC— low also holds bit 341 flip-flop U2-6 (*d*(2) above) reset.

(4) An RFSYNC— low from FS card 21A7 holds frame counter U15 (*e*(1) above) reset. When a major frame sync pattern is decoded, RFSYNC— goes high and releases U15. U15 can subsequently increment response to coinciding R341BT and RCLK high inputs.

(5) Divide-by-2 flip-flop U8-9 (*b*(3) above) must operate in phase with received SG data during 48-channel operation. Upon release for operation (48 CHE high at direct reset pin U8-15), flip-flop U8-9 remains reset until the receive phase forcing (RPHF) low at its J input pin U8-14 goes high. RPHF goes high so as to let RMASCLK— clock pulses from inverter U24-2 start toggling flip-flop U8-9 in phase with received SG data bits.

(6) Diagnostic detector gate U17-6's operation (*h* above) is controlled by the receive diagnostic enable priority 2 (RDEP2—) signal at its input pin U17-4. Al-

so, diagnostic detector gate U19-9 monitors an RDEP2 signal from MO/C card 21A4. The TC (D) card's diagnostic detector is included in the EQUIP and FRAME ALARM circuits simplified diagram in figure FO-2. The detector's operation is described in paragraph 2-15*f*.

Section VII. DUAL GROUP PROCESSOR (DGP) CARD 21A6

2-24. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the DGP card. There are four DGP cards (21A6 No. 1 through No. 4) in the TD-976/G. A DGP card has dual input sections and dual output sections. Each input section processes incoming data for one group, and each output section processes outgoing data for one group. The input section and output section block diagram discussions in paragraphs 2-25 and 2-26 are based on the input section and output section block diagrams in figures 2-10 and 2-11. The detailed theory of operation in paragraphs 2-27 and 2-28 is based on the DGP card schematic diagram in figure FO-6.

2-25. Input Section Block Diagram Discussion

(fig. 2-10)

a. General. The DGP card's two input sections, which are designated channel A and channel B, are functionally identical. Therefore, only the channel A input section is discussed and shown in figure 2-10. The block diagram discussion is divided into four functional circuit descriptions as follows:

(1) The timing extractor divider (*b* below) divides a 4608 kHz channel clock to create an extracted clock that is used for timing group data processing operations performed by the input rate buffer.

(2) Clock and pattern inverters (*c* below) receive TD-976/G internally generated 576 kHz and activity pattern signals for distribution to on-card circuits. These inverters route activity and dummy patterns and timing to channel A and channel B circuits.

(3) The input selector (*d* below) provides a means for routing compatible timing and data or pattern signals to the input rate buffer. It routes a clock signal that has been extracted from incoming group data when the incoming group data are selected for processing. It routes an internally generated clock signal when an activity pattern or dummy pattern is selected for processing.

(4) The input rate buffer (*e* below) converts incoming asynchronous data into a synchronous output. An elastic storage register performs the conversion under control of addressing signals from write and read address counters. The elastic storage register is like an 8-bit random access memory into which data bits can be serially entered (written) at one rate and serially accessed (read out) at a different rate.

b. Timing Extractor Divider. This circuit receives a 4608 kHz channel clock (CHAN) from the MO/C card and divides it to create an extracted clock output. Periodic reset strobe group (RST—) pulses from the GTM card reset and restart timing extractor divider U1 to keep its output synchronized with the incoming group data bits. The GTM card generates an RST— pulse each time an incoming data positive transition occurs. Applied through input selector U2, U1's extracted clock increments the input rate buffer's write address counter and clocks group data bits into its elastic storage register. The extracted clock is at a normal 576 kHz rate.

c. Clock and Pattern Inverters. Inverter U18-2 receives and inverts a 576 kHz output 2 (576 kHz 2) clock from the MO/C card for application to the channel B portion of the card. U16-10 restores the 576 KHZ 2 signal for application to input selector U2 and to the output selector in the output section (para 2-26c). Inverter U18-6 receives a 7-bit repetitive activity pattern (APAT 1) from the GTM card and complements it to supply a 7-bit dummy pattern to channel A and B input selectors. Inverter U16-8 restores the dummy pattern to an APAT 1 for application to input selector U2 and to the output selector in the output section (para 2-26c).

d. Input Selector. Input selector U2 selects a data and timing input for routing to the input rate buffer. U2 is controlled by logic levels from switch S1 and the input good status (IGS—) signal from the AD card. Normally, switch S1 will be in the ON position (group is active) and U2 will select and route the input group data (IGRPD) and extracted clock to the input rate buffer. If there is no activity on the input group data line, as detected by GTM card 21A2, AD card 21A1 generates a high-level IGS— signal that causes U2 to select the dummy pattern and 576 KHZ 2 clock for application to the input rate buffer. When S1 is placed to OFF the activity pattern and 576 KHZ 2 are selected.

e. Input Rate Buffer.

(1) The clock from input selector U2 (nominal 576 kHz rate) is applied through inverter U35-2 as the write clock that increments write address counter U31. The counter produces 3-bit binary address write outputs. The write address outputs sequentially select elastic storage register U8's bit storage cells for entry of selected data bits. The clock from U2 (complement of the write clock) clocks the data into register U8.

(2) Each coincidence of a transmit clock (TCLK)

and a transmit channel clock (TCHAN) (coincidences occur at the group sampling rate of 576.563 kHz), unless inhibited by a transmit channel clock delete (TCHN), increments read address counter U15. In turn, the read address outputs sequentially select elastic storage U8's bit storage cells for outputting group (GRP) data. The two counters operate with a nominal four-count offset between them; but because the coincidences of TCLK's and TCHAN's occur at a higher rate (nominal 576.563 kHz) than the write clocks (nominal 576 kHz), the read address counter advances on the write address counter. When the read address counter advances to within three counts of the write address counter, rate comparator flip-flop U23 detects this condition and produces a rate compare (RCOM) signal ((4) below), requesting that a stuff action be performed. The stuff request circuits on MO/C card 21A4 recognize this condition and cause TC (M) card 21A5, at the proper time, to put TCHN low for one coincidence of a TCLK and TCHAN, inhibiting the read counter from incrementing. This action (stuffing) reestablishes the desired offset of four counts between the two counters.

(3) Elastic storage register U8 temporarily stores asynchronous data for synchronous transfer to the MO/C card. Counter U31's 8-bit write address outputs select the register's bit 1 through bit 8 storage cells in turn. The selected clock signal (synchronous with the selected data) from input selector U2 enters the data bits into the sequentially selected storage cells. Counter U15's read address outputs, which are normally delayed four counts, sequentially transfer the data bits from the storage cells to the MO/C card.

(4) Rate comparator flip-flop U23 sends a rate compare (RCOM) status signal to the MO/C card. U23 monitors the write address counter's most significant digit (MSD, count 4) output. Positive transitions of the read address counter's MSD output clock the first counter's MSD level into U23. If the MSD level is low (counters offset desired four counts), U23 remains reset and its RCOM output stays low. However, when the read counter advances to within three counts of the write counter, the write counter's MSD level is high when a read counter MSD positive transition occurs, and the positive transition clocks U23 set. The clock-set action puts U23's RCOM output high. This high goes through the MO/C card's stuff request circuits to the TC (M) card's stuff circuits. The stuff circuits respond with a TCHN low, which slows the read address counter one count ((2) above).

2-26. Output Section Block Diagram Discussion

(fig. 2-11)

a. General. The DGP card's two output sections, which are designated channel A and channel B, are functionally identical. Therefore, only the channel A output section is discussed and shown in figure 2-11. The block diagram discussion is divided into four functional descriptions as follows:

(1) The destuff gate (*b* below) controls application of write address counter clock pulses during group data processing. The gate provides for periodical inhibiting of single clock pulses to accomplish destuffing operations.

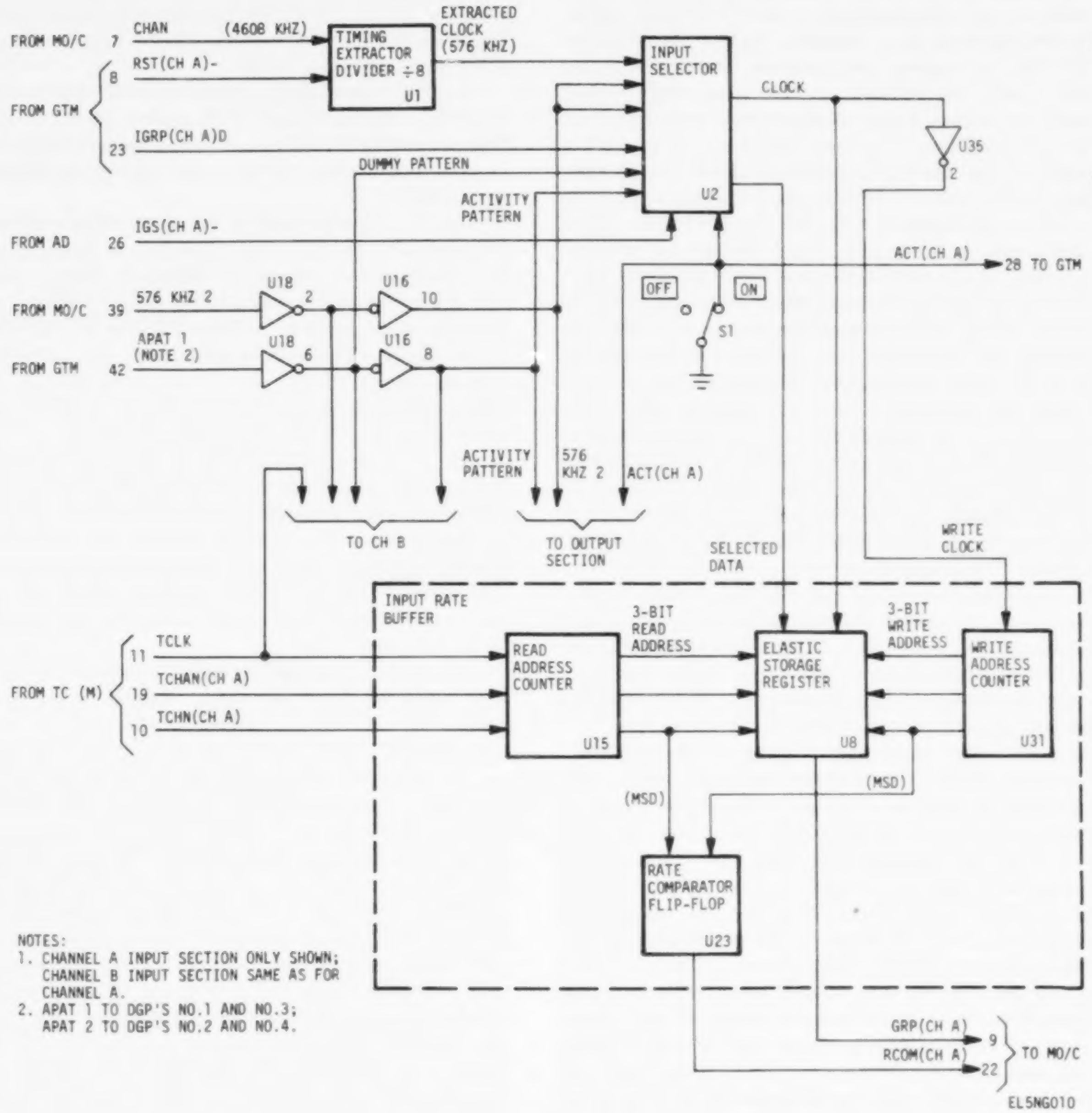
(2) The output selector (*c* below) provides a means for routing compatible timing and data or pattern signals to the output rate buffer. Normally, the SG data and the output of the destuff gate will be selected as the data and timing to be routed to the output rate buffer. However, if the demultiplexer section is unable to acquire major frame sync or if the given group is inactive, an internally generated activity pattern and clock signal are selected as the data and timing.

(3) The output rate buffer (*d* below) extracts a given group's data from the incoming SG data stream. Write and read address counters control an elastic storage register that extracts the data and then outputs the data at a smooth rate. A phase-locked loop circuit varies the read address counter's clock rate to maintain a smooth data output rate that is the average of the data input rate.

(4) The output logic (*e* below) converts the data and timing outputs of the output rate buffer to levels compatible with interfacing equipments.

b. Destuff Gate. During processing of incoming group data, coincidences of receive clocks (RCLK—) and receive channel clocks (RCHAN) (coincidences occur at the nominal 576.563 kHz group sampling rate), unless inhibited by receive channel clock deletes (RCHN), are gated through U29-12 to clock the write address counter elastic storage register. RCHN goes low whenever the demultiplexer section is to accomplish a destuff action to compensate for a stuff action transmitted by the far-end multiplexer section (destuff actions occur at a nominal 563 Hz rate). A destuff action (RCHN low) inhibits one coincidence of an RCLK— and RCHAN and will occur a maximum of once for each group in a major frame, since that is the maximum rate at which the multiplexer section can take stuff actions. Thus, the output pulses of U29-12 occur at the average rate of the incoming group data but are not regularly (uniformly) spaced.

c. Output Selector. Output selector U17 selects a data and timing output for routing to the output rate buffer. U17 is controlled by logic levels from card-mounted switch S1 (ACT(CH A)) and the receive major frame sync (RMSYNC—) signal from the FS card. Normally, switch S1 will be in the ON position (group is active) and ACT(CH A) will be low and RMSYNC— will be high (demultiplexer section has acquired major frame sync). In this case, SG data (SDATA) and the


FROM MO/C 7
CHAN
(4608 KHZ)
FROM GTM
8
RST(CH A)-
23
IGRP(CH A)D
TIMING EXTRACTOR DIVIDER ÷8
U1
EXTRACTED CLOCK (576 KHZ)
INPUT SELECTOR
U2
CLOCK
U35
2
DUMMY PATTERN
ACTIVITY PATTERN
FROM AD 26
IGS(CH A)-
ACT(CH A)
28 TO GTM
OFF
ON
S1
FROM MO/C 39
576 KHZ 2
U18
2
U16
10
FROM GTM 42
APAT 1 (NOTE 2)
U18
6
U16
8
ACTIVITY PATTERN
576 KHZ 2
ACT(CH A)
TO CH B
TO OUTPUT SECTION
SELECTED DATA
WRITE CLOCK
INPUT RATE BUFFER
3-BIT READ ADDRESS
3-BIT WRITE ADDRESS
FROM TC (M)
11
TCLK
19
TCHAN(CH A)
10
TCHN(CH A)
READ ADDRESS COUNTER
U15
ELASTIC STORAGE REGISTER
U8
WRITE ADDRESS COUNTER
U31
(MSD)
(MSD)
RATE COMPARATOR FLIP-FLOP
U23
GRP(CH A)
9
RCOM(CH A)
22
TO MO/C
EL5NG010

NOTES:
1. CHANNEL A INPUT SECTION ONLY SHOWN; CHANNEL B INPUT SECTION SAME AS FOR CHANNEL A.
2. APAT 1 TO DGP'S NO.1 AND NO.3; APAT 2 TO DGP'S NO.2 AND NO.4.

Figure 2-10. DGP card 21A6 input section, block diagram.

output of the destuff gate will be selected as the data and timing. If S1 is placed to OFF or if the demultiplexer section is unable to acquire major frame sync, the activity pattern and 576 KHZ 2 will be selected as the data and timing. This selection will deep the phase-locked loop (*d*(4) below) operating at its nominal 576 kHz frequency.

d. Output Rate Buffer.

(1) The clock from output selector U17 is applied through inverter U35-4 as the write clock that increments 4-bit write address counter U10. The counter produces 3-bit binary write address outputs. The two least significant digit outputs (counts 1 and 2) go directly to elastic storage register U9. Inverter U16-1 complements the count 4 output and effectively advances the elastic storage register's write address inputs four counts. This advance imparts a four-count offset between the register's write and read address inputs. The write address counter's most significant digit (MSD) output (count 8) goes to the phase-locked

loop ((4) below) for comparison with the read counter's MSD output.

(2) The 4-bit read address counter sequentially generates a 3-bit read address output to the elastic storage register. The counter's MSD output goes to the phase-locked loop for comparison with the write counter's MSD output. Detection of any phase difference between the two MSD outputs results in a phase-locked loop action that slowly and smoothly decreases or increases the read address counter's clock input. This action locks the read counter to the write counter, which is being clocked at the incoming data rate. Thus, the read counter is clocked at the same average rate as the write counter. Variations in the incoming data rate and the irregular spacing of the write clocks are smoothed by the phase-locked loop action.

(3) Elastic storage register U9 operates like the input section's elastic storage register described in paragraph 2-25*e*(3). Selected clock pulses from output selector U17 clock data bits into the U9 bit storage cells. Write address inputs sequentially address the storage cells for serial entry of the data bits. Read address inputs, which are delayed four counts, serially transfer the register's data bits to the output logic.

(4) The phase-locked loop provides a smooth clock for incrementing the read address counter and operating a timing pulse generator in the output logic. Voltage-controlled oscillator (VCO) U7 generates a nominal 576 kHz clock signal. A phase comparator controls the VCO's frequency rate by means of an RC network. Phase comparator U5 monitors MSD outputs from the write and read address counters for phase variations.

(a) When the phase of the write counter's MSD output leads the read counter's MSD output, U5 generates narrow + 10 v pulses (every 16th write clock). Conversely, when the phase of the write counter's MSD output lags the read counter's MSD output, U5 generates narrow 0 v (ground) pulses. U5 outputs an open (infinite impedance) when both counters' MSD outputs are exactly in phase. The periodic + 10 v or 0 v pulses progressively charge or discharge C19 in the RC network through high-value resistor R23. A rising charge voltage increases VCO U7's output frequency rate; a falling charge voltage decreases the output frequency. When the counters are operating exactly in phase, a continuous open from the phase comparator lets C19 retain its charge and hold VCO U7's frequency constant.

(*b*) Although the VOC's output frequency varies above and below the instantaneous frequency of the write clocks, its nominal (smooth) frequency rate is equal to the average rate of write clocks (normally 576 kHz). The fast acquisition circuit accelerates the phase-locked loop's ability to lock to the input write clocks upon power turn-on or immediately after temporary loss of power. As power is rising toward + 12 v, the RC circuit of C26, CR5, R40 is activated and closes analog switch U13 for a short period of time.

(*c*) U13's switch closure parallels low-value resistor R27 with R23, thus decreasing the input resistance path to the RC network and allowing it to rapidly respond to the output of the phase comparator. Switch S13 subsequently opens and restores the normal high-resistance input path to the RC network. The voltage regulator (Q9, VR2) maintains phase comparator U5 and VCO U7 operating power at a regulated + 10 v level. Buffer/converter U11 converts the VCO output to TTL levels that are applied directly to timing pulse generator U27, and through inverter U18-12, to read address counter U10.

e. Output Logic.

(1) Each negative transition of the phase-locked loop output triggers pulse generator U27 into a nominal 100-nanosecond duty cycle. U27's true (positive pulse) output clocks data buffer flip-flop U34 and is also outputted as output group timing (OGRP(CH A)T) to the GTM card. U27's negative pulse output goes to level shifter Q2, Q3.

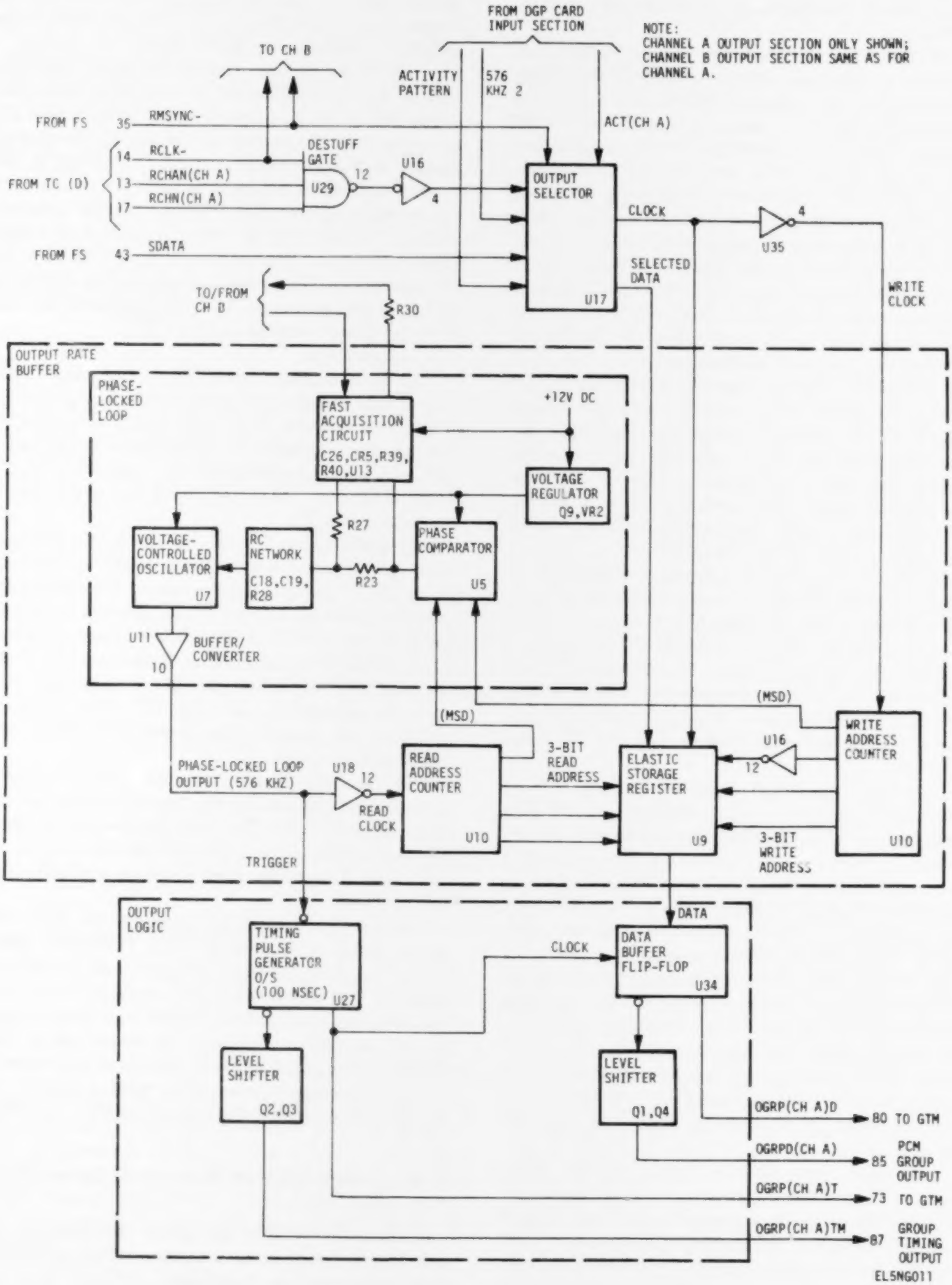
(2) Level shifter Q2, Q3 converts U27's 100-nanosecond negative pulse output to TD-660/G compatible levels (fig. 2-1). Each negative-going 100-nanosecond pulse switches Q2 off and Q3 on, placing the output group timing (OGRP(CH A)TM) line at approximately 0 volt. When Q2 is switched on, it switches Q3 off and the OGRP(CH A)TM line goes to approximately − 2.2 volts. An external 91 ohms load (TD-660/G) must be connected to complete the circuit and allow these levels to be produced.

(3) The data output of the elastic storage register is clocked into data buffer flip-flop U34 by the positive pulse output of U27. The true data output of U34 is supplied as output group data (OGRP(CH A)D) to the GTM card. A complementary output is applied to level shifter Q1,Q4.

(4) Level shifter Q1,Q4 converts the TTL NRZ output levels of U34 to an NRZ TD-660/G format (logic 1 is approximately 0 volt and logic 0 is approximately − 2.2 volts). When U34 contains a logic 1, its output to the level shifter is a low level that switches Q1 off and Q4 on, placing the output group data (OGRPD(CH A)) line to the TD-660/G at approximately 0 volt. Conversely, when U34 contains a logic 0, the OGRPD(CH A) line goes to approximately − 2.2 volts.

2-27. Input Section Theory of Operation
(fig. FO-6)

a. Introduction. This paragraph describes the detailed operation of an input section on DGP card 21A6. Each DGP card has functionally identical input sections designated channel A and channel B. The chan-


FROM DGP CARD INPUT SECTION
TO CH B
ACTIVITY PATTERN
576 KHZ 2
ACT(CH A)
FROM FS
35
RMSYNC-
14
RCLK-
FROM TC (D)
13
RCHAN(CH A)
17
RCHN(CH A)
DESTUFF GATE
U29
12
U16
4
OUTPUT SELECTOR
U17
CLOCK
4
U35
SELECTED DATA
WRITE CLOCK
FROM FS
43
SDATA
TO/FROM CH B
R30
OUTPUT RATE BUFFER
PHASE-LOCKED LOOP
FAST ACQUISITION CIRCUIT
C26,CR5,R39, R40,U13
+12V DC
VOLTAGE REGULATOR
Q9,VR2
R27
VOLTAGE-CONTROLLED OSCILLATOR
U7
RC NETWORK
C18,C19, R28
R23
PHASE COMPARATOR
U5
U11
10
BUFFER/ CONVERTER
(MSD)
(MSD)
PHASE-LOCKED LOOP OUTPUT (576 KHZ)
U18
12
READ CLOCK
READ ADDRESS COUNTER
U10
3-BIT READ ADDRESS
ELASTIC STORAGE REGISTER
U9
U16
12
WRITE ADDRESS COUNTER
U10
3-BIT WRITE ADDRESS
TRIGGER
OUTPUT LOGIC
TIMING PULSE GENERATOR O/S (100 NSEC)
U27
CLOCK
DATA
DATA BUFFER FLIP-FLOP
U34
LEVEL SHIFTER
Q2,Q3
LEVEL SHIFTER
Q1,Q4
OGRP(CH A)D
80 TO GTM
OGRPD(CH A)
85 PCM GROUP OUTPUT
OGRP(CH A)T
73 TO GTM
OGRP(CH A)TM
87 GROUP TIMING OUTPUT

NOTE:
CHANNEL A OUTPUT SECTION ONLY SHOWN;
CHANNEL B OUTPUT SECTION SAME AS FOR
CHANNEL A.

EL5NG011

Figure 2-11. DGP card 21A6 output section, block diagram.

nel A sections of DGP cards No. 1 through No. 4 individually process incoming data for groups 1, 2, 3, and 4. The channel B sections of the same cards individually process incoming data for groups 5, 6, 7, and 8. Only the channel A input section theory of operation is discussed as typical. The theory of operation is divided into four functional descriptions established in the input section block diagram discussion, as listed below.

(1) Timing extractor divider (*b* below).
(2) Clock and pattern inverters (*c* below).
(3) Input selector (*d* below).
(4) Input rate buffer (*e* below).

NOTE

> Unless otherwise noted, all circuits discussed in *b* through *e* below are shown on sheet 3 of figure FO-6. Input inverters that serve channel's A and B circuits are identified and their dual functions are defined.

b. Timing Extractor Divider. This circuit is a divide-by-8 counter (U1) that is clocked at a 4608 kHz rate by the channel clock (CHAN) input from MO/C card 21A4. GTM card 21A2 generates a short-duration reset strobe (RST—) pulse each time a group data positive (logic 0 to logic 1) transition occurs. Each RST— negative pulse briefly resets counter U1 and restarts it. The recurring reset/start actions insure that the counter's extracted clock output pulses (nominal 576 kHz) remain aligned within an eighth of a bit time of received group data bits. A high (+5 v pullup) at the counter's PE, CEP, and CET pins (U1-9, -7, and -10) lets the counter operate continuously while equipment power and CHAN are applied. Counter U1's extracted clock output is synchronized with the incoming group data but is not synchronized with the TD-976/G's internally generated 576 kHz clock.

c. Clock and Pattern Inverters. Two inverters are used to receive DGP card clock and pattern inputs for fanout through other inverters to several on-card circuits.

(1) U18-2 and U16-10 apply to 576 KHZ 2 clock from MO/C card 21A4 to three input pins of channel A input selector U2 and to three input pins of channel A output selector U17. Another inverter (U18-4, sheet 4) restores the 576 KHZ 2 clock to corresponding pins of channel B input and output selectors (U32 and U24, sheet 4).

(2) The MO/C card's 576 KHZ 1 clock operates an activity pattern generator on GTM card 21A2 that provides activity pattern 1 (APAT 1) to DGP cards No. 1 and No. 3, and APAT 2 (delayed three bit periods) to DGP cards No. 2 and No. 4 APAT is a repeating 7-bit pattern (1011000, with rightmost bit as leading bit) that is processed through a DGP card channel's input section when the given group is inactive (card-mounted switch S1 or S2 set to OFF). APAT enters a DGP card through pin 42, inverts through U18-6, restores through U16-8, and is applied to two pins of channel A input selector U2 and to three pins of channel A output selector U17. The U16-8 output also goes to corresponding pins of channel B input and output selectors (U32 and U24, sheet 4). The complemented pattern (0100111) at U18-6 is the dummy pattern that is processed through a DGP card channel's input section when the given group is active (card-mounted switch S1 or S2 placed to ON) and the GTM card does not detect activity on the group's input line. The inverter pin U18-6 dummy pattern goes directly to channel A input selector pin U2-11 and to the corresponding pin of the channel B input selector (U32, sheet 4).

d. Input Selector. Input selector U2 is a dual four-input multiplexer. One section selectively routes data (input group, dummy pattern, or activity pattern) to the input rate buffer's elastic storage register (*e*(3) below). The other section routes the related timing (extracted clock or 576 KHZ 2) to the elastic storage register and a write counter (*e*(1) below). An input good group status (IGS—) signal from AD card 21A1 and ON/OFF (logic 0 and logic 1) levels from card-mounted switch S1 determine the data and timing input that is selected. The switch S1 ON/OFF activity select (ACT) level also informs GTM card 21A2 whether the group is active or inactive. U2's four select input level combinations and corresponding data and clock outputs are listed in table 2-4.

Table 2-4. Input Selector U2 Operating Conditions

Select inputs		U2 inputs selected for routing to input rate buffer	
Pin U2-13 (IGS—)	Pin U2-3 (S1, ACT)	Pin U2-15 output (selected data)	Pin U2-1 output (selected clock)
0	0	Input group data (pin U2-12 input).	Extracted clock (pin U2-4 input).
1	0	Dummy pattern (pin U2-11 input).	576 KHZ 2 (pin U2-5 input).
0	1	Activity pattern (pin U2-10 input).	576 KHZ 2 (pin U2-6 input).
1	1	Activity pattern (pin U2-9 input).	576 KHZ 2 (pin U2-7 input).

e. Input Rate Buffer. The input rate buffer converts its asynchronous input data stream into an output data stream that is synchronous with the TD-976/G internal timing. An eight-cell elastic storage register (U8) performs the asynchronous-to-synchronous conversion under control of write and read address counters (U31 and U15). The write address counter sequentially selects the register's bit storage cells for clock entry (write-in) of selected data. The read address counter, which is delayed four counts, sequentially accesses (reads out) data bits from the register's cells for output to MO/C card 21A4. As the asynchronous data are being processed, the read counter operates faster than the write counter and gradually advances on it (para 2-25*e*(2)). Periodic deletions of single read counter clock pulses (stuffing operations) delay the read counter one clock period to maintain its read address outputs four counts behind the write counter's address ouputs. A rate comparator flip-flop (U23-6), controlled by both counters' most significant digit (MSD) outputs, sends an RCOM to MO/C card 21A4 when the read counter advances to within less than four counts of the write counter. In turn, the MO/C card signals TC (M) card 21A5 to perform a stuff operation. The TC (M) card responds with a clock delete signal that blocks one read counter clock pulse (stuff action) and restores the counters to the desired four-count offset.

(1) Write address counter U31 is a binary counter that is clocked by the write clock output of U2 (nominal 576 kHz rate) that is inverted by U35-2. The counter sequentially generates 3-bit binary addresses for serially entering data bits into elastic storage register U8 ((3) below). The MSD output also goes to the J-K inputs of rate comparator flip-flop U23-6 ((4) below).

(2) Read address counter U15 also sequentially generates 3-bit binary addresses, but for serially accessing data bits from elastic storage register U8. Each coincidence of TCHAN and TCLK pulses (coincidences occur at a nominal 576.563 kHz rate), unless inhibited by TCHN, increments the counter. TCHAN and TCLK highs appear at counter pins U15-10 and U15-2, respectively, when it is that (channel A) group's turn to output a data bit to the MO/C card. If read counter U15 lags write counter U31 by less than four counts, rate comparator flip-flops U23-6 ((4) below) detects this condition and produces RCOM, requesting that a stuff action be performed. The stuff request circuits on MO/C card 21A4 recognize this condition and cause TC (M) card 21A5, at the proper time, to put TCHN low, inhibiting U15 from incrementing for one coincidence of TCHAN and TCLK. This action (stuffing) can occur at a maximum rate of once per major frame for each group. Stuff actions are performed, as necessary, to maintain the desired four-count offset between the counters. The MSD output also goes to the clock input of rate comparator flip-flop U23-6.

(3) Elastic storage register U8 temporarily stores its asynchronous data input for synchronous output as group data (GRP) to MO/C card 21A4. The register's data bits may represent group data or activity or dummy patterns from input selector U2 (table 2-4). Counter U31 write addresses at pins U8-15, U8-14, and U8-13 sequentially address register bit storage cells 1 through 8 for serial clock-in of the data. Counter U15 read addresses (delayed four clock periods) appear at read input pins U8-1, U8-2, and U8-3 and sequentially access register cells 1 through 8. This read-out activity serially transfers the register's data bits onto the GRP line.

(4) Rate comparator flip-flop U23-6 provides write/read counter status to MO/C card 21A4. The status output is a low (logic 0) on the RCOM line when write and read address counters U31 and U15 are offset four counts. The status output is a high (logic 1) when the counters merge within less than four counts, and stuffing is required to restore a four-count offset. Every eighth count of U15 produces a positive transition at U15-12 to clock flip-flop U23-6 and enters the output level of U31-5 into the flip-flop. If U15 and U31 are offset four counts, U31-5 will be low when a positive transition occurs and flip-flop U23-6 will be reset (or remain reset) (RCOM logic 0 out). Conversely, if the offset of the two counters has decreased to less than four counts, U31-5 will be high when a positive transition occurs and flip-flop U23-6 will be set (or remain set) (RCOM logic 1 out). The RCOM high, processed through MO/C card 21A4's stuff request circuits, initiates a TCHN low (stuff command) from TC (M) card 21A5. The TCHN low restores the read/write counters' offset to four counts ((2) above).

2-28. Output Section Theory of Operation

(fig. FO-6)

a. Introduction. This paragraph describes the detailed operation of an output section on DGP card 21A6. Each DGP card has functionally identical output sections designated channel A and channel B. Channel A sections of DGP cards No. 1 through No. 4 individually process outgoing data for groups 1, 2, 3, and 4. Channel B sections of the same cards individually process outgoing data for groups 5, 6, 7, and 8. Only the channel A output section theory of operation is discussed as typical. The theory of operation is divided into four functional descriptions established in the output section block diagram discussion, as listed below.

(1) Destuff gate (*b* below).
(2) Output selector (*c* below).
(3) Output rate buffer (*d* below).
(4) Output logic (*e* below).

NOTE

The sheet number references in *b* through *e* below refer to figure FO-6.

b. Destuff Gate. Three-input AND gate U29-12 (sheet 3) controls application of receive clock (RCLK—) pulses that ultimately increment write address counter U10-6 (*d*(1) below) for group data processing. A receive channel clock (RCHN) high at pin U29-1 conditions the gate only when it is channel A's turn to extract a group data bit from the incoming SG data stream. A receive channel clock delete (RCHN) low at pin U29-13 inhibits the gate for one coincidence of RCHAN and RCLK— when a destuff action is to be performed; RCHN is high when destuffing is not required. Coinciding RCHAN and RCHN highs let U29-12 pass and restore RCLK— pulses. TC (D) card 21A5 supplies the three inputs to the destuff gate. The TC (D) card's destuff circuits put RCHN low in response to periodic RDLTTY high from FS card 21A7's destuff detection circuits. Each RCHN low inhibits passage of one RCLK— write clock to output selector U17. These clock delete actions are the inverse of the stuffing actions taken by the far-end multiplexer section. RCHN is low only for the first bits (96-channel operation) or first 4 bits (48-channel operation of minor frame 0; thus, only the first bit of a frame, for a given group, is deleted when necessary.

c. Output Selector. Output selector U17 (sheet 3) operates like input selector U2 described in paragraph 2-27*d*. One four-input multiplexer section of U17 selectively routes SG data (SDATA) or 7-bit activity patterns to the input rate buffer's elastic storage register U9. The other section routes the related timing (U29-12 output or 576 KHZ 2) to clock U9. At the same time, it routes the selected clock's complement to write address counter U10-6. Card-mounted switch S1 ON/OFF levels and a receive major frame sync (RMSYNC—) input from FS card 21A7 control U17's data and clock routing. U17 receives its activity patterns and 576 KHZ 2 clock signals from inverters U16-8 and U16-10, respectively (para 2-27*c*). Output selector U17's four select input level combinations and the corresponding data and clock outputs are listed in table 2-5.

Table 2-5. Output Selector U17 Operating Conditions

Select inputs		U17 inputs selected for routing to output rate buffer	
Pin U17-13 (RMSYNC—)	Pin U17-13 (S1, ACT)	Pin U17-15 output (selected data)	Pin U17-1 output (selected clock)
0	0	Activity pattern (pin U17-12 input).	576 KHZ 2 (pin U17-4 input).
1	0	SDATA (pin U17-11 input).	Gated RCLK— (pin U17-5 input).
0	1	Activity pattern (pin U17-10 input).	576 KHZ 2 (pin U17-6 input).
1	1	Activity pattern (pin U17-9 input).	576 KHZ 2 (pin U17-7 input).

d. Output Rate Buffer. The output rate buffer extracts the corresponding group's data from the incoming SG data stream at a clock rate derived from the data. Output selector U17 (sheet 3) routes the SG data (SDATA) and extracted clock (gated RCLK—) signals to elastic storage register U9, and the gated RCLK clock to write address counter U10-6 (table 2-5). Each time it is the group's turn to extract a data bit, the write counter addresses one of register U9's eight bit storage cells; a gated RCLK— positive transition enters a data bit into the addressed cell. In this manner, the write counter sequentially addresses register U9 bit cells for entry of group data bits by gated RCLK— positive transitions. The gated clocks from U29-12 are not spaced at regular intervals, especially if a clock is inhibited (destuff operation performed (*b* above)). Thus, write counter U10-6 and register U9 are clocked by what could be termed a stuttering clock. However, the average rate of the stuttering clock is the same as the group data rate contained in the SG (nominal 576 kHz). Read address counter U10-8 is slaved to the write address counter through a phase-locked loop whose function is to smooth the stuttering effect and clock the read counter at the average rate of the write counter. A voltage-controlled oscillator (VCO) provides the smooth clock to the read counter. The VOC is part of the phase-locked loop and slowly and smoothly varies the read clock frequency as the phase relationship of the count 8 output of the write and read counters varies. A phase comparator translates the phase differences of the counters into positive and negative pulses at 16-count intervals. Pulse widths represent the amount of phase difference; pulse polarities indicate the direction of phase shift. An RC network responds to these intermittent pulses by slowly raising or lowing a dc control voltage it supplies to the VCO. The VOC responds by slowly increasing or decreasing its read clock output frequency rate. This activity smooths out the effect of the stuttering clocks from U29-12. While the read counter's clock rate varies, its rate is exactly the same as the rate of the data inputted by that group to the far-end multiplexer section. The VCO smooth clock increments the read counter's address outputs that serially access group data bits from U9. The data bits go through an output logic level shifter to an output group data jack on the rear of the TD-976/G. The VCO smooth clock also triggers an output timing pulse generator (one-shot) that provides a timing signal through a level shifter to an output group timing jack on the rear of the TD-976/G. The varying (smoothed) data and timing rates are acceptable to group level interfacing equipments.

(1) Write address counter U10-6 (sheet 3) is a binary counter that is clocked by negative transitions. The selected write counter clock from pin U17-1 is inverted by U35-4 and applied to U10-6. The counter's 2^0 (pin U10-3), 2^1 (pin U10-4), and 2^2 (pin U10-5 inverted through U16-12) outputs sequentially address elastic storage register U9's bit storage cells. The complement of the selected clock enters data bits into the addressed cells. Inverter U16-12 on the write counter's 2^2 output imparts the desired four-count offset between the write addresses and read addresses applied to the elastic storage register. By inverting the 2^2 (count 4) output, U16-12 converts the write counter's actual 0,1,2,3,4,5,6,7 (binary 000 through 111) count-

ing sequence to a 4,5,6,7,0,1,2,3 (binary 001 through 111 and then 000 through 110) address count sequence at register U9's write input pins. The write counter's 2^3 (pin U10-6) output goes to a phase detector ((4)(*a*) below), where its phase is compared with the read counter's 2^3 output phase for VCO frequency control.

(2) Read address counter U10-8 (sheet 3) generates 3-bit binary read addresses that sequentially access data bits from elastic storage register U9. A clock from the phase-locked loop ((4)(*a*) below) increments the counter. The counter's 2^0 (pin U10-11), 2^1 (pin U10-10), and 2^2 (pin U10-9) read address outputs go directly to one set of register U9's read inputs. The read address counter's 2^3 (pin U10-8) output goes to the phase-locked loop.

(3) Elastic storage register U9 (sheet 3) operated like the input section's elastic storage register U8 (para 2-27*e*(3)). U9 receives its selected data and clock inputs from output selector U17. Write address counter U10-6 write addresses sequentially select U9's eight bit storage cells for entering the group's data bits by the selected clock's positive transitions. Four clock periods later, corresponding addresses from read address counter U10-8 sequentially access the data bits from U9's bit cells. The accessed data bits go out through pin U9-4 to J-K inputs of data buffer flip-flop U34-6 (*e*(3) below). Register U9's selected clock pulses coincide with the group's data bits that appear at data input pin U9-12. By entering only these bits into U9's cells, the selected clock pulses continually extract the group's incoming data. When channel A is inactive (switch S1 is placed to OFF), or if the demultiplexer section is unable to acquire major frame sync, the 576 KHZ 2 clock pulses enter activity pattern bits into register U9. This action keeps the phase-locked loop operating at its nominal 576 kHz rate.

(4) The phase-locked loop slaves read counter U10-8 to write counter U10-6 by providing a slowly changing smooth clock output that tracks the average rate of the write counter. VCO U7 (sheet 5) generates the smooth clock. Phase comparator U5 controls the VOC's output frequency rate by means of an RC network. A fast acquisition circuit increases the phase-locked loop's ability to lock to the input write clocks upon equipment power turn-on or after a power interruption.

(*a*) Phase comparator U5 (sheet 5) monitors the positive transitions of the 2^3 (count 8) outputs of the write address and read address counters ((1) and (2) above). When the two inputs are exactly in phase (A, fig. 2-12), the phase comparator, a three-state device, opens its pin U5-13 output and presents an infinite impedance to the RC network that it controls. With the control line open, the RC network remains at the level to which its capacitor has charged or discharged. If the read counter's 2^3 output lags (occurs later than) the write counter's 2^3 output (B, fig. 2-12), U5 outputs +10 v amplitude pulses at 16-count (read clock period) intervals. The width of each positive pulse indicates the read counter's real-time phase lag. Conversely, if the read counter's 2^3 output leads (occurs earlier than) the write counter's 2^3 output (C, fig. 2-12), U5 reverses its output pulse polarity to 0 v (ground) at 16-count intervals. The width of each 0v pulse indicates the read counter's real-time phase lead. A three-state buffer within the phase comparator provides the output pin U5-13 +10 v pulses, 0 v pulses (grounds), and intervening opens. A 22-megohm resistor (R23) couples the pin U5-13 output to the RC network. In summary, U5 translates the read and write counters' operating phase differences into periodic positive or negative pulses that the RC network converts to a slowly varying dc voltage for control of VCO U7.

(*b*) R28, C18, C19 is a high-frequency filter that removes the switching transitions of the pulses applied through R23 and develops the VCO control voltage that is applied to pin U7-9. Two basic examples of VCO control voltage are shown in figure 2-12 In the first example, the two counters start out in phase, but the write counter is being clocked at a slightly faster instantaneous rate and advances on the read counter. In this case, the phase comparator outputs narrow-width +10 v amplitude pulses that cause the VCO control voltage to gradually increase. This action continues until the read counter catches up and the two counters are once again in phase with each other (width of phase comparator pulses will become progressively narrower as read counter starts to catch up). In the second example, the read counter is leading the write counter (this situation could occur when a destuff operation was accomplished). In this case, the phase comparator outputs narrow-width 0 v pulses that cause the VCO control voltage to gradually decrease. This action continues until the read counter has been slowed to the point where it is once again in phase with the write counter. The +5 v nominal voltage is representative of a nominal VCO output of 576 kHz. Variable resistor R45 is a depot adjustment. R45 is adjusted to center the output of U7 when U5 is producing an average ac switching output.

(*c*) VCO U7 varies the read clock and output timing clock frequency as its VCOIN pin U7-9 voltage varies. A nominal +5 v input sets the VCO's pin U7-4 output frequency at a nominal 576 kHz. Higher and lower input voltages increase and decrease the output frequency, respectively. Nominal extremes are a +5.33 v input that increase the VOC's output frequency to about 590 kHz, and a +4.64 v input that decreases it to about 560 kHz. The pin U7-4 output goes through buffer/converter U11-10 and backplane jumper DGPCT0X to read address counter U10 (*d*(2)

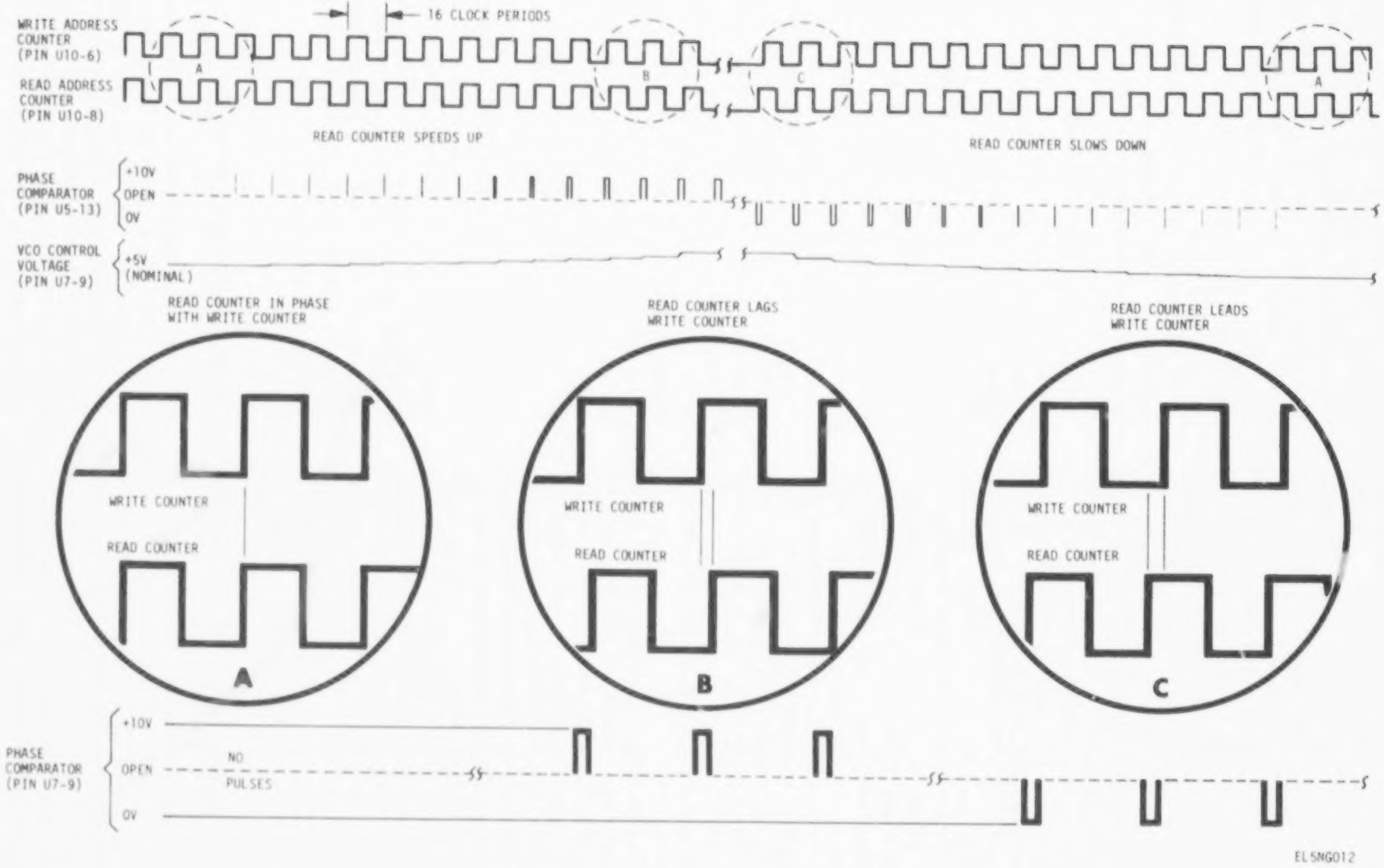

WRITE ADDRESS COUNTER (PIN U10-6)
READ ADDRESS COUNTER (PIN U10-8)
16 CLOCK PERIODS
A
B
C
A
READ COUNTER SPEEDS UP
READ COUNTER SLOWS DOWN
PHASE COMPARATOR (PIN U5-13)
+10V
OPEN
0V
VCO CONTROL VOLTAGE (PIN U7-9)
+5V (NOMINAL)
READ COUNTER IN PHASE WITH WRITE COUNTER
READ COUNTER LAGS WRITE COUNTER
READ COUNTER LEADS WRITE COUNTER
WRITE COUNTER
READ COUNTER
WRITE COUNTER
READ COUNTER
WRITE COUNTER
READ COUNTER
A
B
C
PHASE COMPARATOR (PIN U7-9)
+10V
OPEN
0V
NO PULSES
EL5NG012

Figure 2-12. DGP card 21A6 output section read clock smoothing, typical waveforms.

above) and to timing pulse generator U27 (*e*(1) below).

(*d*) The fast acquisition circuit consists of dual analog switch U13 (sheet 5) and its controlling RC circuit R39, R40, C26, CR5. The RC circuit monitors equipment + 12 v power and closes U13's two switches for a brief time when + 12 v rises to its operating level. The fast acquisition circuit operates upon equipment power turn-on. It also recycles after each power interruption that is long enough for the + 12 v supply to drop below + 9 v. Initially, C26 couples a power turn-on + 12 v rise through R39 to pins U13-12 (for channel A) and U13-13 (for channel B). The positive voltage immediately closes the switches. Closure of the pins U13-10 to U13-11 switch parallels lower value (2.7 kilohms) resistor R27 with 22-megohm resistor R23. This greatly reduced resistance path for the output of U5 causes the RC network (R28, C18, C19) to respond at a much faster rate. This accelerated response rapidly increases or decreases the output frequency of U7 to reduce the phase difference between read and write address counters. The negative side of C26 differentiates to ground through R40 as the capacitor charges up to + 12 v. The ground (low) opens U13's switches, disconnects R27 and R23, and restores the RC network to its normal slow-response operating configuration. Any subsequent power interruption lets C26 quickly discharge through CR5 to ground. Restoration of equipment power and rise of + 12 v reactivates the fast acquisition circuit in the same manner as after power turn-on.

(*e*) Voltage regulator Q9,VR2 (sheet 5) maintains phase comparator U5 and VCO U7 V_{CC} power at + 10 v. Zener diode VR2 regulates Q9's biasing voltage at + 10 ± 1 v. Capacitor C24 filters the base voltage to maintain the Q9 emitter at 10 v even though the collector + 12 v level may vary. Zener diode VR3 provides + 12 v overvoltage protection for U5 and U7 in the event of voltage regulator failure.

e. Output Logic. A data buffer flip-flop, a timing pulse generator (one-shot), and two level shifters comprise the output logic. The output of the one-shot shifts group data bits through the flip-flop to provide group output data and timing that are aligned with each other. The level shifters convert TTL level data and timing outputs to NRZ TD-660/G compatible levels.

(1) Timing pulse generator U27-5 (sheet 3) generates complementary 100-nanosecond duration pulses in response to negative transitions of the phase-locked loop at its trigger pin U27-9. The pin U27-5 positive pulses go to data buffer flip-flop U34-6 ((3) below) and to GTM card 21A2 as output group timing (OGRP(CH A)T). The pin U27-12 negative pulses go to level shifter Q2,Q3.

(2) Timing pulse level shifter Q2,Q3 (sheet 3) converts the TTL negative-going pulse output of U27-12 to TD-660/G compatible levels. Each TTL low from U27-12 biases Q2 off and the resulting − 4.4 v on the base of Q3 biases Q3 on. With Q3 on, the output group timing (OGRP(CH A)TM) line is at approximately 0 v. Conversely, when U27 times out, pin U27-12 goes high and biases Q2 on. Q2 switch-on puts the R7, R11, CR2 junction at about + 0.7 v (diode junction drop) and switches Q3 off. Q3 switch-off lowers its collector to about − 2.2 v when the level shifter's output is loaded (connected by a transmission of a down-link TD-660/G). The − 2.2 v level is developed at the junction of a two-resistor voltage divider between − 4.4 v and ground. The level shifter's 91-ohm resistor R10 between card pin 87 and − 4.4 v is one-half of the voltage divider. A corresponding 91-ohm resistor at the input of the receiving TD-660/G is the grounding half of the voltage divider.

(3) Data buffer flip-flop U34-6 (sheet 3) receives data at its J-K input pins from elastic storage register U9. Positive transitions of the pulse output from U27-5 clock the group data bits into and through U34. The flip-flop provides a pin U34-6 output group data (OGRP(CH A)D) signal to GTM card 21A2. It also provides a pin U34-7 complementary output to data level shifter Q1,Q4.

(4) Data level shifter Q1,Q4 operates like the timing pulse level shifter ((2) above). When U34 contains a logic 1, pin U34-7 output is low, turning Q1 off and Q4 on. This places the output group data (OGRP(CH A)) line at about 0 v. Conversely, when U34 contains a logic 0, its pin U34-7 output is high, turning Q1 on and Q4 off. This places the output group data line at about − 2.2 v.

Section VIII. DIGITAL VOICE ORDERWIRE (DVOW) CARD 21A11

2-29. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the DVOW card. There is one DVOW card (21A11) in the TD-976/G. The DVOW card has two functional sections: An encoder section and decoder section. The encoder section converts voice analog signal inputs to a digital voice orderwire data output for insertion into the outgoing SG data stream. The decoder section extracts digital voice orderwire data from the incoming SG data stream and converts the data back to voice analog signals. The encoder and decoder block diagram discussions in paragraphs 2-30 and 2-31 are based on the encoder and decoder block diagrams in figures 2-13 and 2-14. The detailed theory of operation in paragraphs 2-32 and 2-33 is based on the DVOW card schematic diagram in figure FO-7.

2-30. Encoder Section Block Diagram Discussion

(fig. 2-13)

a. General. The encoder section receives audio signals from remote, extension, and local handsets, encodes these signals into digital voice data, and synchronously shifts the data bits out for insertion in the outgoing SG data stream. The encoder section block diagram discussion is divided into functional descriptions of the input circuits (*b* below), the CVSD encoder (*c* below), and the timing selection circuits (*d* below).

b. Input Circuits. An extension input circuit and a two-stage filter/amplifier condition the voice audio inputs for application to the continuously variable slope delta (CVSD) encoder.

(1) Transformer T1 in the extension input circuit couples a digital voice extension input (DVEXI) to the two-stage filter/amplifier. DVEXI is applied through the RAU from an extention input. Resistor R5 matches T1 impedance to the 600-ohm DVEXI input. Adjustment of R6 sets the output of T1 to the two-stage filter/amplifier. Variable resistor R3 sets the level of a digital voice microphone (DVMIC) input audio signal applied to the filter/amplifier. DVMIC originates at a handset connected to either the front panel or the RAU and comes in from AVOW card 21A10. Resistor R4 attenuates the digital voice ring signal (DVRNGS) (1600 Hz tone). AVOW card 21A10 generates DVRNGS when an outgoing system orderwire call is initiated at the front panel or the RAU.

(2) Two-stage filter/amplifier U22 is a low-pass filter that limits the band of frequencies that are passed to the CVSD encoder. The second stage filtered audio output goes through scaling resistor R13 to a summing point at one input of comparator U24.

c. CVSD Encoder. The CVSD encoder's functional circuits convert summed filtered audio and dc signals to digital patterns from which the audio signals can be reconstructed (decoded) at a far-end TD-976/G. Comparator U24 encoded digital levels are used to control up and down integrators whose outputs are fed back for delta error modulation of comparator U24's sum input. The digital patterns produced by the delta error modulation are synchronously shifted through output data buffer U27 to MO/C 21A4 for bit-by-bit insertion into the outgoing SG data stream. The delta error modulation signal consists of up and down integration voltage segments superimposed on a dc level that undulates at the filtered audio frequency. This combined signal represents reconstructed audio derived from the comparator's digital output. A filtered dc level, which is also derived from encoded digital pattern control of up and down integrators, is applied through scaling resistor R17 to the summing point at the input to comparator U24. U24 continually compares its sum (filtered audio plus filtered dc) input with the reconstructed audio (delta error) input. A delta error level below the sum level drives the comparator's output high (logic 1 out). A delta error level above the sum level drives the comparator's output low (logic 0 out). Comparator logic 1 and 0 outputs ultimately reverse the delta error voltage upward and downward integration transitions to correct the error difference. Each such reversal heads the delta error voltage toward the sum level and progressively reduces the error to zero (delta error voltage level same as sum level). However, since a delta error transition can be reversed only at a clock positive transition, it invariably crosses the sum level and builds an opposite polarity error difference before being reversed. This overshoot operating feature maintains a continuously varying slope delta (CVSD) level whose transitions coarsely follow the sum (filtered audio plus filtered dc) signal. The CVSD encoder outputs a logic 1 DVOWI bit for each clock period that the sum level exceeds the delta error level, and outputs a logic 0 for each clock period that the delta error level exceeds the sum level.

(1) Comparator U24 compares the sum input at its noninverting (+) input with the delta error (reconstructed audio) input at its inverting (−) input. U24 puts its digital output high when the (+) input is above the (−) input and low when the (+) input is below the (−) input.

(2) The digital output of comparator U24 is serially clocked into the 3-bit shift register. In 96-channel operation, the clock is derived from the transmit digital voice orderwire clock (TDVOW), while in 48-channel operation, the clock is derived from the transmit digital voice orderwire smooth clock (TDVOWC—). In each case, the clock is homogenous (nearly evenly spaced) and at a nominal rate of 57.656 kHz (DVOW sampling rate, as shown in figures 2-3 and 2-4). The register's first stage provides a true output to output data buffer U27, and complementary outputs to decoder U21.

(3) Output data buffer U27 consists of a J-K flip-flop that synchronously shifts the 3-bit shift register's first stage data output to the MO/C card for insertion into the outgoing SG. U27 is clocked by a gated TDVOW clock (time for a bit of DVOW information to be inserted in the SG) occurring at a 57.656 kbps rate.

(4) Decoder U21 monitors the 3-bit shift register for 3 consecutive matching logic bits (111 or 000). All 111 match denotes that the delta error level has remained below the sum level for three clock periods. A 000 match denotes that the delta error level has remained above the sum level for three clocks periods. Upon detecting either of the 3-bit match conditions, the decoder produces a boost enable output to control

inverters for the up and down integrators. Inverted and restored through U28-4 and U19-8, the boost enable high steepens the up integrator's rising slope voltage output. At the same time, a boost enable low from inverter U19-6 steepens the down integrator's falling slope voltage output. Steepening of either slope forces the delta error level to cross a steep high frequency or amplitude sum level sooner.

(5) The up and down integrators normally provide +5 v/+9 v and +4 v/0 v integration voltage outputs, respectively, to dual sections of switch U26. During a boost condition, the up integrator operates between +5 v and +9 v, while the down integrator operates between +4 v and 0 v. Inverters U19-8 and U19-6 control the normal and boost operating ranges by changing the voltage on each integrator's three-resistor voltage divider. The applied voltage levels establish a capacitor's integrating speed and the level to which it can charge (integrate) or discharge (differentiate).

(6) Switch U26 has two pairs of switches that are controlled by 1's and 0's from the 3-bit shift register's first stage. One switch pair (A and D) simultaneously routes up integration and down integration voltages to the dc filter and the reference filter, respectively. The other switch pair (B and C) simultaneously routes down and up integration voltages to the dc filter and the reference filter, respectively. When a logic 1 is stored in the first stage of the register, U19-3 will be high, closing switches B and C. Conversely, a logic 0 stored in the first stage of the register will cause U19-11 to be high, closing switches A and D.

(7) DC filter C18, R14 maintains a nominal dc level of the up and down integration voltages applied to it through switch U26. The dc level slowly decreases as the filtered audio input to comparator U24 rises. The dc level also slowly rises as the filtered audio input drops. The varying dc output level effectively offsets the filtered audio signal that is summed with it at the comparator's (+) input pin. Because of scaling resistors R13 and R17, the dc level only offsets (slightly lowers or raises) the filtered audio level closer to the reconstructed audio (delta error) level at the comparator's (−) input pin. The dc level offsets the filtered audio level about 10 percent.

(8) Reference filter C19, R15 reconstructs an audio analog signal from the up and down integration voltages switched to it. Durations of the up and down integration voltages vary according to the consecutive number of 3-bit shift register logic 1's and 0's that indirectly switched them to the filter. Longer strings of 1's than 0's progressively charge capacitor C19 positive; longer strings of 0's than 1's discharge the capacitor. By alternately charging and discharging in response to up and down integration voltage segments, filter C19, R15 coarsely follows or traces the audio signal. The filter's reconstructed audio output goes to comparator U24's (−) input.

d. Timing Selection Circuits. The timing selection circuits selectively gate appropriate timing clocks to the output data buffer and the 3-bit shift register.

(1) Coincidences of transmit clocks (TCLK) and transmit digital voice orderwire clocks (TDVOW) create gated TDVOW clocks (time during which a bit of DVOW information will be inserted into the outgoing SG). The gated TDVOW clock always clocks the output data buffer, and in 96-channel operation, is routed through the clock selector to clock the 3-bit shift register.

(2) Coincidences of transmit clocks (TCLK) and transmit digital voice orderwire smooth clocks (TDVOWC—) create gated TDVOWC— clocks, which, in turn 48-channel operation, are selected by the clock selector to clock the 3-bit shift register. The gated TDVOWC— clocks are homogenous (nealy evenly spaced).

2-31. Decoder Section Block Diagram Discussion

(fig. 2-14)

a. General. The decoder section synchronously extracts digital voice data information from the incoming SG data stream, converts it to a reconstructed audio analog signal, and then filters it for output to remove, extension, and local handsets. A ring detector circuit, upon detecting a ring tone audio signal, causes the SYSTEM CALL indicators on the front panel and the RAU to light. The decoder section block diagram discussion is divided into functional descriptions of the timing selection circuits (*b* below), the input data buffer (*c* below), the CVSD decoder (*d* below), the output circuits (*e* below), and the ring detector circuits (*f* below).

b. Timing Selection Circuits. The decoder's timing selection circuits operate in the same manner as the encoder's timing selection circuits (para 2-30*d*), except that receive clock inputs are used. A gated RDVOW clock synchronously operates the input data buffer to extract DVOW data bits from the SG data (SDATA) line. the gated RDVOW clock also operates the 3-bit shift register through clock selector U33 during 96-channel operation. A gated RDVOWC— (smooth) clock operates the register through U33 during 48-channel operation.

c. Input Data Buffer. The input data buffer extracts DVOW data bits from the SDATA stream at a 57.656 kbps rate and provides the DVOW data to the 3-bit shift register.

d. CVSD Decoder. The CVSD decoder converts DVOW data input patterns into a reconstructed audio analog signal, and then filters it into a clean audio signal for output to remote, extension, and local handset earphones.

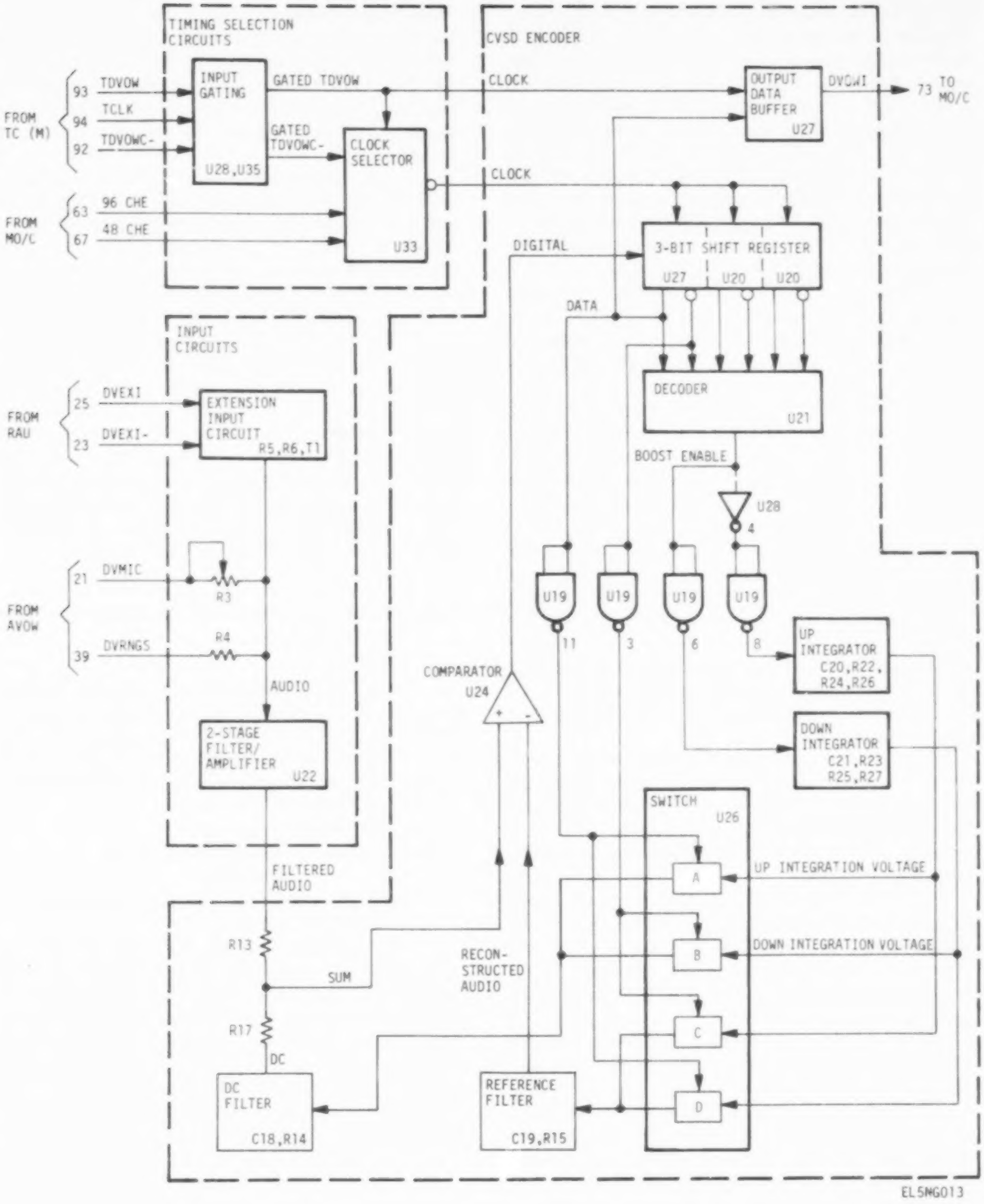

TIMING SELECTION CIRCUITS
CVSD ENCODER
FROM TC (M)
93
TDVOW
94
TCLK
92
TDVOWC-
INPUT GATING
U28,U35
GATED TDVOW
GATED TDVOWC-
CLOCK SELECTOR
U33
CLOCK
OUTPUT DATA BUFFER
U27
DVOWI
73
TO MO/C
FROM MO/C
63
96 CHE
67
48 CHE
CLOCK
DIGITAL
3-BIT SHIFT REGISTER
U27
U20
U20
DATA
DECODER
U21
INPUT CIRCUITS
FROM RAU
25
DVEXI
23
DVEXI-
EXTENSION INPUT CIRCUIT
R5,R6,T1
BOOST ENABLE
U28
4
FROM AVOW
21
DVMIC
R3
39
DVRNGS
R4
AUDIO
U19
U19
U19
U19
11
3
6
8
UP INTEGRATOR
C20,R22,R24,R26
COMPARATOR
U24
+
-
2-STAGE FILTER/ AMPLIFIER
U22
DOWN INTEGRATOR
C21,R23 R25,R27
SWITCH
U26
FILTERED AUDIO
A
UP INTEGRATION VOLTAGE
R13
B
DOWN INTEGRATION VOLTAGE
SUM
RECON- STRUCTED AUDIO
R17
C
DC
DC FILTER
C18,R14
REFERENCE FILTER
C19,R15
D
EL5NG013

Figure 2-13. DVOW card 21A11 encoder section, block diagram.

(1) Except for gated receive instead of gated transmit clock inputs, the decoder's 3-bit shift register operates in the same manner as the encoder's 3-bit shaft register (para 2-30c(2)). The decoder's 3-bit shift register first stage provides complementary outputs to switch U12 control inverters U5-6 and U5-3. All three stages provide complementary outputs to decoder U6, U34. A receive major frame sync level 8 (SYNC 8-) signal presets the shift register to 100 when the TD-976/G is midway through its major frame sync acquisition sequence. This preset action allows time for CVSD decoder circuit preconditioning (nulling) before audio subsequently arrives.

(2) Decoder U6, U34 monitors the 3-bit shift register for three consecutive matching logic 1's or 0's. The decoder controls up and down integrators through inverters in the same manner as decoder U21 (para 2-30c(4)).

(3) The decoder's up and down integrators operate in the same manner and at the same normal and boost voltages as the encoder's integrators (para 2-30c(5)). The up integrator supplies its integration voltage to switch C of U12. The down integrator supplies its integration voltage to switch D of U12.

(4) Only two switches (C and D) of U12 are used in the decoder; also, only one switch is closed at any one time. The logic 1's and 0's passing through the first stage of the 3-bit shift register control U12's switches through inverters U5-6 and U5-3. A logic 1 closes switch C and passes an up integration voltage to the audio reconstructor. Conversely, a logic 0 closes switch D and passes a down integration voltage to the audio reconstructor.

(5) Audio reconstructor R37, C23 is a switching transients filter that is exactly the same as the encoder's reference filter (para 2-30c(8)). The reconstructor serially assembles the up and down integration voltages switches to it into a coarse reconstructed audio analog signal.

(6) Filter/amplifier U8 filters out up and down integration voltage transitions from the reconstructed audio signal. Filter C32-C34, L1 provides additional filtering to produce an output audio signal that closely resembles the original audio signal encoded by the sending TD-976/G.

e. Output Circuits. The output circuits condition the filtered audio for output to separate handset earphones.

(1) Gain amplified U17-1 provides an amplified audio signal to output transformer T2. Variable resistor R57 sets the amplifier's driving gain. Fixed resistor R62 matches T2's impedance to the digital voice extension output (DVEXO and DVEXO—) lines. DVEXO goes through the RAU to an extension handset earphone.

(2) Gain amplifier U17-9 provides an amplified digital voice earphone (DVEAR) output to AVOW card 21A10. The AVOW card routes the audio signal to a handset plug-in jack on the front panel and the RAU. Variable resistor R59 sets the amplifier's driving gain.

f. Ring Detector Circuits. A ring detector and a ring detector latch operate to light CALL indicators and sound an audible alarm when a ring tone appears on the input audio.

(1) The ring detector's 2-stage filter U15 passes a 1600 Hz ring tone frequently and attenuates higher and lower frequencies. When a ring tone comes in and appears at the filter's second stage output, diode CR1 applies its positive half-cycles to a charge delay RC circuit (R48, C29). Upon charging positive, the RC circuit switches transistor Q1 on, creating the set output.

(2) The ring detector's set output sets the ring detector latch each time a ring tone is detected. The latch-set action puts the latch's digital voice call (DVCAL—) output low to AD card 21A1. The AD card responds by causing the SYSTEM CALL indicators on the front panel and the RAU to light. The AD card also causes the audible ALARM horn on the front panel to sound. The latch remains set until a switch-activated local or remote digital talk/listen (LDTL— or RDTL—) signal from the front panel or the RAU resets it.

2-32. Encoder Section Theory of Operation

(fig. FO-7)

a. General. This paragraph describes the detailed operation of the circuits in the encoder section on DVOW card 21A11. The theory of operation is divided into the three functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Input circuits (*b* below).
(2) CVSD encoder (*c* below).
(3) Timing selection circuits (*d* below).

NOTE

The sheet number references in *b* through *d* below refer to figure FO-7.

b. Input Circuits (sheet 2). The input circuits provide impedance matching, level setting, and audio bandpass filtering for applied analog signals. These input signals include a ring tone and two voice audio signals. The three audio analog inputs are applied to a two-stage bandpass filter that passes a limited band of audio frequencies to the CVSD encoder.

(1) Transformer T1 couples digital voice extension input (DVEXI and DVEXI—) signals from the DGTL VO XMT jack on the RAU through variable resistor R6 to filter input pin U22-7. R6 is normally adjusted for a 700-millivolt peak-to-peak audio input to the filter. Resistor R5 across the T1 secondary winding matches the 1:1 transformer's impedance to the 600-ohm DVEXI input line.

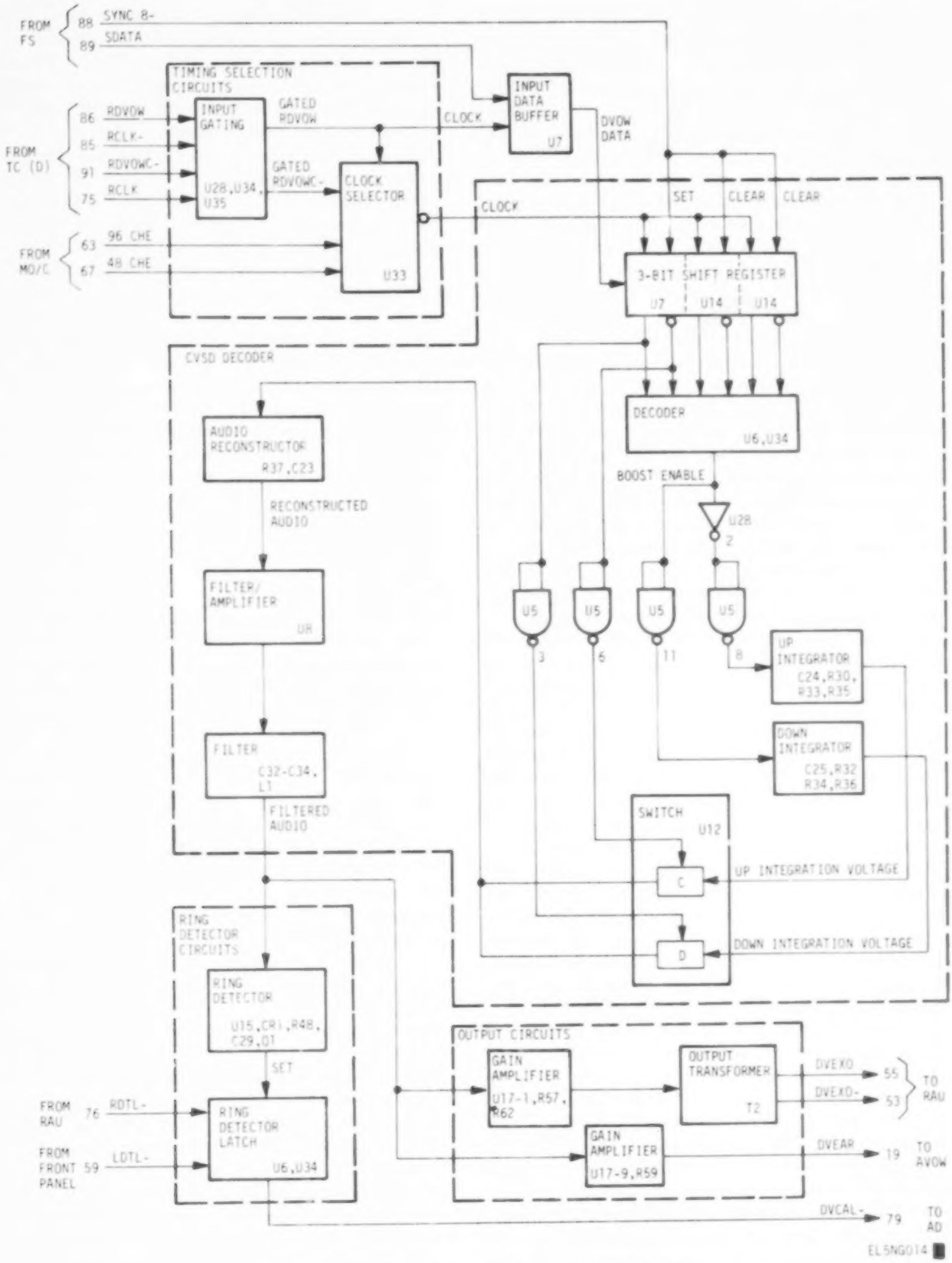

FROM FS
88 SYNC 8-
89 SDATA
TIMING SELECTION CIRCUITS
FROM TC (D)
86 RDVOW
85 RCLK-
91 RDVOWC-
75 RCLK
INPUT GATING U28,U34, U35
GATED RDVOW
GATED RDVOWC-
CLOCK SELECTOR U33
FROM MD/C
63 96 CHE
67 48 CHE
CLOCK
INPUT DATA BUFFER U7
DVOW DATA
SET
CLEAR
CLEAR
CLOCK
3-BIT SHIFT REGISTER
U7
U14
U14
CVSD DECODER
DECODER U6,U34
BOOST ENABLE
U28 2
U5
U5
U5
U5
3
6
11
8
UP INTEGRATOR C24,R30, R33,R35
DOWN INTEGRATOR C25,R32 R34,R36
AUDIO RECONSTRUCTOR R37,C23
RECONSTRUCTED AUDIO
FILTER/ AMPLIFIER U8
FILTER C32-C34, L1
FILTERED AUDIO
SWITCH U12
C
D
UP INTEGRATION VOLTAGE
DOWN INTEGRATION VOLTAGE
RING DETECTOR CIRCUITS
RING DETECTOR U15,CR1,R48, C29,Q1
SET
RING DETECTOR LATCH U6,U34
FROM RAU 76 RDTL-
FROM FRONT PANEL 59 LDTL-
OUTPUT CIRCUITS
GAIN AMPLIFIER U17-1,R57, R62
OUTPUT TRANSFORMER T2
GAIN AMPLIFIER U17-9,R59
DVEXO 55
DVEXO- 53
TO RAU
DVEAR 19 TO AVOW
DVCAL- 79 TO AD
EL5NG014

Figure 2-14. DVOW card 21A11 decoder section, block diagram.

(2) Variable resistor R3 couples and level sets a digital voice microphone (DVMIC) signal to filter input pin U22-7. DVMIC comes in through AVOW card 21A10 from a local handset plugged into the VOICE O.W. HANDSET jack on the front panel or a handset plugged into the handset jack on the RAU. R3 is normally adjusted to set the DVMIC signal level at about 700 millivolts peak to peak.

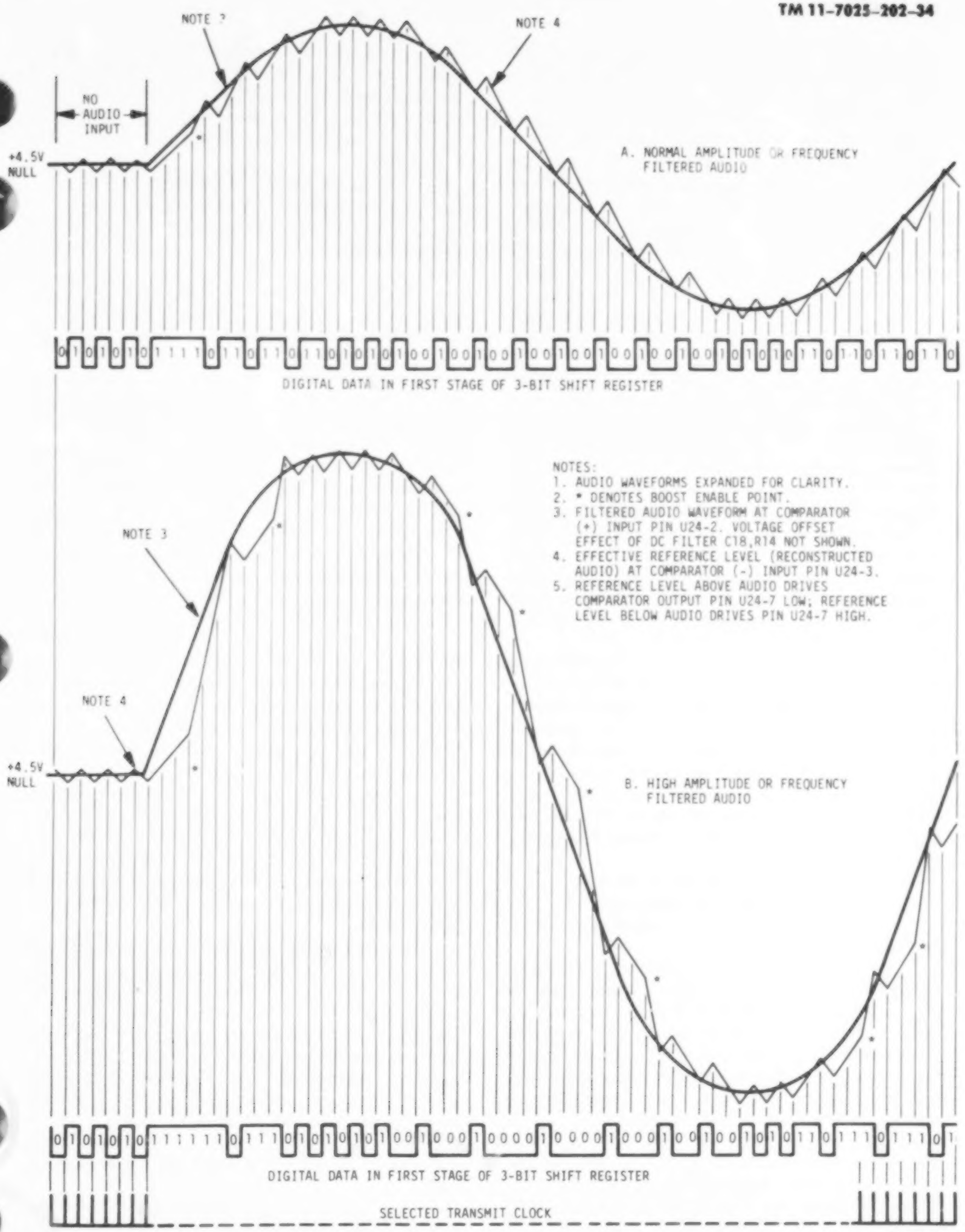
(3) Fixed resistor R4 couples a digital voice ring signal (DVRNGS) to filter input pin U22-7. DVRNGS is a 1600 Hz continuous tone that AVOW card 21A10 generates when either the VOICE O.W. TALK/LISTEN-OFF-RING switch on the front panel or the VO ORDW SYSTEM T/L-OFF-RING switch on the RAU is placed to RING. DVRNGS is multiplexed into the outgoing SG data to ring a far-end user.

(4) Two-stage filter/amplifier U22 passes desired audio frequency signals and attenuates high frequency out-of-band signals that could affect CVSD encoder circuit operation. Amplifier U22-9, capacitor C13, and resistor R10 make up a single-pole low-pass filter, while amplifier U22-1, capacitors C12 and C14, and resistors R7 and R9 make up a double-pole low-pass filter. Capacitor C15 couples the filtered audio signal to an audio/dc summing point, where it is superimposed on an offset dc level (*c*(7) below) for application to input comparator U24 of the CVSD encoder.

c. CVSD Encoder. The CVSD encoder converts the filtered audio analog signal to digital levels that are clocked into a 3-bit shift register for synchronous shiftout through an output data buffer to MO/C card 21A4. There, the encoded digital data are multiplexed into the SG data stream for transmission to a far-end TD-976/G. A CVSD decoder in the receiving TD-976/G translates the demultiplexed digital data into a reconstructed data analog (up/down integrating dc) signal, and then filters it into a close reproduction of the original audio signal. Delta modulating of the original audio signal with a switchable reference level (up/down integrating dc) controls the initial audio-to-digital conversion (encoding) process. The encoded digital levels, in turn, control the integrating direction of the reference level. These alternating up and down integrations effectively raise or lower (from +4.5 v null) an accumulative dc level upon which they are superimposed. Longer periods of up integration than down integration proportionally raise the dc level; shorter periods of up than down integration lower the dc level. This continuing activity is such that the sum signal (up/down integrations plus accumulative dc) coarsely tracks the filtered audio; that is, it reconstructs the encoded audio signal. Typical encoding activity waveforms for normal and high amplitude/frequency audio signals are shown in figure 2-15.

(1) Comparator U24-7 (sheet 2) monitors filtered audio signal and reference voltage levels at its two input pins. The audio signal is summed with an offsetting dc level ((7) below) at the R17, C15 junction input to comparator noninverting (+) pin U24-2. U24 continually compares this summed level with an inverting (−) pin U24-3 reference level (integrating dc) from reference filter C19,R15. Encoded logic levels being shifted through the 3-bit shift register's first stage control the reference level's integrating direction through switch U26 ((6) below). An encoded logic 1 switches +5 v (normal) or +9 v (boost) to filter C19, R15 for a slow or fast upward integration of the reference level. Conversely, a logic 0 switches +4 v or 0 v (ground) to the filter for a slow or fast downward integration of the reference level. These integrations alternately impart positive and negative errors with respect to the summed audio and offset dc level. The CVSD encoder repeatedly tries to correct the changing errors by reversing the reference level integration back toward the audio signal level. Since a corrective integration continues across the audio signal level to a next clock positive transition time, it creates an opposite polarity error before integration is again turned back toward the audio level. When normal integration continues for three clock periods without crossing the audio level, a boost enable signal ((5) below) steepens the integration slope (ramp) so that it will reach the audio level sooner. As the reference level crosses the audio level on an upward integration, it drives the comparator's output pin U24-7 low. The next clock positive transition clocks the low (logic 0) into the 3-bit shift register's first stage. Similarly, a reference level down integration across the audio level drives comparator pin U24-7 high, so that the next clock positive transition clocks a logic 1 into the register's first stage. The comparator's digital level output goes via DVOW card test loop (backplane jumper) (DVCT01) to the 3-bit shift register's first stage (U27-2 and U27-3, sheet 3). The typical effects of null (no audio), normal, and boost enable on the response of comparator U24 are shown in figure 2-15 and described in (*a*) through (*d*) below.

(*a*) With no audio input (A, fig. 2-15), the CVSD encoder nulls out at a +4.5 v dc level for subsequent receipt of an audio signal. Alternate logic 1's and 0's clocked into the 3-bit shift register operate switch U26 (sheet 2) to alternately reverse the dc filter C18, R14 input voltage between +4 v and +5 v at each clock positive transition. C18 charges to +4.5 v in response to the regular voltage reversals and steadily maintains that null voltage at the comparator's (+) pin U24-2. Out-of-phase reversal of the reference filter C19, R15 input integrates the comparator's (−) pin U24-3 reference level up and down across the +4.5 v null level at each clock positive transition. The comparator responds by switching its pin U24-7 output between high and low at each clock positive transition. This


NOTE 2
NOTE 4
NO AUDIO INPUT
+4.5V NULL
A. NORMAL AMPLITUDE OR FREQUENCY FILTERED AUDIO
0 1 0 1 0 1 0 1 1 1 1 0 1 1 0 1 1 0 1 1 0 1 0 1 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 1 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0
DIGITAL DATA IN FIRST STAGE OF 3-BIT SHIFT REGISTER
NOTE 3
NOTE 4
+4.5V NULL
B. HIGH AMPLITUDE OR FREQUENCY FILTERED AUDIO
0 1 0 1 0 1 0 1 1 1 1 1 1 0 1 1 1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0 1 0 0 1 0 1 0 1 1 0 1 1 1 0 1 1 1 0 1
DIGITAL DATA IN FIRST STAGE OF 3-BIT SHIFT REGISTER
SELECTED TRANSMIT CLOCK
EL5NG015

NOTES:

1. AUDIO WAVEFORMS EXPANDED FOR CLARITY.
2. * DENOTES BOOST ENABLE POINT.
3. FILTERED AUDIO WAVEFORM AT COMPARATOR (+) INPUT PIN U24-2. VOLTAGE OFFSET EFFECT OF DC FILTER C18,R14 NOT SHOWN.
4. EFFECTIVE REFERENCE LEVEL (RECONSTRUCTED AUDIO) AT COMPARATOR (-) INPUT PIN U24-3.
5. REFERENCE LEVEL ABOVE AUDIO DRIVES COMPARATOR OUTPUT PIN U24-7 LOW; REFERENCE LEVEL BELOW AUDIO DRIVES PIN U24-7 HIGH.

Figure 2-15. Typical DVOW card 21A11 CVSD encoder waveform.

activity produces a 010101--- data pattern flow through the 3-bit shift register and output data buffer U27-10 (sheet 3) to the MO/C card.

(*b*) Receipt of audio (initial positive cycle, A or B, fig. 2-15) raises comparator (+) pin U24-2 above the (−) pin U24-3 reference level and holds output pin U24-7 high. The next two clock positive transitions shift logic 1's into the 3-bit shift register's first stage. These successive 1's hold the output of switch U26 to the reference filter at +5 v ((6) below), and the filter's reference level to comparator (−) pin U24-3 integrating upward toward +5 v. When a third logic 1 is clocked into the 3-bit shift register's first stage, decoder U21 ((4) below) initiates a pin U21-12 (sheet 3) boost enable high. This high inverts and restores through U28-4 and U19-8, and forces the up integrator ((5) below) on a steep rise from +5 v toward +9 v. Applied through pins U26-8 to U26-10 (sheet 2) to reference filter C19, R15, the up integrator's voltage quickly raises the comparator (−) pin U24-3 voltage above the audio level at (+) pin U24-2 and drives output pin U24-7 low. The next clock positive transition shifts a logic 0 into the 3-bit shift register's first stage and reverses the reference level's integrating direction downward ((6) below). Since the 3-bit shift register no longer contains three 1's, decoder U21 puts boost enable low and restores the up and down integrators to their normal +5 v and +4 v inputs ((5) below).

(*c*) With a normal amplitude or frequency audio input (A, fig. 2-15), the up and down integrators provide normal integration ramps. Applied through switch U26, after the initial boost enable ((*b*) above), these normal up and down ramps are steep enough to crisscross the audio signal level within three clock period intervals. Typically, normal integration ramps produce the following encoded digital data out patterns for a normal amplitude or frequency audio signal.

1. 110110----for the rising segment.

2. 001001----for the falling segment.

3. 101010----for the positive or negative near-peak segment.

(*d*) A high amplitude or frequency audio signal (B, fig. 2-15) has rising and falling segments that are too steep for normal reference level up/down integrations. The initial boost enable ((*b*) above) steepens the reference level up integration ramp so that it crosses the audio signal's rising level. This crossing and a clock positive transition turn the reference level below the audio level, and the next clock transition turns it upward again at a normal integration rate. Now, since the reference level cannot cross the audio again within three clock periods, decoder U21 sees three 0's in the 3-bit shift register and initiates a boost enable high ((4) below). This high steepens the up integration ramp toward the audio level. The boost enable is repeated each time a reference level normal up/down integration does not cross the audio level within three clock periods. Typically, a mixture of normal and boost integration ramps produces the following encoded digital data output patterns for a high amplitude or frequency audio signal.

1. 11101110----for the rising segment.

2. 00010001----for the falling segment.

3. 10101010----for the positive or negative near-peak segment.

NOTE

> The number of consecutive logic 1's or 0's encoded from a rising or falling audio signal increases as the audio signal amplitude or frequency increases.

(2) Three-bit shift register U27-6, U20-10, and U20-6 (sheet 3) receives the encoded digital output from comparator U24. A selected clock signal from the input timing selection circuits (*d*(1) below) clocks the encoded digital data into and through the register. The 3-bit shift register performs three functions. Its first stage provides a Q pin U27-6 digital output to output data buffer U27-10 and complementary (Q and $\overline{Q}$) outputs to switch U26 ((6) below). All stages provide Q and $\overline{Q}$ outputs to decoder U21, which activates an integration rate boost each time three consecutive 1's or 0's are contained within the register.

(3) Output data buffer U27-10 (sheet 3) provides for synchronous transfer of the encoded digital data to a combiner on MO/C card 21A4 for insertion into the outgoing SG data. A gated transmit clock from gate U35-9 (*d*(1) below) clocks digital data through flip-flop U27-10 onto the digital voice orderwire input (DVOWI) line to the MO/C card.

(4) Decoder U21 (sheet 3) monitors the contents of the 3-bit shift register for three consecutive 0's or 1's. Gate U21-8 looks for three highs (000 contents) at the register's $\overline{Q}$ pins, while gate U21-6 looks for three highs (111 contents) at the register's Q pins. Either trio of highs causes U21-12 to go high, creating the boost enable.

(5) Up and down integrators provide differential error voltages to switch U26 in response to control inputs from inverters U19-8 and U19-6. Under normal conditions, U21-12 is low and holds inverter U19-8 low and inverter U19-6 high. These control inputs stabilize up and down integrator outputs at about +5 v and +4 v, respectively. Under a boost enable condition (111 ot 000 in 3-bit shift register), U19-8 goes high and initiates up integration from +4 v to 0 v. Zener diode VR1 regulates the integrator's operating supply voltage at +9.1 +0.9 v. Resistor R21 limits VR1 current.

(*a*) The up integrator consists of voltage divider R22, R24, R26, and capacitor C20 at the divider's R24, R26 junction. Inverter U19-8 switches the divider's

R22, R24 junction low and high for normal and boost operations, respectively. A low at the R22, R24 junction applies about +5 v to C20 at the R24, R26 junction. C20 stabilizes at +5 v and maintains that level to switch U26 input pins 1 and 8. A boost enable input (U19-8 high) effectively places both ends and both junctions of divider R22, R24, R26 at about +9 v. C20 immediately starts integrating toward +9 v at a fast rate, providing a steep positive-going ramp at switch U26 input pins 1 and 8. Subsequent removal of boost enable (mixed logic levels in 3-bit shift register) restores the R24, R26 junction voltage to +5 v, and C20 integrates downward from the positive level it charged to during the boost.

(*b*) Down integrator R23, R25, R27, and C21 similarly provides a normal +4 v level or a boost +4 v to 0 v integrating level to switch U26 input pins 4 and 11. The voltage divider across +9.1 v and ground responds to an R23, R25 junction high from U19-6 with +4 v to capacitor C21. A boost enable input (U19-6 low) grounds the divider's R25, R27 junction, and C21 integrates downward from +4 v to 0 v. This boost condition provides a steep negative-going ramp at switch U26 input pins 4 and 11. Subsequent removal of boost enable restores the R25, R27 junction to +4 v, and C21 integrates upward from the low level it discharged to during the boost.

(6) Switch U26 (sheet 2) has two dual switch sections for selectively applying up and down integrator outputs to the dc and reference filters. The 3-bit shift register's first stage Q and $\overline{Q}$ outputs control the dual switch sections through inverters U19-11 and U19-3, respectively. A logic 1 in the first stage puts U19-11 low and U19-3 high. The latter high simultaneously completes a down integrator voltage path through pins U26-4 and U26-3 to dc filter C18, R14 and an up integrator voltage path through pins U26-8 and U26-9 to reference filter C19, R15. Conversely, a logic 0 in the first stage reverses integrator voltages to the two filters. A U19-11 high now simultaneously completes an up integrator voltage path through pins U26-1 and U26-2 to the dc filter and a down integrator voltage path through pins U26-11 and U26-10 to the reference filter.

(7) DC filter C18, R14 (sheet 2) maintains a nominal dc level that slightly offsets the filtered audio signal superimposed on it. The dc level effectively attenuates the audio signal about 10 percent. A positive-going audio transition (encoded into longer strings of 1's than 0's) slowly discharges C18 by applying the down integrator voltage for longer periods. This action slightly slows the rise of the audio signal at comparator noninverting pin U24-2. Conversely, a negative-going audio transition (encoded into longer strings of 0's than 1's) slowly charges C18 by applying the up integrator voltage for longer periods. This action slightly slows the drop of the audio signal at comparator pin U24-2.

(8) References filter C19, R15 provides a reconstructed audio signal to comparator inverting pin U24-3. The filter passes either an up integrating voltage through pins U26-8 and U26-9 or a down integrating voltage through pins U26-11 and U26-10 to the comparator. These integrating voltage reversals are attempts to correct a continuing error voltage difference between the reference voltage and the filtered audio level. Absolute correction cannot be achieved, since the clock switched reference voltage invariably crosses the audio level and is then turned back for another attempt at correction. These attempts at error correction (up and down crossings of the audio signal level) produce the logic patterns that can be decoded and filtered to duplicate the original audio at a far-end demultiplexer. Capacitor C19 shunts to ground any high frequency components that may appear on the integrating reference level being passed to comparator U24. The varying reference level consists of encoded logic level controlled up/down integration ramps superimposed on an undulating dc level. The level's undulation amplitude and rate approximate the amplitude and rate of the filtered audio signal.

d. Timing Selection Circuits (sheet 3). The timing selection circuits consist of input gating (U28-8, U35-9, U35-7) and a clock selector (U33-8).

(1) The transmit digital voice orderwire clock (TDVOW) occurs during those bit times when DVOW data are to be inserted into the outgoing SG (at bit 17 times of minor frames 0, 5, 10, and 15 for 96-channel operation, and at bit 17 times of minor frames 0, 1, 5,6, 10, 11, 15, and 16 for 48-channel operation). The transmit clock (TCLK) controls the data rate of the outgoing SG (either 4915.2 kHz for 96-channel operation or 2457.6 kHz for 48-channel operation). The transmit digital voice orderwire smooth clock (TDVOWC—) is homogenous (occurring at bit 17 times of minor frames 0, 5, 10, and 15 and at bit 9 times of minor frames 3, 8, 13, and 18). Each coincidence of TDVOW and TCLK gates a clock to pin U33-9 and to pin U27-12 to clock the encoded digital data through U27-10. Each coincidence of TDVOWC— and TCLK gates a clock to pin U33-13.

(2) Clock selector U33-8 selects one of its gated clock inputs to clock the 3-bit shift register. In 96-channel operation, 96 CHE is high at pin U33-10 and the pin 9 input is selected. In 48-channel operation, 48 CHE is high at pin U33-1 and the pin 13 input is selected. In either case, the register is clocked at the 57.656 kbps DVOW sampling rate.

2-33. Decoder Section Theory of Operation

(fig. FO-7)

a. General. This paragraph describes the detailed operation of the circuits in the decoder section on DVOW card 21A11. The theory of operation is divided into the five functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Timing selection circuits (*b* below).
(2) Input data buffer (*c* below).
(3) CVSD decoder (*d* below).
(4) Output circuits (*e* below).
(5) Ring detector circuits (*f* below).

NOTE

The sheet number references in *b* through *f* below refer to figure FO-7.

b. Timing Selection Circuits (sheet 5). The timing selection circuits consist of input gating (U34-8, U28-6, U35-4) and a clock selector (U33-6).

(1) The receive digital voice orderwire clock (RDVOW) occurs during those bit times when DVOW data are to be extracted from the incoming SG (at bit 17 times of minor frames 0, 5, 10, and 15 for 96-channel operation, and at bit 17 times of minor frames 0, 1, 5, 6, 10, 11, 15, and 16 for 48-channel operation). The receive clock (RCLK and RCLK—) is at the data rate of the incoming SG (either 4915.2 kHz for 96-channel operation or 2457.6 kHz for 48-channel operation). The receive digital voice orderwire smooth clock (RDVOWC—) is homogenous (occurring at bit 17 times of minor frames 0, 5, 10, and 15 and at bit 9 times of minor frames 3, 8, 13, and 18). Each coincidence of RDVOW and RCLK— gates a clock to pin U33-4 and to pin U7-12 of the input data buffer, enabling a bit of DVOW data to be extracted from the incoming SG. Each coincidence of RDVOWC— and RCLK gates a clock to pin U33-3.

(2) Clock selector U33-6 selects one of its gated clock inputs to clock 3-bit shift register U7-6, U14-6, and U14-10. In 96-channel operation, 96 CHE is high at pin U33-5 and the pin 4 input is selected. In 48-channel operation, 48 CHE is high at pin U33-2 and the pin 3 input is selected. In either case, the register is clocked at the 57.656 kbps DVOW sampling rate.

c. Input Data Buffer (sheet 5). Input data buffer U7-10 extracts the DVOW data bits from the incoming SG data (SDATA). The gated clocks from U28-6 occur during those bit times when DVOW data are present in the SDATA. The input data buffer's output is routed to the first stage of the 3-bit shift register (*d*(1) below).

d. CVSD Decoder. The CVSD decoder reconstructs extracted serial DVOW data bit patterns into a coarse audio analog signal, and then filters it to provide a clean audio signal to the output amplifiers. Most of the decoding process is similar to the encoding process (para 2-32*c*), in that DVOW data bit levels in a 3-bit shift register control the switches and up/down integrator circuits. Normal and boost integrations activated by differing and alike 3-bit combinations in the shift register's flowing DVOW pattern develop the coarse audio analog signal at an audio reconstructor RC circuit. This reconstructed audio signal looks like the jagged reference level waveform (fig. 2-15) that produced the DVOW data output patterns at the sending TD-976/G. Subsequent filtering smooths the reconstructed audio analog signal to a close reproduction of the original filtered audio signal.

(1) Three-bit shift register U7-6, U14-6, and U14-10 (sheet 5) receives extracted DVOW digital data from input data buffer U7-10. A selected clock signal from the timing selection circuits (*b*(2) above) clocks the digital levels into and through the register. The 3-bit shift register's first stage provides complementary (Q and $\overline{Q}$) outputs through inverters to switch U12 ((4) below). All stages provide Q and $\overline{Q}$ outputs to decoder U6, U34, which activates an integration rate boost each time three consecutive 1's or 0's are contained within the register.

(2) Decoder U6-6, U6-12, and U34-3 (sheet 5) monitors the 3-bit shift register's contents for three consecutive 0's or 1's. Gate U6-6 looks for three highs (000 contents) at the register's $\overline{Q}$ pins, while gate U6-12 looks for three highs (111 contents) at the register's Q pins. Either trio of highs causes U34-3 to go high, creating the boost enable.

(3) The up and down integrators provide positive- and negative-going integration voltage levels to switch U12 in response to control inputs from inverters U5-8 and U5-11 (sheet 5). The 3-bit shift register is held in a preset condition of 100 by the major frame sync level 8 (SYNC8—) signal when the TD-976/G has not acquired major frame sync. This action inhibits creation of a boost enable and stabilizes the up and down integrator outputs at about +5 v and +4 v, respectively. In turn, the low from U7-7 is inverted by U5-6 and closes up an integrator dc voltage path through switch pins U12-8 and U12-9 to audio reconstructor R37, C23, and C30, causing C30 (sheet 4) to charge to a stabilized +5 v level. This precharge action prepares the audio reconstructor for receipt and processing of data after major frame sync is acquired. When the TD-976/G has detected and counted eight major frame syncs, the SYNC8— signal goes high, releasing the 3-bit shift register to shift in data. The up and down integrators remain stabilized at +5 v and +4 v, respectively, until three consecutive 0's or 1's are shifted into the register. At this time, a boost enable is created and U5-8 (sheet 5) goes high and initiates up integration from +5 v to +9 v, while U5-11 goes low and initiates down integration from +4 v to 0 v. Zener

diode VR2 regulates the integrator's operating supply voltage at +9.1 ±0.1 v. Resistor R31 limits VR2 current.

(a) The decoder's up integrator consists of voltage divider R30, R33, R35, and capacitor C24 at the divider's R33, R35 junction. Inverter U5-8 switches the divider's R30, R33 junction low and high for normal and boost operations, respectively. A low at the R30, R33 junction applies about +5 v to C24 at the R33, R35 junction. C24 integrates to and stabilizes at +5 v and maintains that level to switch input pin U12-8. A boost enable input (U5-8 high) effectively places both ends and both junctions of divider R30, R33, R35 at +9 v. C24 immediately starts integrating toward +9 v at a fast rate, providing a steep positive-going ramp at switch input pin U12-8. Subsequent removal of boost enable (mixed logic levels in 3-bit shift register) restores the R33, R35 junction voltage to +5 v, and C24 integrates downward from the positive level it charged to during the boost.

(b) Down integrator R32, R34, R36 and C25 similarly provides a normal +4 v level or a boost +4 v to 0 v integrating level to switch pin U12-11. The voltage divider across +9.1 v and ground responds to an R32, R34 junction high from U5-11 with +4 v to capacitor C25. A boost enable input (U5-11 low) grounds the divider's R32, R34 junction, and C25 integrates downward from +4 v to 0 v. This boost condition provides a steep negative-going ramp at switch pin U12-11. Subsequent removal of boost enable restores the R34, R36 junction voltage to +4 v, and C25 integrates upward from the low level it discharged to during the boost.

(4) Two of the four switch sections of switch U12 (sheet 5) selectively apply either the up or the down integrator's voltage level through R37 to audio reconstruct capacitor C23. The 3-bit shift register's first stage Q and $\bar{Q}$ outputs control the two switch sections through inverters UR-3 and UR-6, respectively. A logic 1 in the first state (U7-7 low) puts UR-3 low and UR-6 high. The latter high completes an up integrator voltage path through pins U12-8 and U12-8 and U12-9 and through R37 to C23. A logic 0 in the first stage (U7-6 low) puts U5-3 high, which completes a down integrator voltage path through pins U12-11 and U12-10 and through R37 to C23.

(5) Audio reconstructor R37, C23 (a switching transients filter) assembles applied up and down integration voltage segments end to end to reconstruct a coarse audio analog waveform. Starting from a no-audio alternating +4 v and +5 v level, C23 alternately charges and discharges as the up and down integration voltages are switched to it by switch U12 ((4) above). A positive-going integration voltage segment (decoded from longer strings of 1's than 0's, as shown in figure 2-15) progressively charges C23 by applying the up integrator level for longer periods. Conversely, a negative-going integration voltage segment (decoded from longer strings of 0's than 1's) gradually discharges C23 by applying the down integrator level for longer periods. As switch U12 alternates the integrator levels to the audio reconstructor, C23 literally tags the lead end of each new integration voltage segment onto the tail end of the preceding opposite-direction segment. This is, an up integration voltage charges C23 from the voltage level to which it was discharged by the preceding down integration voltage; similarly, the next down integration voltage discharges C23 from the voltage level to which it was charged by the preceding up integration voltage. C23's alternating charge and discharge transitions, caused by the series of up and down integration voltages, trace or reconstruct an audio analog waveform. This reconstructed audio analog signal goes to filter amplifier (+) input pin U8-4 (sheet 4).

(6) The filter amplifier circuit (sheet 4) consists of operational amplifier U8-1 and its negative feedback high-pass filter network R51, R54, R53, C31. The amplifier provides a dc gain of 2 and a high frequency gain of 1.75 for the reconstructed audio analog signal applied at (+) input pin U8-4. Network R51, R54, R53, C31 filters out the amplified signal's high frequency components (positive and negative integration voltage segments) by feeding them back out of phase from output pin U8-1 to (−) input pin U8-3. Resistor R55 couples the amplifier's output to three-pole eliptical filter C32-C34,L1 for additional filtering and distribution to the ring detector and two voice audio gain amplifiers.

e. *Output Circuits* (sheet 4). The output circuits provide signal gain, level setting, and impedance matching for voice audio signals to remote, extension, and local handsets.

(1) Digital voice extension output gain amplifier U17-8 receives filtered audio at its (+) input pin U17-4 directly from the eliptical filter. Variable resistor R57 (−) input pin U17-3 sets the amplifier's driving gain for about 1.6 v peak to peak (−4 ± 1 dBm at 1 kHz) measured at TP7. Resistor R62 matches output transformer T2's impedance to digital voice extension output (DVEXO and DVEXO—) signal lines. T2 provides 1:1 transformer coupling at 600 ohms impedance. The DVEXO output goes to the DGTL VO RCV jack on the RAU.

(2) Digital voice earphone gain amplifier U17-9 receives the eliptical filter's audio signal at (+) input pin U17-6 through voltage divider R56, R58. The divider attenuates the filtered audio about 60 percent at its R56, R58 junction. Variable resistor R59 at (−) input pin U17-7 sets the amplifier's driving gain for about 68 millivolts peak to peak (−5 ±3 dBm at 1 kHz) measured at TP3. The digital voice earphone

(DVEAR) output goets through AVOW card 21A10 to the earphone of a handset plugged into the VOICE O.W. HANDSET jack on the front panel jack on the RAU.

f. Ring Director Circuits (sheet 4). The ring detector circuits detect and respond to received ring tones with a digital voice call signal that lights the SYSTEM CALL indicators on the front panel and the RAU.

(1) Ring detector U15, R40, Q1 monitors the eliptical filter's audio output for the presence of a 1600 Hz ring tone. Capacitor C28 couples the R41 attenuated audio signal to the detector's first stage operational amplifier (−) input pin U15-3. Variable resistor R40 of input voltage divider R40,R38,R41 centers the first stage amplifier's bandpass response at 1600 Hz for activation of the ring detector latch (U34-6, U6-8) through amplifier U15-9, diode CR1, and transistor Q1. Resistor R44 couples the first stage amplifier output to amplifier U15-9. The two-stage filtering accentuates the 1600 Hz frequency and attenuates frequencies at either side of 1600 Hz. Diode CR1 passes only the positive half-cycles of the 1600 Hz (ring tone) signal to charge delay RC circuit C29, R49. This circuit's time constant keeps the ring detector latch from being inadvertenly activated by frequencies near 1600 Hz that may appear in the filtered audio. Only a valid 1600 Hz ring tone persists long enough to charge C29 upward and ultimately activate the ring latch. Upon receipt of a ring tone, C29 charges in a positive direction and biases Q1 fully on. The Q1 switch-on puts its collector near ground (logic 0 out), signifying that a valid ring tone has been detected.

(2) The ring detector latch (U34-6, U6-8) is set by the Q1 logic 0 output and produces the digital voice call (DVCAL—) signal. DVCAL— is routed to AD card 21A1, where it causes the SYSTEM CALL indicators on the front panel an the RAU to light and the audible ALARM horn on the front panel to sound. The latch remains set until either of two reset signals is applied. A local digital talk/listen (LDTL—) low from the VOICE O.W. TALK/LISTEN-OFF-RING switch on the front panel resets the latch through input pin U6-10. A remote digital talk/listen (RDTL—) low from the VO ORDW SYSTEM T/L-OFF-RING switch on the RAU similarly resets the latch through input pin U6-9.

Section IX. DIGITAL DATA ORDERWIRE (DDOW) ENCODER CARD 21A3

2-34. General

This section contains separate block diagram and detailed theory of operations discussions of the functional circuits on the DDOW encoder card. There is one DDOW encoder card (21A3) in the TD-976/G. The card receives asynchronous 75-baud or 1200-baud teletype (TTY) digital data through its input circuits, derives on-card timing from the data, and then processes the data out as synchronous digital data. An on-card code generator generates a 7-bit repetitive ring/ready code pattern for ringing a far-end teletype unit or signaling a ready condition to it. An input rate buffer provides the means for synchronously outputting TTY digital data or the ring/ready code pattern to a combiner circuit on MO/C 21A4 for insertion into the outgoing SG data stream. Paragraph 2-35 provides a general discussion of the Baudot and American Standard Code for Information Interchange (ASCII) code formats used by the teletype units. A general comprehension of these formats is required in order to understand operational concepts of the DDOW encoder card. Paragraph 2-36 provides a block diagram discussion of the DDOW encoder card based on the block diagram in figure 2-17. The detailed theory of operation discussed in paragraph 2-37 is based on the DDOW encoder card schematic diagram in figure FO-8.

2-35. Baudot and ASCII Code Formats
(fig. 2-16)

a. General. Both the Baudot code format (75-baud digital data) (*b* below) and the ASCII code format (1200-baud digital data) (c below) are based on a start-stop signaling code. The intelligence elements are applied sequentially to a signal line in time intervals termed marks and spaces. To ensure synchronization between the transmitting and receiving equipment, a start element, which is always a space, is added at the beginning of each combination of intelligence elements. A stop element, which is always a mark, is added at the end of each combination of intelligence elements. The length of the stop element varies between the two code formats.

b. Baudot Code Format. The Baudot code format, which is a 5-level code, is shown in A of figure 2-16. A mark is defined as the time interval during which there is current flow in the signal line. Conversely, a space is defined as the time interval during which there is no current flow in the signal line. The black circles in the character arrangement chart represent marks, while the blank squares represent spaces. This format has a 7.5-unit transmision pattern.

c. ASCII Code Format. The ASCIII code format, which is an 8-level code, is shown in B of figure 2-16. A mark is defined as the time interval during which there is forward current flow in the signal line. Conversely, a space is defined as the time interval during which there is a reverse current flow in the signal line. The black circles in the character arrangement chart represent marks, while the blank squares represent spaces. The main block shows the arrangements of levels 1 through 5. The four smaller blocks at the right show the arrangements of levels 6 and 7, which select the row of characters that will be used as indicated by the arrows. Level 8 provides an even-parity feature (if even parity is not used, level 8 is always a mark). If even parity is used, level 8 will be a mark whenever the number of marks in levels 1 through 7 is an odd number; otherise, it will be a space. When even parity is used, characters and functions that have white backgrounds have level 8 as a space, and those with dark backgrounds have level 8 as a mark. This format has a 11-unit transmission pattern.

2-36. Block Diagram Discussion

(fig. 2-17)

a. General. The block diagram discussion is divided into five functional circuit descriptions as follows:

(1) The input circuits (*b* below) provide for jumper plug selection of either 75-baud or 1200-baud TTY digital data and 75 Hz or 1200 Hz clock signals for data processing operations. A level shifter converts received 1200-baud data signals to TTL compatible levels for on-card use.

(2) The timing extractor (*c* below) aligns on-card timing with received TTY digital data. It monitors the input TTY for individual coded character start and stop bits. Detection of a start bit triggers a brief reset signal that initializes timing extractor functional circuits and related counter circuits. Detection of stop bits conditions the timing extractor functional circuits for receipt and detection of a subsequent coded character.

(3) The clock generator (*d* below) generates a 75 Hz and two separate 1200 Hz clock signals for timing on-card funtional circuits.

(4) The ring/ready code generator (*e* below) generates a 7-bit repetitive ring/ready code pattern. The patterns are outputted through the input rate buffer for multiplexing into the SG data stream.

(5) The input rate buffer (*f* below) temporarily stores received asynchronous data for synchronous output to the MO/C card. A write address counter enters serial data bits into an elastic storage register for synchronous accessing by a read address counter.

b. Input Circuits. A digital data sent (DDSD—) signal from the RAU enables the input circuits to process either digital data 75-baud input (D75I) or digital data 1200-baud input (D12I) signals from a teletype unit. High-level (+130 v) D75I signals come in through an optical coupler on the RAU and are TTL compatible when applied to the input circuits. Low-level (±6 v) D12I signals come in through the RAU unchanged and therefore require conversion to TTL levels by the level shifter. The plug-in position of a rate switch (jumper plug) determines whether D75I data and related 75 Hz clock signals or D12I and related 1200 Hz clock signals are passed through the data and timing selector to the timing extractor (*c* below).

(1) Level shifter U22 responds to D12I data forward current mark and reverse current space inputs with TTL data logic 1 and logic 0 outputs, respectively. Two zener diodes (VR2,VR3) between the D12I input and ground protect the level shifter from excessive voltages that may appear on the D12I line.

(2) A two-position rate switch (jumper plug) provides the means for selection of the data input rate. In one plug-in position, the switch puts digital data 75-baud enable (D75EN) high and digital data 1200-baud enable (D12EN) low for processing of 75-baud data. In the other position, the switch grounds D75EN and puts D12EN high for processing of 1200-baud data. The D75EN and D12EN signals also establish the data processing rate for the DDOW decoder card (section X).

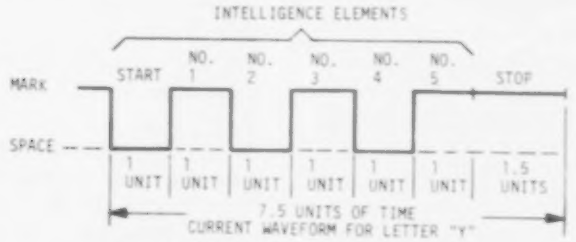
(3) The data and timing selector selects the data and related timing input that will be routed to the timing extractor. D75EN and digital data send (DDSD—) enable passage of D75I data and 75 Hz clock signals to the timing extractor. D12EN and DDSD— similarly enable passage of D12I and 1200 Hz signals to the timing extractor.

c. Timing Extractor. The timing extractor monitors received data with an edge detector and passes the data by its character storage shift register to the input rate buffer (*f* below). The data consist of coded characters with start and stop bits. Upon detecting a coded character's start bit, the edge detector initiates a short reset/clear pulse sequence through a storage flip-flop and a reset one-shot. This pulse briefly clears the character storage shift register, resets the end-of-character latch, and restarts the clock generator counters that supply timing through the data and timing selector. These simultaneous actions align the selected timing positive clock transitions with the incoming data bits. Shift-in of a complete coded character (with preceding start and following stop bits) into the register enables an end-of-character gate, which sets the end-of-character latch. This action readies the edge detector to detect the start bit of the next incoming character on the data line.

(1) The edge detector one-shot is normally held in a clear state by the reset action of the end-of-character latch. When a complete character has been shifted into the character storage shift register, the end-of-character gates decode this fact and set the end-of-character latch, which releases the edge detector one-shot. The next positive transition on the data line triggers the edge detector, which produces a 5-microsecond negative pulse output whose trailing edge (positive transition) clocks the storage flip-flop. If the data line is still high (a start bit (space) is present), the storage flip-flop will be set. If the data line is not high when the flip-flop is clocked (the high that triggered the edge detec-

FIGURES	—	5/8	WRU	5	3	1/4	&		8	'	1/2	3/4	.	7/8	9	0	1	4	BELL	5	7	3/8	2	/	6	"						
LETTERS	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	BLANK	LETTERS	FIGURES	SPACE	CARRIAGE RETURN	LINE FEED
1	●	●		●	●	●				●	●						●		●		●		●	●	●	●		●	●			
2	●		●				●		●	●	●	●				●	●	●			●	●	●					●	●			●
3			●			●		●	●		●		●	●		●	●		●		●	●		●	●			●		●		
4		●	●	●		●	●			●	●		●	●	●			●				●		●				●	●		●	
5		●					●	●				●	●		●	●	●			●		●	●	●	●	●		●	●			

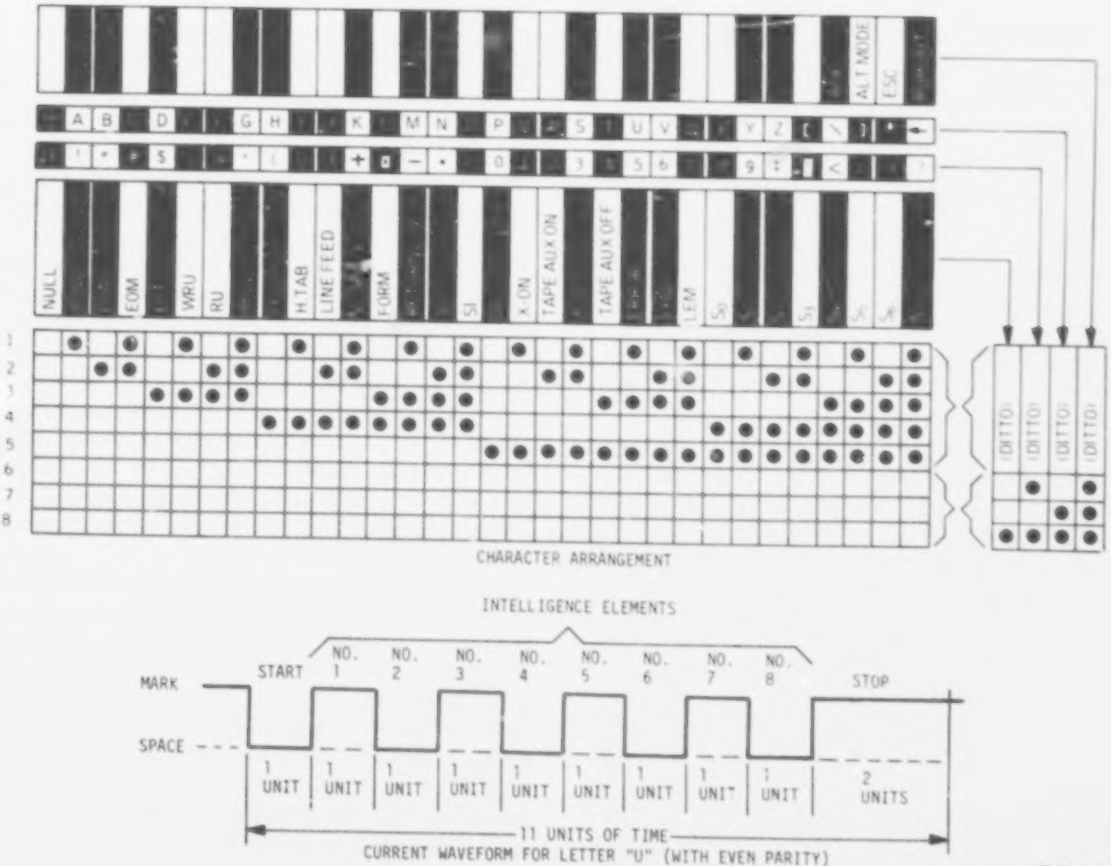
CHARACTER ARRANGEMENT



INTELLIGENCE ELEMENTS
MARK
SPACE
START
NO. 1
NO. 2
NO. 3
NO. 4
NO. 5
STOP
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1.5 UNITS
7.5 UNITS OF TIME

CURRENT WAVEFORM FOR LETTER "Y"

A. BAUDOT CODE FORMAT (5-LEVEL)



ALT MODE
ESC
A
B
D
G
H
K
M
N
P
S
U
V
Y
Z
[
\
]
!
"
#
$
+
0
3
5
6
9
:
<
?
NULL
EOM
WRU
RU
H.TAB
LINE FEED
FORM
SI
X-ON
TAPE AUX ON
TAPE AUX OFF
LEM
1
2
3
4
5
6
7
8
(DITTO)
(DITTO)
(DITTO)
(DITTO)
CHARACTER ARRANGEMENT
INTELLIGENCE ELEMENTS
MARK
SPACE
START
NO. 1
NO. 2
NO. 3
NO. 4
NO. 5
NO. 6
NO. 7
NO. 8
STOP
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
1 UNIT
2 UNITS
11 UNITS OF TIME

CURRENT WAVEFORM FOR LETTER "U" (WITH EVEN PARITY)

B. ASCII CODE FORMAT (8-LEVEL)

EL5NG016

Figure 2-16. Baudot and ASCII code formats.

tor was a noise pulse), the flip-flop will remain in a reset state. Setting of the storage flip-flop triggers the reset one-shot, which produces a 1-microsecond negative pulse output. This output resets the end-of-character latch, causing the edge detector to be held in a clear state. Also, the storage flip-flop is reset, the character storage shift register is cleared, and certain counters in the clock generator are restarted.

(2) The coded character serial data bits are clocked into the shift register by the selected timing signal from the clock generator. Each bit shifted into the register is routed out through its bit 1 output and is applied through U25-8 to the input rate buffer (*f* below).

(3) Seperate end-of-character gates are enabled by D75EN or D12EN and monitor the character storage shift register for the presence of a complete coded character within the shift register. The end-of-character gate enabled by D75EN monitors the shift register bit 7 and inverted bit 1 outputs. When a Baudot coded character's start bit (space, a logic 1) reaches the 7th stage of the shift register and the stop bit (mark, a logic 0) enters the 1st stage, the end-of-character gate is enabled and sets the end-of-character latch. Similarly the end-of-character gate enabled by D12EN monitors the shift register bit 11 and inverted bit 1 and bit 2 outputs. When an ASCII coded character's start bit reaches the 11th stage and the stop bits enter the 1st and 2nd stages, the end-of-character gate sets the end-of-character latch.

(4) The end-of-character latch alternately enables and inhibits operation of the edge detector one-shot. Initially, a power on reset (PRS—) sets the latch and puts its clear output high. This high lets the edge detector one-shot respond to a positive voltage transition on the data line ((1) above). Upon subsequent detection of a coded character's start bit, a 1-microsecond pulse resets the latch, putting its clear output low. This low inhibits the edge detector one-shot so that it will not respond to logic 1 bits (highs) of the coded character being processed. Detection of the coded character's start and stop bits ((3) above) sets the latch and puts its clear output high again. The high lets the edge detector one-shot respond to the next character's start bit when it arrives on the data line.

d. Clock Generator. The clock generator has an input divide-by-16 counter (U2) that converts the 4915.2 kHz digital data clock (DDCLK) input to a 307.2 kHz square wave output. This output drives controlled and free-running divide-by-256 counters. It also increments divide-by-16 counter U9 under control of an enable signal.

(1) Free-running counter U3, U4 generates a 1200 Hz square wave that clocks the input rate buffer's elastic storage register and increments its write address counter. U3, U4 divides its 307.2 kHz input by 256.

(2) Controlled counter U1,U8 also divides its 307.2 kHz input by 256 to produce a 1200 Hz square wave and an enable output. This counter is briefly reset to start in it sychronization with each received coded character's data bits. The 1200 Hz square wave directly clocks a code generator (*e*(2) above). The enable output controls the clocking of divide-by-16 counter U9 by a 307.2 kHz square wave.

(3) Divide-by-16 counter U9 generates a 75 Hz square wave that clocks the character storage shift register in 75-baud data processing operations. The 75 Hz square wave also drives the SG interrupter on the SG D/R card (para 2-42*c*). Each enable pulse (1200 Hz rate) from controlled divide-by-256 counter U1,U8 lets a 307.2 kHz square wave positive transition increment U9 once. This intermittent clocking activity divides the 307.2 kHz clock b 4096 to produce a 75 Hz square wave.

e. Ring/Ready Code Generator. When activated, this circuit generates about 35 identical 7-bit ring/ready code patterns in succession. A resettable code generator provies serial code bits for gating out under control of a one-shot. The gate's code patterns go to the input rate buffer's elastic storage register for output and insertion in the SG data stream. Extracted by a far-end demultiplexer, the code patterns ring a TTY or signal a ready condition to it.

(1) Either a digital data ring (DDRG—) or a digital data ready (DDRY—) low from the TTY switches on the RAU trigger a ring/ready time one-shot. The one shot's 206-millisecond positive pulse output enables U12-11 to pass and invert the serial code bits generated by the code generator. The inverted code pattern bits (1011000) are restored by U12-8 for entry into the elastic storage register. The inverted code pattern bits are also fed back to the code generator.

(2) Between ring/ready signaling requirements, logic 1's (continuous high from U12-11) are repeatedly clocked into the code generator. Whenever a ring/ready sequence is initiated, the inverted code bits are fed to the code generator. These bits are shifted into and through the generator's three stages to create the 7-bit repetitive ring/ready code.

f. Input Rate Buffer. The input rate buffer has a write address counter for entering asynchronous data or repetitive ring/ready code pattern bits into an elastic storage register for synchronous accessing by a read address counter. The accessed data go to the combiner on the MO/C card for insertion into the outgoing SG data stream. The two counters are initially preset to establish a four-count offset so that each data bit entered into the elastic storage register is accessed for output four counts later. Since the read address counter is being clocked at a slightly faster instantaneous rate than the write address counter, the read address counter, gradually advances on the write address counter. A rate comparator monitors both counters' address outputs and causes the desired four-count offset to be reestablished when write and read address counts come within three counts of each other.

(1) A 1200 Hz square wave from the clock generator increments the write address counter and advances its 3-bit write address binary outputs. A PRS— low presets this counter to a count of 4 at equipment power turn-on. The incrementing write address outputs sequentially select the elastic storage register's eight cells for clock-in (entry) of data.

(2) At initial power turn-on, PRS— presets the read address counter to a count of 0 (four counts behind the write address counter). Each coincidence of a transmit clock (TCLK—) and a transmit digital data orderwire (TDTAOW) signal (coincidences occur at the digital data sampling rate of 1201 Hz), unless inhibited by a transmit delete (TDLTTY), increments read address counter U14. In turn, the read address outputs sequentially select bit storage cells of the elastic storage register for output of the teletype orderwire input (TTYOWI) to the MO/C card. Because coincidences of TCLK—'s and TDTAOW's occur at a slightly higher rate (nominal 1201 Hz) than the write clocks (nominal 1200 Hz rate), the address counter advances on the write address counter. When the read address counter advances to within three counts of the write address counter. The rate comparator generates a receive teletype orderwire (RTTYOW) signal requesting that a stuff action be performed. The stuff request circuits on MO/C card 21A4 recognize this condition and cause TC (M) 21A5, at the proper time, to put TDLTTY low for one coincidence of a TCLK— and TDTAOW, inhibiting the read counter from incrementing. This action (stuffing) reestablishes the desired offset of four counts between the two counters.

(3) The 8-bit elastic storage register receives data or ring/ready code bits through U12-8. The 3-bit write address sequentially selects the eight cells of the register for entry of input data by the 1200 Hz clock. The corresponding 3-bit read address sequentially accesses the entered data for serial output on the TTYOWI line to the MO/C card. Each bit of 1200-baud data is entered and accessed once; however, each bit of the slower 75-baud data is entered and accessed 16 times before its following bit is entered.

(4) The rate comparator monitors the write and read address lines to the elastic storage register. When the addresses are separated by the desired four counts, the RTTYOW output remains low. When the read and write address separation narrows to three counts, the comparator puts its RTTYOW output high. This high requests that the MO/C card initiate a stuff action.

2-37. Theory of Operation

(fig. FO-8)

a. General. This paragraph describes the detailed operation of the circuits on DDOW encoder card 21A3. The theory of operation is divided into the five functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Input circuits (*b* below)
(2) Timing extractor (*c* below)
(3) Clock generator (*d* below)
(4) Ring/ready code generator (*e* below)
(5) Input rate buffer (*f* below)

NOTE

The sheet number references in *b* through *f* below refer to figure FO-8.

b. Input Circuits (sheet 3).

(1) The level shifter consists of comparator U22 and its input/output voltage divider networks. The level shifter converts received D12I line level signals to TTL levels for on-card processing. The D12I signal applied across input voltage divider R20, R21 is a forward current for a mark and a reverse current for a space. Each mark (electron flow from ground through resistors R20 and R21) develops about +0.8 v at the R20, R21 junction. Each space (electron flow through resistors R21 and R20 to ground) develops about −0.8 v at the R20, R21, junction. The junction voltage controls comparator U22 by its noninverting input pin U22-2. A received mark (+0.8 v at U22-2) drives output pin U22-7 to approximately +3.5 v; a received space drives pin U22-7 to approximately 0 v. U16-12 inverts the output of U22-7 so that a logic 1 represents a space and a logic 0 represents a mark (this also is the polarity that will untimately be inserted into the SG). Back-to-back zener diodes VR 2 and VR3 protect U22 from voltages that may exceed ±8.2 v. Zener diode VR1 holds the resistor R11, R12 junction at −6.2 v to provide the V_{CC-} input for U22. Resistor R12 limits current flow through VR1. R11's 3900-ohm resistance ensures adequate current for TTL level operation of inverter U16-12. Feedback resistor R8 minimizes hysteresis deviation effects on rising and falling swings at U22-7.

(2) The positioning of rate switch jumper plug P2 in J1 and J2 or in J2 and J3 configures DDOW encoder card circuits for processing 1200-baud or 75-baud digital data, respectively. Plugged into J1 and J2, P2 grounds the D75EN line to data and timing selector U17 and to timing extractor end-of-character gate U20-12. The D75EN low inhibits operation of the 75-baud select gates in both circuits. At the same time, D75EN inverts to a pin U16-8 D12EN high that lets

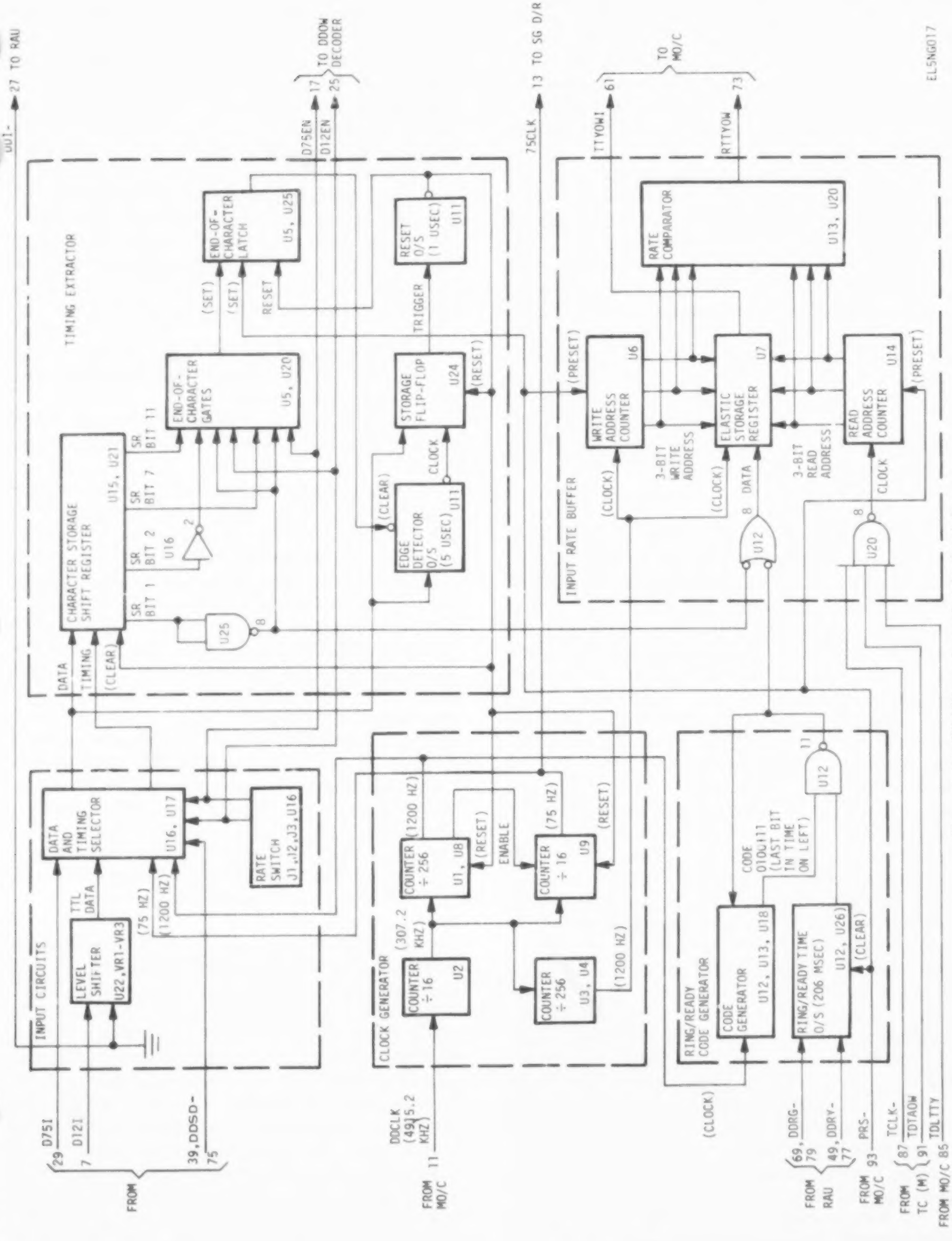

INPUT CIRCUITS
LEVEL SHIFTER U22, VR1-VR3
TTL DATA
DATA AND TIMING SELECTOR U16, U17
RATE SWITCH J1, J2, J3, U16
(75 HZ)
(1200 HZ)
TIMING EXTRACTOR
CHARACTER STORAGE SHIFT REGISTER U15, U21
DATA
TIMING
(CLEAR)
SR BIT 1
SR BIT 2
SR BIT 7
SR BIT 11
U16
U25
END-OF-CHARACTER GATES U5, U20
END-OF-CHARACTER LATCH U5, U25
(SET)
RESET
RESET O/S (1 USEC) U11
TRIGGER
STORAGE FLIP-FLOP U24
(RESET)
CLOCK
EDGE DETECTOR O/S (5 USEC) U11
(CLEAR)
CLOCK GENERATOR
COUNTER ÷ 16 U2
(307.2 KHZ)
COUNTER ÷ 256 U1, U8
(1200 HZ)
(RESET)
ENABLE
COUNTER ÷ 16 U9
(75 HZ)
COUNTER ÷ 256 U3, U4
INPUT RATE BUFFER
WRITE ADDRESS COUNTER U6
(PRESET)
(CLOCK)
3-BIT WRITE ADDRESS
ELASTIC STORAGE REGISTER U7
DATA
U12
3-BIT READ ADDRESS
READ ADDRESS COUNTER U14
U20
RATE COMPARATOR U13, U20
RING/READY CODE GENERATOR
CODE GENERATOR U12, U13, U18
CODE 0100111 (LAST BIT IN TIME ON LEFT)
RING/READY TIME O/S (206 MSEC) U12, U26
DUI- 27 TO RAU
D75EN 17
D12EN 25
TO DDOW DECODER
75CLK 13 TO SG D/R
TTYOWI 61
RTTYOW 73
TO MO/C
EL5NG017
FROM 29 D75I
7 D12I
39, DDSD- 75
FROM MO/C 11 DDCLK (4915.2 KHZ)
FROM RAU 69, 79 DDRG-
49, 77 DDRY-
FROM MO/C 93 PRS-
FROM TC (M) 87 TCLK-
91 TDTAOW
FROM MO/C 85 TDLTTY

Figure 2-17. DDOW encoder card 21A3, block diagram.

the 1200-baud select gates of both circuits operate. Plugging P2 into J2 and J3 lets +5 v pullup resistor R13 put the D75EN line high to the 75-baud select gates. In this configuration, the D75EN high inverts to a pin U16-8 D12EN low that inhibits operation of the 1200-baud select gates. The D75EN and D12EN signals also establish the data processing rate for the DDOW decoder card (section X).

(3) A DDSD— low inverting through U16-10 conditions both three-input gates of the data select portion (upper) of U17. For 75-baud data processing, a D75EN high applied to pins U17-13 and U17-2 enables passage of 75-baud digital data and 75 Hz clock signals. The data output at U16-4 (logic 1 represents a space and logic 0 represents a mark) goest directly to the timing extractor circuit's character storage shift register U15, storage flip-flop U24, and edge detector U11 (*c* below). The timing output at U16-6 goes through backplane jumper DECTO1 to clock input pins of character storage shift register U15,U21. For 1200-baud data processing, a D12EN high from U16-8 enables passage of 1200-baud digital data and 1200 Hz clock signals.

c. Timing Extractor.

(1) Edge detector one-shot U11-12 (sheet 4) is normally held in a clear state by the low applied to its reset pin U11-11 from end-of-character latch U5-6, U25-11 ((5) below) (sheet 3). When a complete character has been shifted into character storage shift register U15, U21 ((3) below), end-of-character gate U5-8 or U20-12 ((4) below) decodes this fact and sets end-of-character latch U5-6, U25-11 ((5) below). U5-6 then goes high, releasing edge detector U11-12 (sheet 4). The next positive transition on the data line triggers U11-12 into a 5-microsecond duty cycle (negative pulse at pin U11-12). Backplane jumper DECTO5 routes the negative pulse to clock storage flip-flop U24-10. If the data line is still high when U11-12 times out, the trailing (positive-going) edge of the negative pulse clocks the start bit (logic 1 represents a space) into U24-10 and sets it. The short duty cycle of U11-12 prevents inadvertent processing of sporadic noise spikes as start bits. When such a positive-voltage noise spike does appear on the data line, it triggers U11-12; however, since the spike is gone when U11-12 times out and clocks flip-flop U24-10, the flip-flop remains reset. Once a valid start bit detect action resets end-of-character latch U5-6, U25-11 ((2) and (5) below), the latch returns a clear low to pin U11-11. This low inhibits U11-12 so that it cannot be retriggered by code bit logic 1's (highs) of the coded character being processed. An end-of-character detect removes the inhibit low so that U11-12 can be triggered again by the next character's start bit.

(2) Storage flip-flop U24-10 and reset one-shot U11-4 (sheet 4) initiate and generate a brief reset pulse each time a valid start bit is detected. The entire initiate/generate/reset cycle occurs as follows. The trailing edge of the negative clock pulse from U11-12 ((1) above) clocks the start bit into storage flip-flop U24-10, putting its pin U24-10 high. This positive transition triggers reset one-short U11-4, which puts its pin U11-4 low for about 1 microsecond. This low loops through backplane jumper DECTO4 and performs the following timing alignment functions.

(*a*) It resets storage flip-flop U24-10 to condition it for the next character's start bit.

(*b*) It briefly resets and restarts divide-by-16 counters U1, U8, U9 to align their 1200 Hz clock positive transitions with the coded character bits being shifted into the character storage shift register ((3) below).

(*c*) It clears character storage shift register U15, U21 (sheet 3) for shift-in of a coded character's start, code, and stop bits.

(*d*) It resets end-of-character latch U5-6, U25-11 to inhibit operation of one-shot U11-12 ((1) above).

(3) The character storage shift register consists of series-connected 4-bit and 8-bit shift registers (U15 and U21) (sheet 3). The register receives 75-baud or 1200-baud data from U16-4 (*b*(3) above). An applicable 75 Hz or 1200 Hz clock timing signal from U16-6 accompanies the selected data and clocks the shift register. A clear low from reset one-shot U11-4 (sheet 4) briefly clears shift register U15, U21 about 5 microseconds after the leading edge of a coded character's start bit is detected ((2) above). The same clear low restarts a clock generator (*d*(2) below) whose clock signal applied to pins U15-10 and U21-8 (sheet 3) shifts in successive coded character bits. The clock positive transitions occur at about midpoint of a coded character's logic bits. The shift register provides parallel outputs (bits 1, 2, 7, and 11) to the end-of-character gates ((4) below). The bit 1 output (pin U15-15) output inverts through U25-8 for processing through the input rate buffer (*f*(3) below) and subsequent output to the MO/C card (section V).

(4) End-of-character gate U20-12 or U5-8 (sheet 3) sets end-of-character latch U5-6,U25-11 upon detecting a coded character's start and stop bits in the character storage shift register. Upon being conditioned by a pin 2 input D75EN high, three-input gate U20-12 monitors successive Baudot coded characters passing through the character storage shift register. U20-12 looks for simultaneous register bit 7 (pin U21-5) and register bit 1 (pin U15-15 inverted by U25-8) highs. The two highs coincide when a Baudot coded character with start and stop bits (para 2-35) is fully entered into the register. At that instant, a pin U21-5 (register bit 7) (start bit) high appears at pin U20-13, while a pin U15-15 (register bit 1) (stop bit)

low goes high trhough U25-8 to pin U20-1. The two highs enable U20-12, which sets end-of-character latch U5-6,U35-11. A D12EN high conditions four-input gate U5-8 for a 1200-baud data processing operation. U5-8 monitors start and stop bits of successive ASCII coded characters passing through the register. U5-8 looks for simultaneous register bit 11 (pin U21-12), register bit 2 (pin U15-14 inverted by U16-2), and register bit 1 (pin U15-15 inverted by U25-8) highs. The three highs coincide when any ASCII coded character with start and stop bits (para 2-35) is fully entered into the register. At that instant, the following three highs enable U5-8, which sets end-of-character latch U5-6, U25-11.

(*a*) A pin U21-12 (register bit 11) (start bit) high appears at pin U5-9.

(*b*) A pin U15-14 (register bit 2) (first stop bit) low goes high through U16-2 to pin U5-12.

(*c*) A pin U15-15 (register bit 1) (second stop bit) low goes high through U25-8 to pin U5-13.

(5) End-of-character latch U5-6,U25-11 (sheet 3) alternately enables and inhibits operation of edge detector one-shot U11-12 ((1) above). A PRS—low initially sets the latch by its pin U5-1 input upon equipment power turn on. The latch remains set (U11-12 enabled) until the first start bit of a TTY digital data character arrives. The coded character's start bit initiates a one-shot U11-12, flip-flop U24-10, one-shot U11-4 trigger-set-trigger sequence that ends with the latch being reset. Upon being reset, the latch puts its pin U5-6 output low to edge detector one-shot pin U11-11 (sheet 4). This low inhibits the one-shot so that it cannot be retriggered by code bit logic 1's (highs) of the coded character being processed. The latch remains reset until one of the end-of-character gates ((4) above) sets the latch. Setting of the latch removes the low (inhibit) from one-shot pin U11-11 so that the one-shot can be triggered again by the next character's start bit.

d. Clock Generator (sheet 4).

(1) Counter U2 is clocked by the 4915.2 kHz DDCLK from MO/C card 21A4 and performs a divide-by-16 function to provide a pin U2-11 307.2 kHz output. This output is applied to controlled counters U1,U8,U9 and to free-running counter U4, U3.

(2) Controlled counter U1, U8 performs a divide-by-256 function that provides a 1200 Hz clock to data and timing selector U17 (*b*)(3) above), to divide-by-16 counter U9 ((3) below), and to the ring/ready code generator (*e* below). A reset pulse from one-shot U11-4 (c(2) above) restarts counter U1,U8 for each received coded character. The 307.2 kHz clock output from U3-11 increments counter U1, which produces a 19.2 kHz clock train at output pin U1-15 that lets a 307.2 kHz positive transition increment counter U8 once. Thus incremented at a 19.2 kHz rate, U8 divides its input pin U8-2 307.2 kHz clock by 256 for a 1200 Hz output a pin U8-11. The counter also provides a pin U8-15 1200 Hz output to divide-by-16 counter U9.

(3) Counter U9 provides a pin U9-11 75 Hz output and timing selector U17 (*b*(3) above). Each positive pulse from U8-15 lets a 307.2 Khz clock positive transition increment counter U9 once. Thus incremented at a 1200 Hz rate, the counter produces a 75 Hz output at its pin U9-11.

(4) Free-running divide-by-256 counter U4, U3 operates continuously while equipment power is applied. This counter operates like counter U1, U8 ((2) above). This is, a 307.2 kHz clock increments U4 whose 19.2 kHz pin U4-15 output lets 307.2 kHz clock positive transitions increment U3. This counter's pin U3-11 1200 Hz clock output goes through backplane jumper DECTO3 to the input rate buffer (*f* below).

e. Ring/Ready Code Generator (sheet 5).

(1) Gate U12-6 and one-shot U26-5 make up the ring/ready time one-shot. Upon equipment power turn-on, a PRS— low from the MO/C card to one-shot clear pin U26-11 inhibits the one-shot until equipment dc voltages reach desired operating levels. Subsequent receipt of a DDRY— low from TTY RCV-OFF-READY switch S2 or a DDRG— low from TTY SEND-OFF-RING switch S3 on the RAU initiates a ring/ready code output cycle.

(2) Either of the received lows goes high through U12-6 to one shot pin U26-10 and triggers the one-shot into a 206-millisecond duty cycle. The one-shot's output pin U26-5 high goes through backplane jumper DECTO2 to code output gate pin U12-13. This applied high lets gate U12-11 pass a repetitive 7-bit ring/ready code pattern to the input rate buffer (*f* below). Gate U12-11 passes about 35 ring/ready code patterns before the one-shot's duty cycle expires and its pin U26-5 output goes low.

(3) The code generator consists of shift register U18, XOR gate U13-3, and two-input gates U12-3 and U12-11. Pullup resistor R19 lets U18 operate continuously while equipment power is applied. Between ring/ready code cycles, a pin U12-11 high lets a 1200 Hz clock shift logic 1's into the shift register through its J-K pins U18-2 and U18-3. When two logic 1's reach the register's bit 2 and bit 3 stages, its pin U18-14 and U18-13 output highs enable U12-3. This lets the next clock positive transition parallel-load (preset) a hard-wired 101 pattern into the register. Two clock transitions later, pin U18-14 and U18-13 highs enable U12-3 to preset the shift register again. U18 idles in this manner until a 206-milisecond ring/ready cycle starts. At that time, a high applied through backplane jumper DECTO2 to pin U12-13 lets XOR gate U13-3 control the J-K inputs to U18.

(4) XOR gate U13-3 and gate U12-3 monitor

shift register bit 2 and bit 3 stage outputs. U12-3 enables a U18 preset action each time the register's bit 2 and bit 3 are high. XOR gate U13-3's output goes high and enables U12-11 each time the register's bit 2 and bit 3 differ. Gate U12-11 returns a logic 0 or a logic 1 to U18 when enabled or inhibited, respectively, by XOR gate U13-3. This activity generates the following repetitive 7-bit ring/ready code pattern at XOR gate pin U13-3 (0100111, last bit in time on left).

f. Input Rate Buffer (sheet 5).

(1) Write address counter U6 is initially preset to a count of 4 (0010) by PRS—. It is then clocked by a 1200 Hz clock applied through backplane jumper DECT03 and sequentially generates 3-bit binary write addresses for serially entering (writing) data bits (either coded character or ring/ready pattern) into elastic storage register U7 ((3) below). The counter's binary 2^0 (pin U6-14), 2^1 (pin U6-13), and 2^2 (pin U6-12) address outputs go to the elastic storage register's write address input pins and to rate comparator U13, U20 ((4) below). The address outputs increment to count 7(111) and then continue recycling from count 0 through count 7.

(2) Read address counter U14 is initially preset to a count of 0 (0000) (four counts behind the write address counter) by PRS—. Each coincidence of a TCLK— and a TDTAOW (coincidences occur at the digital data sampling rate of 1201 Hz), unless inhibited by a TDLTTY, enables U20-8 to clock U14. Thus clocked, U14 sequentially generates 3-bit binary read addresses for serially accessing (reading) data bits from elastic storage register U7 as the TTYOWI output to the MO/C card. The counter's three binary outputs go to the read address inputs of U7 and to rate comparator U13, U20. Because the coincidences of TCLK—'s and TDTAOW's occur at a slightly higher rate (nominal 1201 Hz) than the write clocks (nominal 1200 Hz), read counter U14 advances on write counter U6. When U14 advances to within three counts of U6, the rate comparator ((4) below) generates an RTTYOW high requesting that a staff action be performed. The stuff request circuits on MO/C card 21A4 recognize this condition and, at the proper time, put TDLTTY low for one coincidence of the TCLK— and TDTAOW, thus inhibiting U20-8 from clocking U14. This inhibiting of one read clock (stuffing) reestablishes the desired four-count offset between the two counters.

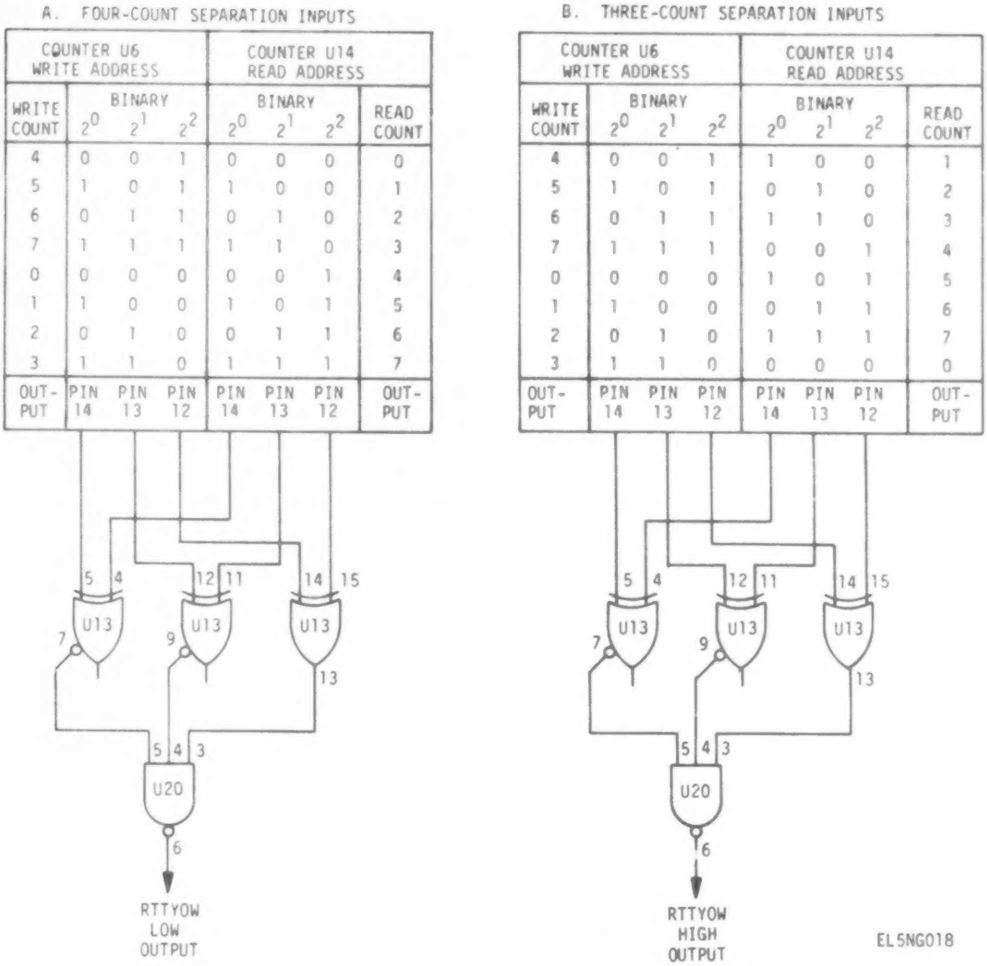
(3) Eight-bit elastic storage register U7 temporarily stores received asynchronous data for synchronous output to MO/C card 21A4. Gate U12-8 provides the means for serially applying either TTY (coded character) data or a ring/ready pattern to register data input pin U7-12. Inverted TTY data (pin U12-9) comes from U25-8 at the bit 1 output of the character storage shift register. The inverted ring/ready pattern (pin U12-10) comes from the ring/ready code generator. The data or pattern bits are restored to their true logic levels at pin U12-8. Counter U6 write addresses at register pins U7-15, U7-14, and U7-13 sequentially select the register's bit 1 through bit 8 cells for clock-in of applied data or pattern bits. Counter U14 read addresses at register pins U7-1, U7-2, and U7-3 sequentially access the data or pattern bits for output at pin U7-4. Since the read addresses lag the write addresses by four counts, each bit entered by a write address and a clock transition is accessed four counts later by a corresponding read address. Rate comparator U13, U20 ensures that write and read addresses remain separated by four counts. In 75-baud data processing operations, each bit of a coded character persists at the elastic storage register's input pin U7-12 about 13.33 milliseconds. Since the register's write and read addresses increment once every 0.833 millisecond, each 75-baud data bit is entered and accessed 16 times.

(4) The rate comparator consists of three XOR gates U13 and output gate U20-6. Each XOR gate monitors corresponding count output lines from write and read address counters U6 and U14. An XOR gate's noninverting output goes high or its inverting output goes low only when its two inputs differ. While corresponding counter U6 write addresses and counter U14 read addresses remain separated by four counts (A, fig. 2-18), three highs from XOR gates U13 hold the U20-6 RTTYOW output low. For example, in a write count 3/read count 7 condition, a matching 2^0 pair (11) holds pin U13-7 high, a matching 2^1 pair (11) holds pin U13-9 high, and a differing 2^2 pair (01) holds pin U13-13 high. The three highs hold U20-6 RTTYOW low to MO/C card 21A4. When any counter U14 address advances to within three counts of a corresponding counter U6 address (B, fig. 2-18), at least one XOR gate output low inhibits U20-6, putting RTTYOW high. For example, in a write count 3/read count 0 condition, a differing 2^0 pair (10) holds pin U13-7 low, putting U20-6 RTTYOW high to MO/C card 21A4. The MO/C card's subsequent return of a TDLTTY low to U20-8 ((2) above) blocks one counter U14 clock pulse (stuff action) so that its read addresses again lag counter U16 write addresses by four counts.

Section X. DIGITAL DATA ORDERWIRE (DDOW) DECODER CARD 21A8

2-38. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the DDOW decoder card. There is one DDOW decoder card (21A8) in the TD-976/G. The card extracts TTY digital data from the incoming SG data stream, and then processes the data out as asynchronous digital data. An on-card ring/ready pattern



A. FOUR-COUNT SEPARATION INPUTS

COUNTER U6 WRITE ADDRESS				COUNTER U14 READ ADDRESS			
WRITE COUNT	BINARY 2^0	2^1	2^2	BINARY 2^0	2^1	2^2	READ COUNT
4	0	0	1	0	0	0	0
5	1	0	1	1	0	0	1
6	0	1	1	0	1	0	2
7	1	1	1	1	1	0	3
0	0	0	0	0	0	1	4
1	1	0	0	1	0	1	5
2	0	1	0	0	1	1	6
3	1	1	0	1	1	1	7
OUTPUT	PIN 14	PIN 13	PIN 12	PIN 14	PIN 13	PIN 12	OUTPUT

B. THREE-COUNT SEPARATION INPUTS

COUNTER U6 WRITE ADDRESS				COUNTER U14 READ ADDRESS			
WRITE COUNT	BINARY 2^0	2^1	2^2	BINARY 2^0	2^1	2^2	READ COUNT
4	0	0	1	1	0	0	1
5	1	0	1	0	1	0	2
6	0	1	1	1	1	0	3
7	1	1	1	0	0	1	4
0	0	0	0	1	0	1	5
1	1	0	0	0	1	1	6
2	0	1	0	1	1	1	7
3	1	1	0	0	0	0	0
OUTPUT	PIN 14	PIN 13	PIN 12	PIN 14	PIN 13	PIN 12	OUTPUT

Figure 2-18. Rate comparator logic operating conditions.

detector, upon detecting a series of incoming ring/ready patterns, causes the TTY CALL indicator on the RAU to light. A smoothing buffer provides the means for smoothing the extracted TTY data and outputting it through output circuits to the RAU for interface with a local TTY unit. The block diagram discussion in paragraph 2-39 is based on the block diagram in figure 2-19. The detailed theory of operation in paragraph 2-40 is based on the DDOW decoder card schematic diagram in figure FO-9.

2-39. Block Diagram Discussion

(fig. 2-19)

a. General. The block diagram discussion is divided into six functional circuit descriptions as follows:

(1) The divide-by-4096 counter (*b* below) generates a 1200 Hz clock signal for timing all DDOW decoder card functional circuits except the elastic storage register and write address counter in the smoothing buffer.

(2) The smoothing buffer (*c* below) extracts TTY data from the incoming SG and temporarily stores the data for smooth input through the RAU to a local TTY unit. A write address counter controls entry of the serial TTY data bits into an elastic storage register for accessing by a read address counter.

(3) Two separate output circuits (*d* below) convert TTL level data to compatible signal levels for transmission through the RAU to a local TTY unit. 75-baud data are passed through an optical coupler in the RAU.

(4) The resync circuit (*e* below) regularly presets the read and write address counters to count 4 and 0 states, respectively, when the TTY switches on the RAU are placed to OFF and a TTY call is not being received.

(5) The call circuits (*f* below) generate a call signal each time a ring/ready pattern sequence is detected by the ring/ready pattern detector. The call signal ultimately lights the TTY CALL indicator on the RAU.

(6) The ring/ready pattern detector and counter (*g*

below) monitors and counts incoming ring/ready patterns. The counter sets the call latch after a cumulative total of eight ring/ready patterns has been detected.

b. Divide-by-4096 Counter. A 4915.2 kHz receive master clock (RMASCLK) signal from SG D/R card 21A9, which is synchronous with the incoming SG, drives this counter's three divide-by-16 sections. The counter progressively divides the RMASCLK input down to 307.2 kHz, 19.2 kHz, and finally to a 1200 Hz square wave output. Inverter U3-12 complements the 1200 Hz square wave for use as the clock input to the smoothing buffer's read address counter, output interface circuit flip-flops, ring/ready pattern detector and counter, and resync circuit.

c. Smoothing Buffer. The smoothing buffer extracts the TTY data bits from the incoming SG data (SDATA) line under control of a write counter. A read address counter accesses the extracted data for application to the output circuits and to a ring/ready pattern detector and counter.

(1) The read and write address counters are preset with a four-count offset (write counter preset to a count of 0 and read counter preset to a count of 4) as controlled by gate U22-6 and inverter U3-4. A power-on reset (PRS—), a receive major frame sync level 8 (SYNC 8—), or a resync— signal controls the presetting operation.

(2) Each coincidence of a receive clock (RCLK—) and a receive digital data orderwire (RDTAOW) signal (coincidences occur at a nominal 1201 Hz digital data sampling rate), unless inhibited by a receive delete (RDLTTY), is gated through U18-6 to clock the write address counter and elastic storage register. RDLTTY goes low whenever the demultiplexer section is to accomplish a destuff action to compensate for a stuff action transmitted by the far-end multiplexer section (destuff actions for TTY data occur at a nominal 1 Hz rate). As a result of destuff actions, the output pulses of U18-6 occur at the average rate of the received TTY data (1200 Hz), but are not regularly (uniformly) spaced. The clock output of U3-2 occurs each time a TTY data bit appears on the SDATA line and enables that data bit to be entered into the elastic storage register. The write address counter generates a 3-bit write address that sequentially selects the eight cells of the elastic storage register into which the data bits will be entered.

(3) The read address counter (which lags the write address counter by four counts) is clocked at a nominal 1200 Hz smooth rate and generates 3-bit read address outputs to the elastic storage register. The read address outputs sequentially access elastic storage register cells for transfer of TTY data bits to two output interface circuits and a ring/ready pattern detector.

d. Output Circuits. The output circuits convert TTL level data from the smoothing buffer to compatible interface signal levels for transmission through the RAU to a local TTY unit.

(1) Digital data 75-baud enable (D75EN) and digital data 1200-baud enable (D12EN) signals from the DDOW encoder card rate switch (para 2-36*b*) cause the selection circuits to select the appropriate output interface circuit. Coinciding SYNC 8—, D75EN, and digital data received (DDRV) highs enable 75-baud output interface circuit operation. Coinciding SYNC 8—, D12EN, and DDRV highs enable 1200-baud output interface circuit operation.

(2) The 1200-baud output interface circuit has a data flip-flop (U4) that applies TTY data to a voltage divider in response to a 1200 Hz clock. An output amplifier (U26) converts the applied TTL level signals to +6 v and −6 v level outputs (logic 1 representing a space is converted to −6 v and logic 0 representing a mark is converted to +6 v). Back-to-back zener diodes (VR1, VR2) limit the output signal positive and negative voltage levels. The +6 v and −6 v D120 output signal goes through RAU jumper switches to a local TTY unit.

(3) The 75-baud output interface circuit has a flip-flop (U4) that applies the data to an output driver (Q1). Data logic 1's (spaces) and 0's (marks) switch the driver off and on, respectively. Q1 operates an optical coupler in the RAU that provides the interface to a local TTY unit for 75-baud operation.

e. Resync Circuit. The resync circuit functions when the TTY switches on the RAU are placed to OFF and the call latch is not set. During these conditions, the resync circuit continually goes through a cycle of presetting the write and read counters to a count of 0 and 4, respectively, then letting them operate for a 206-millisecond period to handle any received ring/ready patterns, then presetting them again, and so on.

(1) An eight-input gate (U21) monitors DDRV—, digital data send (DDSD—), digital data call (DDCAL—), digital data ring (DDRG—), and digital data ready (DDRY—) signals. It also monitors a receive last bit of major frame (RLBMF) signal and a 206-millisecond strobe signal initiated by it. While all inputs are high, gate U21 holds a resync flip-flop (U14) reset and its resync— output low. This low holds the smoothing buffer's write and read address counters in their preset states. Any input signal going low inhibits gate U21, which lets a clock pulse set flip-flop U14 and puts its resync— output high. The resync— high releases the write and read counters to operate from their count 0 and count 4 preset states.

(2) A strobe one-shot (U10) generates a 206-millisecond low each time it has timed out and RLBMF— goes high. The one-shot U10 output puts resync— high so that the write and read address counters can operate long enough (206 milli-seconds) to handle any re-

ceived series of ring/ready patterns.

f. Call Circuits. These circuits have a call latch (U13, U20) and a latch reset one-shot (U10) with an input gate (U20). The call circuits generate a digital data call (DDCAL—) low that ultimately lights the TTY CALL indicator on the RAU when an incoming series of ring/ready patterns has been detected.

(1) A power-on reset (PRS—) low initially resets the call latch, putting DDCAL— high. Subsequent detection of a cumulative total of eight ring/ready patterns causes the ring/ready pattern confidence counter to set the latch, putting DDCAL— low. This low holds resync— high so that write and read address counters will continue operating for received TTY data. The DDCAL— low also lights on the TTY CALL indicator on the RAU by means of the AD card's orderwire control circuit.

(2) Setting one of the TTY switches on the RAU to READY or SEND puts DDRY— or DDSD— low. Either low going high through gate U20 triggers latch reset on-shot U10. A 7-microsecond low from the one-shot resets call latch U13, U20. The call latch remains reset until another series of ring/ready patterns is detected.

g. Ring/Ready Pattern Detector and Counter. The ring/ready pattern detector monitors incoming data for ring/ready patterns. Upon detecting the first pattern, the detector decrements a confidence counter that enables a spacing counter. The spacing counter subsequently enables the confidence counter only when another pattern is expected. Detection of a cumulative total of eight ring/ready patterns decrements the confidence counter to a count of 7 and sets the call latch (*f*(1) above).

(1) Two gates (U11 and U13) monitor data passing through a shift register (U12). Presence of a 7-bit ring/ready pattern (0100111, last bit in time on left) in the shift register generates a pattern detected low. The low lets a clock pulse decrement confidence counter U9 one count from its count 15 (1111) preset state. Detection of each subsequent ring/ready pattern also decrements counter U9. Also, nondetection of an expected pattern increments counter U9 one count. When the counter has decremented a cumulative total of eight counts, it sets call latch U13, U20.

(2) Upon being decremented to a count of 14 by the first pattern detect low, counter U9 puts its maximum/minimum output low to the spacing counter. The spacing counter now enables the confidence counter every seventh count at the time a ring/ready pattern is expected in the pattern detector. When the confidence counter has decremented to a count of 0000, it puts its maximum/minimum output high again to inhibit spacing counter enabling of U9.

2-40. Theory of Operation

(fig. FO-9)

a. General. This paragraph describes the detailed operation of the circuits on DDOW decoder card 21A8. The theory of operation is divided into the six functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Divide-by-4096 counter (*b* below).
(2) Smoothing buffer (*c* below).
(3) Output circuits (*d* below).
(4) Resync circuit (*e* below).
(5) Call circuits (*f* below).
(6) Ring/ready pattern detector and counter (*g* below)

NOTE

The sheet number references in *b* through *g* below refer to figure FO-9.

b. Divide-by-4096 Counter. Three 4-bit binary up counters U2, U1, and U15 (sheet 2) make up the divide-by-4096 counter. Each counter performs a divide-by-16 function. A 4915.2 kHz receive master clock (RMASCLK), which is extracted from the incoming SG by SG D/R card 21A9, continuously increments U2 to produce a positive pulse at a 307.2 kHz rate at its terminal count (TC) output pin U2-15. Each 307.2 kHz positive pulse at the next counter (pin U1-10) lets a 4915.2 kHz clock positive transition increment that counter once. This intermittent clocking action produces a 19.2 kHz positive pulse at TC pin U1-15. The 19.2 kHz positive pulses similarly let 4915.2 kHz clock positive transitions increment counter U15. A 1200 Hz square wave output produced at pin U15-11 goes out through backplane jumper DDCT04 and inverts through U3-12 (sheet 4) for on-card timing of all functional circuits except elastic storage register U6 and write address counter U7 (sheet 3).

c. Smoothing Buffer (sheet 3).

(1) Read address counter U5 and write address counter U7 are preset with a four-count offset (U5 preset to a count of 4 and U7 reset to a count of 0) as controlled by gate U22-6 and inverter U3-4. During initial equipment power on, a PRS— low applied to pin U22-5 holds U5 and U7 in their preset states. Whenever the major frame sync confidence counter on FS card 21A7 has advanced to a count of 8 (indicating a declining confidence in major frame sync status), SYNC 8— applied to pin U22-3 is low and holds U5 and U7 in their preset states. When the TTY switches on the RAU are placed to OFF and a call is not being received, the resync circuit (*e*(1) below) periodically applies a low to pin U22-4 to preset U5 and U7.

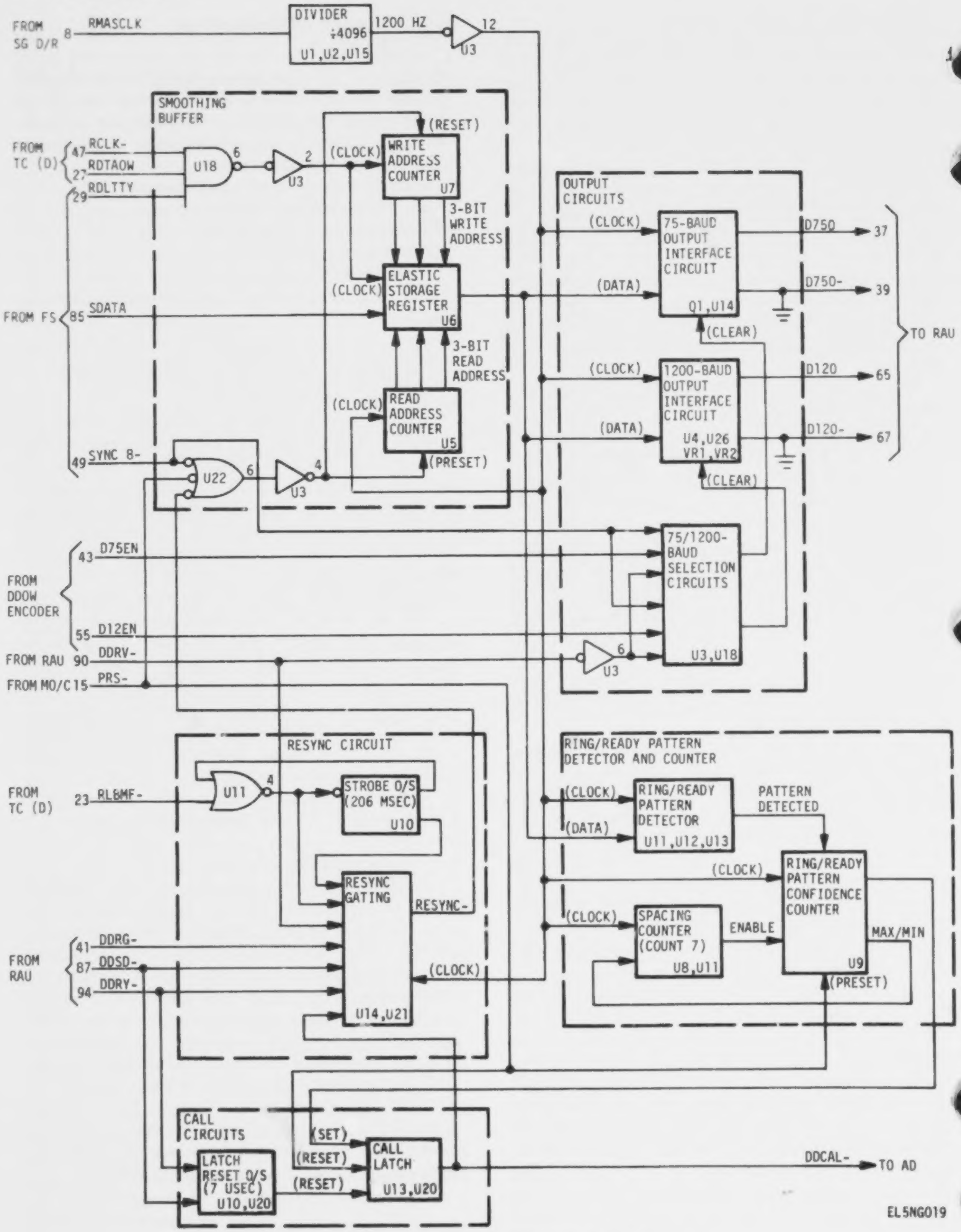

FROM SG D/R
8
RMASCLK
DIVIDER ÷4096 U1,U2,U15
1200 HZ
U3
12
SMOOTHING BUFFER
(RESET)
FROM TC (D)
47 RCLK-
27 RDTAOW
29 RDLTTY
U18
6
U3
2
(CLOCK)
WRITE ADDRESS COUNTER U7
3-BIT WRITE ADDRESS
(CLOCK)
ELASTIC STORAGE REGISTER U6
FROM FS
85 SDATA
3-BIT READ ADDRESS
(CLOCK)
READ ADDRESS COUNTER U5
(PRESET)
49 SYNC 8-
U22
6
U3
4
OUTPUT CIRCUITS
(CLOCK)
75-BAUD OUTPUT INTERFACE CIRCUIT Q1,U14
(DATA)
(CLEAR)
D750
37
D750-
39
TO RAU
(CLOCK)
1200-BAUD OUTPUT INTERFACE CIRCUIT U4,U26 VR1,VR2
(DATA)
(CLEAR)
D120
65
D120-
67
75/1200-BAUD SELECTION CIRCUITS U3,U18
FROM DDOW ENCODER
43 D75EN
55 D12EN
FROM RAU 90 DDRV-
U3
6
FROM MO/C 15 PRS-
RESYNC CIRCUIT
FROM TC (D)
23 RLBMF-
U11
4
STROBE O/S (206 MSEC) U10
RESYNC GATING
RESYNC-
(CLOCK)
U14,U21
FROM RAU
41 DDRG-
87 DDSD-
94 DDRY-
RING/READY PATTERN DETECTOR AND COUNTER
(CLOCK)
(DATA)
RING/READY PATTERN DETECTOR U11,U12,U13
PATTERN DETECTED
(CLOCK)
RING/READY PATTERN CONFIDENCE COUNTER U9
(CLOCK)
SPACING COUNTER (COUNT 7) U8,U11
ENABLE
MAX/MIN
(PRESET)
CALL CIRCUITS
LATCH RESET O/S (7 USEC) U10,U20
(SET)
(RESET)
(RESET)
CALL LATCH U13,U20
DDCAL-
TO AD
EL5NG019

Figure 2-19. DDOW decoder card 21A8, block diagram.

(2) Gate U18-6 controls application of RCLK— pulses to clock write address counter U7 and elastic storage register U6. Each coincidence of an RCLK— and an RDTAOW (coincidences occur at a nominal 1201 Hz digital data sampling rate), unless inhibited by an RDLTTY, is gated through U18-6 to clock U6 and U7. RDLTTY goes low whenever the demultiplexer section is to accomplish a destuff action to compensate for a stuff action transmitted by the far-end multiplexer section (destuff actions for TTY data occur at a nominal 1 Hz rate). As a result of destuff actions, the output pulses of U18-6 to clock U6 and U7. RDLTTY goes low whenever the demultiplexer section is to accomplish a destuff action to compensate for a stuff action transmitted by the far-end multiplexer section (destuff actions for TTY data occur at a nominal 1 Hz rate). As a result of destuff action, the output pulses of U18-6 occur at the average rate of the received TTY data (1200 Hz), but are not regularly (uniformly) spaced. The clock output of U3-2 occurs each time a TTY data bit appears on the SDATA line and enables that data bit to be entered into U6. The binary 2^0 (pin U7-14), 2^1 (pin U7-13), and 2^2 (pin U7-12) outputs of U7 go to U6 and address the cell into which the data bit will be entered.

(3) Read address counter U5 (which lags U7 by four counts) is clocked at a nominal 1200 Hz smooth rate by the output of inverter U3-12 (*b* above). The binary 2^0 (pin U5-14), 2^1 (pin U5-13), and 2^2 (pin U5-12) outputs of U5 address U6 as to which cell of U6 will be accessed and appear at output pin U6-4. The data output of U6 is applied to two output interface circuits (*d* below) and a ring/ready pattern detector (*g* below).

d. Output Circuits (sheet 4).

(1) The 75-baud output interface circuit consists of gate U18-12, inverter U3-10, flip-flop U4-9, resistor R8, and transistor Q1.

(*a*) Gate U18-12 provides the means for selecting the 75-baud output by a D75EN high from the rate switch on DDOW encoder card 21A3 (para 2-37*b*(2)). Additional control level requirements are a digital data receive (DDRV) high from inverter pin U3-6 and a SYNC 8— high from FS card 21A7. The three coinciding input highs put gate pin U18-12 low. This low inverts through U3-10 to flip-flop pin U4-15 and lets the flip-flop operate.

(*b*) A 1200 Hz inverted clock from the divide-by-4096 counter (*b* above) clocks TTY data bits into flip-flop U4 through its J-K input pins U4-14 and U4-13. The flip-flop's pin U4-9 inverted output controls output driver transistor Q1.

(*c*) Each high from flip-flop pin U4-9 (logic 0 contained in flip-flop representing a mark) biases Q1 on. Q1 switch-on completes an electron path from ground through Q1 and through an optical coupler in the RAU to 24 v. The current flow closes the 75-baud output line current loop, denotign a mark. Each low from flip-flop pin U4-9 (logic 1 contained in flip-flop representing a space) biases Q1 off for no current through the optical coupler in the RAU and 75-baud line loop, denoting a space.

(2) A D12EN high similarly selects the 1200-baud output interface circuit consisting of gate U18-8, inverter U3-8, flip-flop U4-6, and inverting amplifier U26. Gate U18-8 also requires DDRV and SYNC 8— highs for selection of the 1200-buad output interface circuit.

(*a*) The flip-flop provides a pin U4-6 output to the R9, R10 junction of voltage divider R9, R10, R11 between +5 v and −12 v. Each high from pin U4-6 (logic 1 contained in flip-flop representing a space) develops about +2.5 v at the R10, R11 junction; each low (logic 0 contained in flip-flop representing a mark) develops about −1.5 v at the junction.

(*b*) U26 amplifies and inverts its inputs to +6 v (mark) and −6 v (space) outputs. Zener diodes VR1 and VR2 limit the amplifier's D120 output to ±6 v. Zener diodes VR3 and VR4 protect U26 from voltage surges on the D120 line by limiting the voltage to +8.2 v. The D120 output goes through jumper plugs on the RAU to a local TTY unit.

e. Resync Circuit.

(1) Gate U21-8 and flip-flop U14-6 (sheet 3), together with gate U11-4 and one-shot U10-5 (sheet 2), periodically preset the read and write address counters (*c* above) when the TTY switches on the RAU are placed to OFF and a call is not being received. Under these conditions, the following five inputs to U21-8 (sheet 3) are constantly high: DDRV— to pin U21-4, DDRG— to pin U21-11, DDSD— to pin U21-1, DDRY— to pin U21-13, and DDCAL— to pin U21-10. The input to pin U21-3 is high at all times except the last bit time of each major frame. Therefore, U21-8 is periodically enabled by a high to input pin U21-2 when U10-5 times out. When U21-8 is enabled, it resets flip-flop U14, causing its pin U14-6 to go low. This low is applied through U22-6 and U3-4 to preset the read and write counters. Conversely, when U21-8 is inhibited, the next positive transition of a 1200 Hz clock sets U14-6, which releases the read and write counters to operate.

(2) One-shot U10-5 (sheet 2) is triggered into a 206-millisecond duty cycle at the end of a major frame by an inverted RLBMF—. Once U10-5 is triggered, it is inhibited from being retriggered by the feedback to pin U11-2 until it completes its duty cycle. During the time U10-5 is in its duty cycle, its pin U10-12 output is low and is routed through backplane jumper DDCT01 to pin U21-2. This low inhibits gate U21-8 and allows the read and write counters to operate and pass any ring/ready pattern that may be in the in-

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coming SG. When U10-5 times out, its pin U10-12 goes high and enables gate U21-8 to initiate a preset action on the read and write counters. The next RLBMF— pulse triggers U10-5 to repeat the above cycle. When any TTY switch on the RAU is active or a call is being received, gate U21-8 is inhibited and the read and write counters are allowed to operate uninterrupted.

f. Call Circuits (sheet 2).

(1) A latch reset circuit, consisting of gate U21-11 and one-shot U10-4, generates a 7-microsecond reset pulse (low) in response to a DDRY— or DDSD— low from the two TTY switches on the RAU. Either low going high through the gate triggers the one-shot, and the one-shot resets call latch U20, U13 with a pin U10-4 low. This low goes through backplane jumper DDCTG3 to call latch pin U13-10.

(2) A PRS— low at call latch input pin U13-9 initially resets the latch upon equipment power turn-on. The latch remains reset until it receives a set (count down to 7) low from ring/ready pattern confidence counter U9 (*g*(2)(*c* below). Setting of the latch puts its pin U13-8 DDCAL— output low to the AD card's orderwire control circuit, which ultimately lights the TTY CALL indicator on the RAU.

g. Ring/Ready Pattern Detector and Counter (sheet 2).

(1) The ring/ready pattern detector consists of shift register U12 and gates U13-6 and U11-12. A 1200 Hz clock continuously clocks output data from elastic storage register U6 into U12. The two gates monitor the contents of U12 for a 0100111 (last bit in time on left) ring/ready pattern. Gate U13-6 looks for logic 1's at pins U12-4, U12-10, U12-11, and U12-12, while gate U11-12 looks for logic 0's at pins U12-3, U12-5, and U12-6, as well as a low from gate U13-6. Each time a ring/ready pattern appears in U12, pin U11-12 goes high and is routed through backplane jumper DDCT05 to confidence counter U9. This high lets a clock positive transition decrement the counter one count.

(2) Ring/ready confidence counter U9 counts the number of times a ring/ready pattern is detected. Gate U11-9 controls operation of the counter through inverter U11-7. A PRS— low initially presets counter U9 to a count 15 (1111) upon equipment power turn-on.

(*a*) While counter U9 is thus preset, a pin U9-5 low (ring/ready pattern not detected condition) holds the counter's maximum/minimum pin U9-12 high. The persistent high inhibits counter U9's enable control gate U11-9. During the inhibit condition, a pin U11-9 low goes high through inverter U11-7 to counter enable pin U9-4 and prevents the counter from operating.

(*b*) Subsequent detection of a ring/ready pattern ((1) above) puts the counter's down/up input pin U9 5 high for a complete clock period. This high (down count level) puts the maximum/minimum pin U9-12 output low to pin U11-11. Combined with a pin U11-10 low from spacing counter U8 ((3) below), gate pin U11-9 goes high. This high inverts to a pin U11-7 low, which lets a clock positive transition simultaneously decrement counter U9 once and preset spacing counter U8.

(*c*) Now, since the counter's maximum/minimum output can be put high only by an up enable low when the count is 1111 (maximum) or by a down enable high when the count is 0000 (minimum), the maximum/minimum output to pin U11-11 stays low. Spacing counter U8 takes control of gate U11-9 and subsequently lets the gate enable confidence counter U9 every seventh count. Each enable low coincides with an expected appearance of another ring/ready pattern in U12. If a 0100111 ring/ready pattern is contained in U12, a 1200 Hz clock positive transition decrements U9 once; if not, U9 is incremented one count. This every-seventh-count sampling activity continues until U9 has decremented to a count of 0000. However, at a count of 7 (0111), a counter 2^3 pin U9-7 low sets call latch U20, U13 (*f*(2) above), which lights the TTY CALL indicator on the RAU.

(*d*) When counter U9 has decremented to a count of 0000, its pin U9-12 maximum/minimum output stays high and inhibits counter operation until all ring/ready patterns (about 35) have passed through U12. Thereafter, 15 nondetect lows increment counter U9 to a count of 1111 so that it can respond to another ring/ready pattern.

(3) Spacing counter U8 times the sampling rate for confidence counter U9 while ring/ready patterns are being received. Although counter U8 operates continuously from equipment power turn-on, its pin U8-11 output is ignored until a ring/ready pattern appears in U12. Detection of this first pattern presets spacing counter U8 by gate U11-9 and inverter U11-7 to a count of 10 presets spacing counter U8 by gate U11-9 and inverter U11-7 to a count of 10 (1010). The next six clock positive transitions increment counter U8 from 1010 to 0000 and put its 2^3 pin U8-11 low. This low puts gate pin U11-9 high, which puts inverter pin U11-7 low. Each of these lows lets a 1200 Hz clock positive transition decrement confidence counter U9 once and also presets spacing counter U8 to a count of 10 (1010) again. The sequence of counting from 1010 to 0000, incrementing U9, and presetting U8 repeats until confidence counter U9 has decremented to a count of 0 (0000). Each enable U9 decrementing/incrementing and U8 presetting action is timed to coincide with the expected arrival of a 7-bit

ring/ready pattern in U12. When U9 has decremented to a count of 0000, a maximum/minimum high from pin U9-12 inhibits gate U11-9 to prevent operation of counter U9 and further presetting of counter U8.

Section XI. SUPERGROUP DRIVER/RECEIVER (SG D/R) CARD 21A9

2-41. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the SG D/R card. There is one SG D/R card (21A9) in the TD-976/G. The card contains circuits that process the SG input and SG output signals in the multiplexer and demultiplexer sections as described in the overall block diagram discussion. The block diagram discussion in paragraph 2-42 is based on the block diagram in figure 2-20. The detailed theory of operation in paragraph 2-43 is based on the SG D/R card schematic diagram in figure FO-10.

2-42. Block Diagram Discussion

(fig. 2-20)

a. General. The block diagram discussion is divided into three functional circuit descriptions as follows:

(1) The receiver section (*b* below) contains the circuits that receive the SG data in a ½-baud bipolar format and convert it to a TTL NRZ format for processing within the demultiplexer section.

(2) The driver section (*c* below) contains the circuits that convert the outgoing SG data from a TTL NRZ format to a ½-baud bipolar format for application to the cable system.

(3) The cable test clamp circuit (*d* below) functions only during cable testing operations.

b. Receiver Section.

(1) The SG input (SGIN1, SGIN2), which is in a bipolar format, is routed from the CABLE IN connector on the rear of the TD-976/G to the input line buildout network. The input line buildout network consists of one-half of the CABLE MILES switch and a quarter-mile attenuation network. The CABLE MILES switch is a two-position switch. When the switch is placed to the ½ position, the incoming bipolar signals are routed through the switch and applied directly to the input transformer. When the switch is placed to the ¼ position, the incoming bipolar signals are applied through the switch and the quarter-mile attenuation network to the input transformer. Signals applied through the quarter-mile attenuation network are attenuated by an amount that is equal to the signal loss that occurs in a quarter of a mile of transmission cable.

(2) The bipolar signals coupled through the input transformer are applied to the linear amplifier. The amplified signals from the amplifier are coupled through the coupling transformer and applied to the bipolar-to-polar (TTL) conversion circuits and to the threshold detector. The threshold detector produces a threshold level that is applied to the control comparator and the conversion circuits. The threshold level is proportional to the amplitude of the applied signals.

(3) When the bipolar signals applied to the threshold detector are interrrupted, the threshold level decreases and causes the control comparator to produce an inhibit signal that disables the conversion circuits. When the bipolar signal input is reestablished and a nominal threshold voltage is obtained, the control comparator inhibit output is removed and the enable output is generated and applied to the conversion circuits.

(4) The bipolar-to-polar (TTL) conversion circuits convert each positive and negative ½-baud bipolar pulse into a ½-baud polar data pulse. The ½-baud polar data pulses are effectively half-width TTL data bits that are applied to the timing recovery circuits and to the digital loop selector. The function of the inhibit signal from the control comparator is to prevent the conversion circuits from processing noise pulses as data pulses when the threshold level decreases to a level that allows noise pulses to be detected. In normal operation, the conversion circuits receive an enable signal from the comparator and an adequate threshold level from the detector that enables the conversion circuits to reject the noise voltage peaks and process only the bipolar data pulses.

(5) The timing recovery circuits produce a 4915.2 kHz timing output based on transitions of the ½-baud polar data. As a result, this recovered timing is synchronized with the ½-baud polar data. In normal operation, the loopback (LOOP—) signal is high and the applied ½-baud polar data and 4915.2 kHz timing are routed through the digital loop selector and applied to the NRZ data flip-flop. When the DIGITAL LOOP BACK switch on the front panel is placed to ON, the resulting low-level LOOP— signal causes the digital loop selector to route the ½-baud polar data and 4915.2 kHz timing to the NRZ-to-bipolar conversion circuits in the driver section.

(6) Each time a ½-baud polar data pulse is applied through the selector to the NRZ data flip-flop, the pulse is clocked into the flip-flop by an associated synchronous 4915.2 kHz timing pulse. By design, the timing pulse occurs several nanoseconds after the data pulse is present at the flip-flop to ensure proper processing of the data pulses. Since the timing pulses occur at the 4915.2 kHz rate, each ½-baud data pulse applied to the flip-flop is stretched to a full-width data pulse (NRZ) that occupies a full bit time. The receive data (RDATA) output from the flip-flop is applied to the phase control circuit and to FS card 21A7. The timing

pulses are also routed to TC (D) card 21A5 and DDOW decoder card 21A8 as the receive master clock (RMASCLK) to time the operation of the demultiplexer section.

(7) The phase control circuit produces the receive phase forcing (RPHF) signal that is applied to the TC (D) card. The RPHF signal is used by the TC (D) card only in 48-channel operation. The RPHF signal controls a divide-by-2 flip-flop on the TC (D) card to ensure that the RCLK produced by the flip-flop occurs slightly after the start of the data pulse.

(8) The TC (D) card applies the receive no clock (RNOCLK) signal to the SG D/R card when the RMASCLK signals are interrupted for a given period of time. The RNOCLK signal causes the diagnostic indicator to light. The RNOCLK signal is removed when the RMSACLK signals are again applied to the TC (D) card.

c. *Driver Section.*

(1) Normally, the nonreturn to zero (NRZOUT) and the transmit master clock (TMASCLK) from MO/C card 21A4 are routed through the digital loop selector as the data and timing to the NRZ-to-bipolar conversion circuits. when the DIGITAL LOOP BACK switch on the front panel is placed to ON, NRZOUT and TMASCLK are routed through the selector and applied as data and timing to the NRZ data flip-flop in the receiver section.

(2) The NRZ-to-bipolar conversion circuits process the NRZ data bits (logic 1's) into bipolar pulses that are applied to the line drivers. The signals from the line drivers are coupled through the output transformer and applied to the CABLE MILES switch in the output line buildout network. When the switch is in the ½ position, the SG output (SGOUT1, SGOUT2) signals are routed directly to the CABLE OUT connector on the rear of the TD-976/G. When the switch is in the ¼ position, the SGOUT1 signal is applied through the quarter-mile attenuation network to the CABLE OUT connector.

(3) The SG interrupter is used only during cable testing operations. When the CABLE TEST switch on the front panel is placed to ON, the cable fault normal (CFNRM—) signal is high and enables gate U27-8. At this time, the 4.69 Hz output from the divide-by-16 counter is passed through U27-8 and applied as an alternating inhibit signal to the NRZ-to-bipolar conversion circuits. Thus, the SG is modulated on and off at a 4.69 Hz rate as required for cable testing.

(4) The traffic monitors monitor the outputs of the line drivers for the presence of traffic (activity). When there is no traffic, the monitors produced the transmit error (XMTERR) signal. In turn, the AD card processes XMTERR, causing the CABLE SIGNAL indicators on the front panel and the RAU to light and the audible ALARM horn on the front panel to produce an alternating on-off beeping sound.

d. *Cable Test Clamp Circuit.* The cable test clamp circuit functions only during cable testing (section XVI). When the CABLE TEST switch on the front panel is placed to OFF, the peak detector (PDET) line is grounded and the clamp circuit is inoperative. When the CABLE TEST switch is placed to ON, the clamp circuit functions to clamp (reference) the base of the cable fault (CABFLT) signal to 0 v.

2-43. Theory of Operation

(fig. FO-10)

a. *General.* This paragraph describes the detailed operation of the circuits on SG D/R card 21A9. The theory of operation is divided into the three functional descriptions established in the block diagram discussion, as listed below.

(1) Receiver section (*b* below).
(2) Driver section (*c* below).
(3) Cable test clamp circuit (*d* below).

NOTE

The sheet number references in *b* through *d* below refer to figure FO-10.

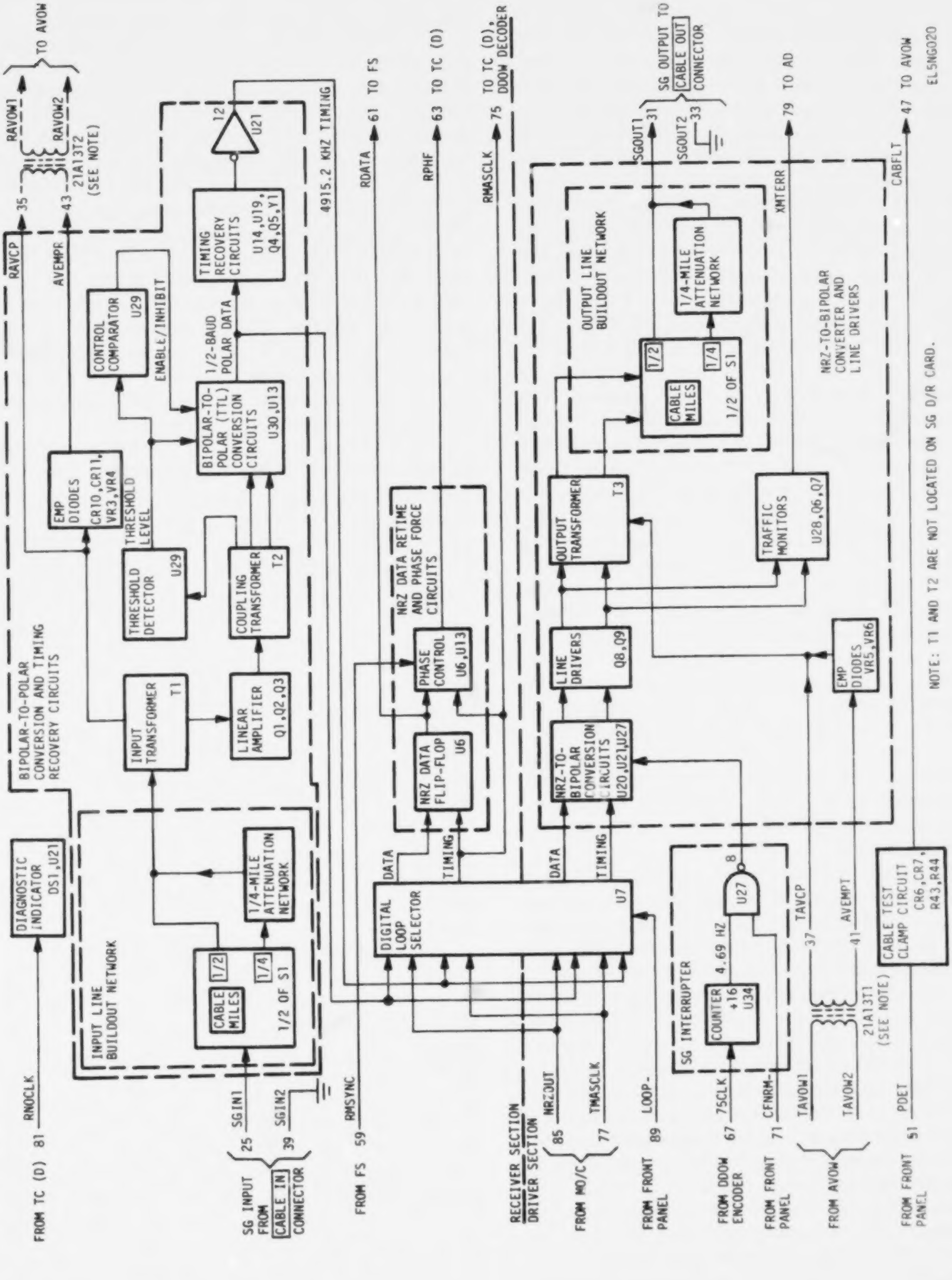
b. *Receiver Section.*

(1) The input line buildout network (sheet 5) consists of one half of CABLE MILES switch S1 and a quarter-mile attenuation network. When switch S1 is placed to the ½ position, the incoming SGIN1 signal is routed through S1 and applied directly (no attenuation) to the input of T1 (sheet 2). When switch S1 is placed to the ¼ position, the incoming SGIN1 signal is applied through S1 and the quarter-mile attenuation network to the input of T1.

(2) Diodes CR1 and CR2 (sheet 2) are part of the EMP circuits on the SG D/R card. The diodes limit any noise voltages developed across the input of T1 to approximately ± 0.7 v. Diodes CR10 and CR11, together with zener diodes VR3 and VR4 (sheet 5), are connected by card pins 35 and 43 across the primary of AVOW transformer 21A12T2 to approximately ± 6 v.

(3) The positive-going and negative-going bipolar (½-baud) pulses are coupled through input transformer T1 (sheet 2) to the base of Q1 in the linear amplifier circuit. Transformer T1 is a pulse transformer that rejects low frequency audio and noise signals and couples the desired 4.9152 kHz bipolar pulses to Q1. The RC components in the secondary of T1 terminate the cable input into the characteristic impedance (approximately 56 ohms) of the cable. The linear amplifier, consisting of amplifiers Q1 and Q2 and emitter-follower Q3, is configured to amplify the bipolar pulses and reject the low frequency components applied to the circuits.

(4) The alternating positive and negative signals developed across the primary of T2 (sheet 2) in the emitter circuit of Q3 are coupled through the dual


FROM TC (D) 81 RNOCLK
DIAGNOSTIC INDICATOR DS1,U21
SG INPUT FROM CABLE IN CONNECTOR
25 SGIN1
39 SGIN2
INPUT LINE BUILDOUT NETWORK
CABLE MILES
1/2
1/4
1/2 OF S1
1/4-MILE ATTENUATION NETWORK
BIPOLAR-TO-POLAR CONVERSION AND TIMING RECOVERY CIRCUITS
INPUT TRANSFORMER T1
LINEAR AMPLIFIER Q1,Q2,Q3
THRESHOLD DETECTOR U29
COUPLING TRANSFORMER T2
THRESHOLD LEVEL
EMP DIODES CR10,CR11, VR3,VR4
CONTROL COMPARATOR U29
ENABLE/INHIBIT
BIPOLAR-TO-POLAR (TTL) CONVERSION CIRCUITS U30,U13
1/2-BAUD POLAR DATA
TIMING RECOVERY CIRCUITS U14,U19, Q4,Q5,Y1
U21
T2
RAVCP
AVEMPR
35
43
RAVOW1
RAVOW2
21A13T2 (SEE NOTE)
TO AVOW
4915.2 KHZ TIMING
FROM FS 59 RMSYNC
RDATA 61 TO FS
RPHF 63 TO TC (D)
RMASCLK 75 TO TC (D), DDOW DECODER
DATA
TIMING
NRZ DATA FLIP-FLOP U6
PHASE CONTROL U6,U13
NRZ DATA RETIME AND PHASE FORCE CIRCUITS
DIGITAL LOOP SELECTOR U7
RECEIVER SECTION
DRIVER SECTION
FROM MO/C
85 NRZOUT
77 TMASCLK
FROM FRONT PANEL 89 LOOP-
FROM DDOW ENCODER 67 75CLK
FROM FRONT PANEL 71 CFNRM-
SG INTERRUPTER
COUNTER ÷16 U34
4.69 HZ
U27
8
FROM AVOW
TAVOW1
TAVOW2
37 TAVCP
41 AVEMPT
21A13T1 (SEE NOTE)
FROM FRONT PANEL 51 PDET
CABLE TEST CLAMP CIRCUIT CR6,CR7, R43,R44
NRZ-TO-BIPOLAR CONVERSION CIRCUITS U20,U21,U27
LINE DRIVERS Q8,Q9
OUTPUT TRANSFORMER T3
OUTPUT LINE BUILDOUT NETWORK
CABLE MILES
1/2
1/4
1/2 OF S1
1/4-MILE ATTENUATION NETWORK
EMP DIODES VR5,VR6
TRAFFIC MONITORS U28,Q6,Q7
NRZ-TO-BIPOLAR CONVERTER AND LINE DRIVERS
SGOUT1 31
SGOUT2 33
SG OUTPUT TO CABLE OUT CONNECTOR
XMTERR 79 TO AD
CABFLT 47 TO AVOW
EL5NG020

NOTE: T1 AND T2 ARE NOT LOCATED ON SG D/R CARD.

Figure 2-20. SG D/R card 21A9, block diagram.

secondary outputs of T2 to pins U30-13, U30-6, and U29-12. Threshold detector U29-1, a peak detector, establishes a voltage level across C30 that is applied as the threshold voltage input through R27 to pins U30-5 and U30-12. Diode CR3 allows only the positive outputs from U29-1 to charge C30. The threshold voltage level developed across C30 is proportional to the amplitude of the output from U29-1. In normal operation, the minimum number of positive bipolar pulses applied to U29-1 is more than adequate to establish and hold C30 charged. When incoming bipolar pulses are interrupted and there are no positive outputs from U29-1, C30 is discharged through R27 and R21. When the voltage across C30 drops to approximately 0.3 v, control comparator U29-8 produces a negative inhibit signal to pins U30-2 and U30-9. The inhibit signal prevents U30-1 and U30-8 from erroneously processing noise signals applied through T2 as data when there is no (or a low-level) threshold voltage applied to pins U30-5 and U30-12. When a threshold voltage is reestablished across C30, the U29-8 output becomes a positive enable signal to pins U30-2 and U30-9. At this time, the threshold voltage level applied to pins U30-5 and U30-12 is sufficient to inhibit any noise components associated with the bipolar pulses being processed through U30-1 and U30-8.

(5) The positive and negative pulse outputs from T2-1 and T2-4 are the same, but 180° out of phase. For example, a positive pulse from T2-1 that is applied to pin U30-13 is a negative pulse from T2-4 to pin U30-6. Each time a positive pulse is applied to the inverting input of U30-1 or U30-8 that exceeds the threshold voltage applied to their noninverting pin inputs, a negative pulse is applied to gate U13-8. The result is that a ½-baud (TTL level) data bit (in RZ format) is produced at U13-8 for each positive or negative bipolar pulse applied through T2 to the bipolar-to-polar conversion circuits.

(6) One-shot multivibrator U14-5 in the timing recovery circuits (sheet 3) is triggered on each time a ½-baud pulse is applied from U13-8. The output from U14-5 is a 100-nanosecond pulse that forces Q4 into conduction. Each time Q4 conducts, crystal Y1 is excited to continue oscillating. Variable capacitor C36 neutralizes the internal capacitance of Y1 and is adjusted to obtain an optimized sine wave output to amplifier Q5. The components in the collector circuit of Q5 form a resonant/phase-shift circuit at 4915.2 kHz. Variable capacitor C39 is adjusted to obtain the proper phase relationship between the data pulses and the timing pulses as they are eventually applied to pins 12, 13, and 14 of NRZ data flip-flop U6-10 (sheet 4). The adjustment is made so that the positive-going transition of the clock pulse applied to U6-12 occurs after the data pulses are applied and present at the J-K inputs (pins 13 and 14) of U6. This adjustment ensures that any system jitter that occurs is within the timing recovery zone to prevent any erroneous clocking of data in the RZ-to-NRZ conversion function.

(7) The 4915.2 kHz pulses from Q5 (sheet 3) are coupled to comparator U19. Comparator U19 performs a squaring function on the applied signals to produce TTL compatible pulses that are applied to inverter U21-12. The output U21-12 is 4915.2 kHz timing pulses that are routed through backplane jumper DRCT02 and applied to digital loop selector U7 (sheet 4). The ½-baud polar data pulses from U13-8 (sheet 2) are routed through backplane jumper DRCT01 and applied to digital loop selector U7. Normally, the ½-baud polar data (DRCT01) and the 4915.2 kHz recovered timing (DRCT02) are selected by U7 for application to NRZ data flip-flop U6-10. However, when the DIGITAL LOOP BACK switch on the front panel is placed to ON, the loopback (LOOP—) signal goes low, causing U7 to select NRZOUT and TMASCLK as the data and timing applied to flip-flop U6-10.

(8) NRZ data flip-flop U6-10 (sheet 4) converts the ½-baud polar data pulses (in RZ format) into NRZ (full-width pulse equal to one bit time) format. The output of U6-10 is the receive data (RDATA) that are routed to FS card 21A7. The data are clocked through U6-10 by the applied 4915.2 kHz timing pulses. To illustrate the RZ-to-NRZ conversion, figure 2-21 shows six RZ data bits (110011) applied to pins U6-13 and U6-14, and the resulting NRZ data output (110011) from U6-10. In 96-channel operation, one bit time of NRZ data is equal to one cycle of the 4915.2 kHz timing. In 48-channel operation, the true data rate is 2457.6 kbps, which is one-half the data rate of 96-channel operation. In 48-channel operation, each bit of data is transmitted twice (in succession) to maintain the 4915.2 kbps cable rate. Therefore, in 48-channel operation, the incoming RZ data bits (110011) at the 4915.2 kbps rate represent (and are converted to) an NRZ output of 101 at the 2457.6 kbps rate. This is shown as the 48-channel equivalent from U6-10 on figure 2-21.

(9) The phase control circuit, consisting of flip-flop U6-7 (sheet 4) and gate U13-6, produces the receive phase forcing (RPHF) signals that are used by the TC (D) card during 48-channel operation. In 48-channel operation, two 4915.2 kHz receive master clocks (RMASCLK's) are applied to the TC (D) card during each data bit time (data at 2457.6 kbps rate). On the TC (D) card, the RMASCLK frequency is divided in half to produce clock signals for processing the data at the 48-channel rate. The RPHF signals applied to the TC (D) card ensure that the divided-down pulses are phased so that positive transitions of the divided-down clock signals occur approximately ¼ bit time after each 48-channel rate RDATA bit is present. The low-level RPHF signal form U13-6 is produced when

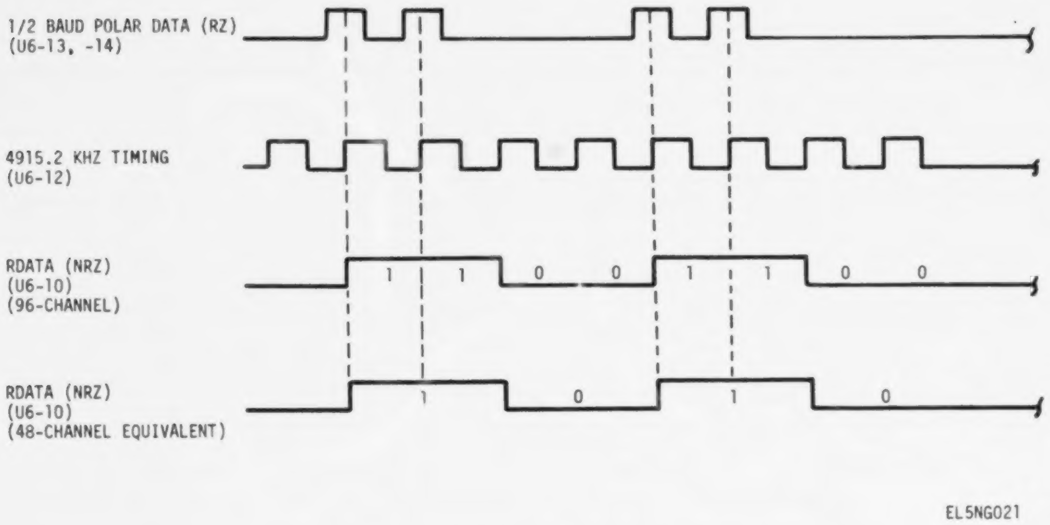


Figure 2-21. RZ-to-NRZ conversion waveform diagram.

major frame synchronization is established (RMSYNC is high), a high output from U6-7 is present, and the RDATA output from U6-10 is high. As shown in figure 2-22, this is a recurring event that takes place at the start of each RDATA bit that transitions from a logic 0 to a logic 1.

(10) Indicator DS1 (sheet 2) is a diagnostic aid. The indicator lights when applied receive no clock (RNOCLK) signal is high. The RNOCLK signal from the TC (D) card will be high when there are no RMASCLK signals produced by the SG D/R card. This condition implies that there is a malfunction on the SG D/R card when RMASCLK signals are not produced and applied to the TC (D) card.

c. *Driver Section.*

(1) In normal operation, the transmit master clock (TMASCLK) and nonreturn to zero output (NRZOUT) signals from the multiplexer section are routed through digital loop selector U7 (sheet 4) to the driver section for processing into the outgoing SG. However, when the DIGITAL LOOP BACK switch on the front panel is placed to ON, the resulting LOOP—signal causes U7 to select the data (DRCTO1) are recovered timing (DRCT02) from the receiver section for application to the driver section for processing into the outgoing SG. Hence, the incoming SG is processed by the receiver section and is then looped by U7 to the driver section for processing into the outgoing SG. Also, the data (NRZOUT) and timing (TMASCLK) from the multiplexer section are looped back by U7 into the demultiplexer section as RDATA and RMASCLK.

(2) The data from pin U7-12 are applied to the J-K inputs of flip-flop U20-6. The 4915.2 kHz timing signals from pin U7-9 are applied to the clock inputs of flip-flops U20-6 and U20-10. The timing output from pin U7-9 is also applied through inverter U21-2 as enable inputs to gates U27-6 and U27-12. Figure 2-23 shows that each time the data bit is a logic 1, either a drive pulse from inverter U21-6 biases on line driver Q9, or a drive pulse from inverter U21-4 biases on driver Q8. The logic configuration of U20-6, U20-10, U27-6, and U27-12 is such that logic 1 pulses are alternately applied to either U21-4 or U21-6 as shown in figure 2-23. Therefore, Q9 and Q8 are alternately pulsed on to produce the bipolar pulse inputs to the primary of T3.

(3) The bipolar pulses coupled through T3 (sheet 4) are applied to the output line buildout network (sheet 5). The network is basically the same as the input line buildout network (*b*(1) above). Zener diodes VR5 and VR6, together with CR12 through CR15, make up the EMP circuits in the driver section. Diodes CR12 through CR15 limit the voltage across the secondary of T3 to approximately ± 1.5 v. Zener diodes VR5 and VR6 limit the voltage across the secondary of AVOW transformer 21A12T1 in the card file to approximately ± 6 v.

(4) One-shots U28-12 and U28-13, together with transistors Q6 and Q7, form a circuit to monitor outgoing traffic (sheet 4). In normal operation, line drivers Q8 and Q9 alternately bias Q6 and Q7 on and off. When Q9 conducts, Q6 is biased off and the input to pin U28-10 goes low. When Q9 turns off, Q6 conducts and produces a high (trigger) to pin U28-10 to keep the stage retriggered. The next bipolar pulse performs the same function with Q8 and Q7. The output from Q7 is applied to pin U28-2, keeping U28-13 retriggered. In normal operation bipolar pulses occur fre-

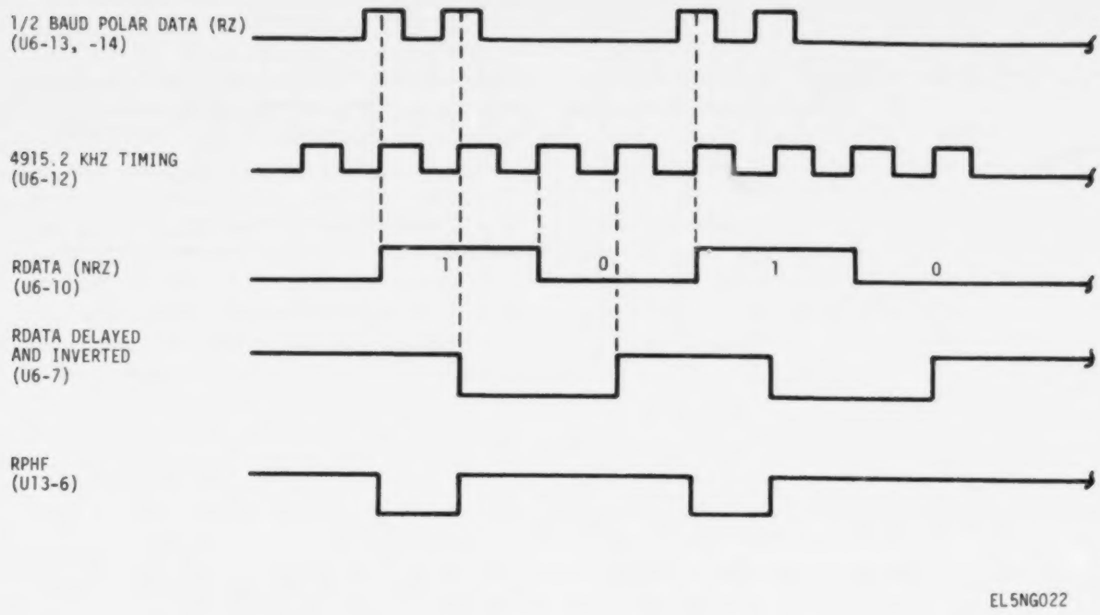


Figure 2-22. Phase control circuit RPHF waveform diagram.

quently enough to keep both U28-12 and U28-13 retriggered. Both U28-12 and U28-13 have an average duty cycle of 340 microseconds. When the data pulses to either U28-12 or U28-13 are interrupted for a period longer than 340 microseconds, the XMTERR signal from U28-12 goes high, causing the CABLE SIGNAL indicators on the front panel and the RAU to light and the audible ALARM horn on the front panel to produce an alternating on-off beeping sound.

d. Cable Test Clamp Circuit (sheet 4). Diodes CR6 and CR7, together with resistors R43 and R44, form the cable test clamp circuit. This circuit functions only during cable testing to clamp (reference) the peak detector (PDET) line to 0 v. CR7 is forward biased and develops approximately ±0.7 v at its anode, which is also connected to the anode of CR6. Therefore, whenever the PDET line attempts to go more negative than 0 v, CR6 is forward biased and clamps the PDET line to 0 v. R43 is part of a voltage divider that also includes resistors on AVOW card 21A10. Refer to section XVI for a discussion relating to cable testing. Whenever cable testing is not being performed, the PDET line is grounded by the CABLE TEST switch on the font panel.

Section XII. FRAME SYNC (FS) CARD 21A7

2-44. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the FS card . There is one FS card (21A7) in the TD-976/G. The circuits on the FS card continually look for and decode frame/major frame sync patterns to control and synchronize demultiplexer section operation. The FS card also decodes and produces receive delete signals to accomplish destuff actions in the demultiplexer section based on stuff codes transmitted by a far-end multiplexer. The block diagram discussion in paragraph 2-45 is based on the block diagram in figure 2-24. The detailed theory of operation in paragraph 2-46 is based on the FS card schematic diagram in figure FO-11.

2-45. Block Diagram Discussion

(fig. FO-9)

a. General. The block diagram discussion is divided into three functional circuit descriptions as follows:

(1) The frame sync detection circuits (*b* below) look for the 8-bit frame/major frame sync pattern contained within the 11-bit frame synchronization and stuff pattern in the O/H bits that are interwoven into each frame of the incoming SG data stream.

(2) The frame sync maintenance circuits (*c* below)

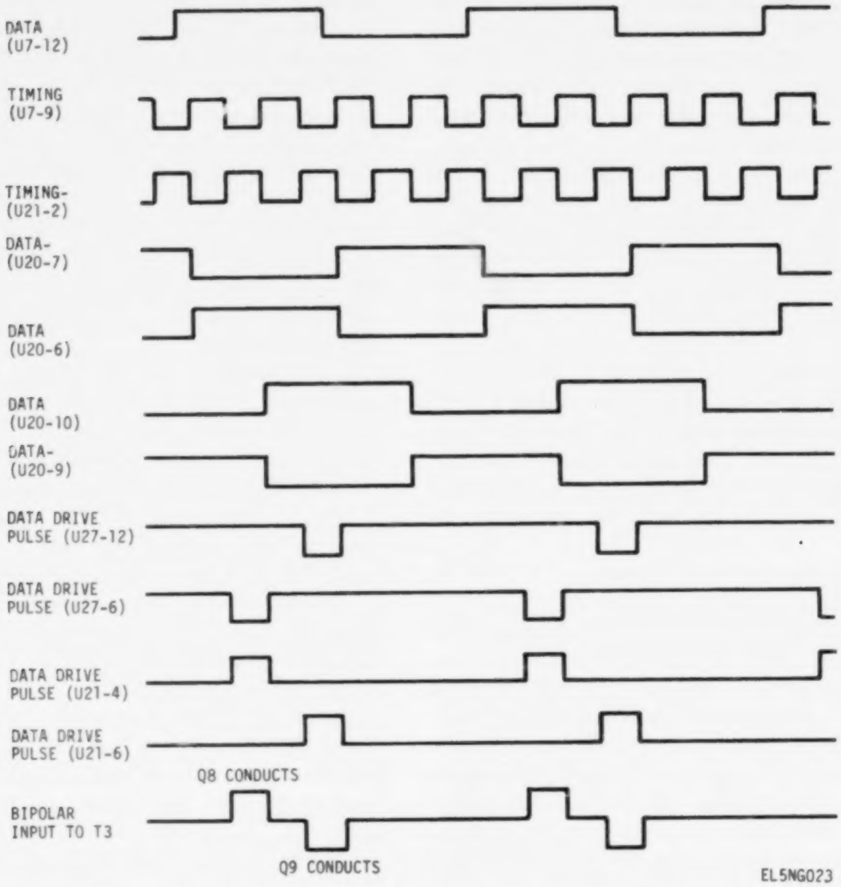

DATA (U7-12)
TIMING (U7-9)
TIMING- (U21-2)
DATA- (U20-7)
DATA (U20-6)
DATA (U20-10)
DATA- (U20-9)
DATA DRIVE PULSE (U27-12)
DATA DRIVE PULSE (U27-6)
DATA DRIVE PULSE (U21-4)
DATA DRIVE PULSE (U21-6)
Q8 CONDUCTS
BIPOLAR INPUT TO T3
Q9 CONDUCTS
EL5NG023

Figure 2-23. NRZ-to-bipolar conversion waveform diagram.

create frame and major frame sync confidence signals that time the initiation of demultiplexing operations.

(3) The destuff detections circuits (*d* below) monitor for the presence of a stuff code transmitted by a far-end multiplexer.

b. Frame Sync Detection Circuits.

(1) The frame sync detection circuits continually monitor the incoming receive data (RDATA) for the presence of a frame/major frame sync pattern contained within the RDATA. When a frame/major frame sync pattern is decoded, the circuits produce the applicable major frame sync decode and/or frame sync decode signal for application to the frame sync maintenance circuits.

(2) The RDATA are continually clocked through the 189-bit serial shift register by the receive clocks (RCLK--). As previously described in the overall block diagram discussion (section IV) and shown in figures 2-3 and 2-4, the frame/major frame sync pattern is contained in bits locations B3 through B10 (or A3 through A10) of the 11-bit frame synchronization and stuff pattern. These O/H bits are located starting at bit 153 (O/H bit of minor frame 8) and ending at bit 340 (O/H bit of minor frame 19) of each frame. There are 16 tape pickoffs from the shift register that are used by the frame sync pattern decoders.

(3) The 16 tap pickoffs represent a logic 1 and a logic 0 output for each of the eight O/H bit locations being monitored. Eight of the tap pickoffs are selected and connected to each of the four frame sync pattern decoders. Thus, each pattern decoder is constantly taking a broadside look at eight pickoff points of the shift register. The eight tap pickoffs applied to each of the pattern decoders are representative of one of the four

possible patterns contained in a frame. The patterns will be in one of four forms: B, B—, A, or A—. The A-pattern appears in the last frame of each major frame and indicates no stuff code transmitted (the A pattern indicates that a stuff code was transmitted). The B—pattern appears in all other frames and indicates no stuff code transmitted (the B pattern indicates that a stuff code was transmitted).

(4) At the time that a frame is positioned in the shift register so that the bits applied through the selected tap pickoffs represent a frame/major frame sync pattern, one of the four pattern decoders will decode the appropriate pattern. The frame sync decode output is produced whenever a B, B—, A, or A— pattern is decoded.

(5) The shift register is configured so that the last bit of a frame (bit 341) is applied through gate U23-6 as SDATA during the bit time that a frame sync pattern decode is performed. This configuration establishes the relationship that allows the demultiplexer section timing to be synchronized with the incoming data frames.

c. *Frame Sync Maintenance Circuits.*

(1) The frame sync maintenance circuits contain a frame sync confidence counter and a major frame sync confidence counter (both counters are up/down counters). The two confidence counters perform a confidence function by permitting the demultiplexer timing and O/H functions to continue operating when there is an occasional loss of a frame/major frame sync decode during a frame. The counters also cause demultiplexing timing and demultiplexing operations to be inhibited when frame synchronization is lost. The frame sync and major frame confidence counters are configured to count down to a minimum count of 0 (0000) (maximum confidence) or to count up to a maximum count of 15 (1111) (no conficence). The counters are not allowed to cycle past their maximum and minimum counts. Application of the RNOCLK— signal presets both counters to a maximum count (no confidence) condition. RNOCLK— is active whenever SG D/R card 21A9 is not producing a receive master clock (RMASCLK).

(2) When the frame sync confidence counter contains a maximum count of 15 (1111), a no-confidence condition exists and the receive frame sync (RFSYNC—) signal is low, inhibiting operation of the bit counter and minor frame counter on TC (D) card 21A5. The RFSYNC— signal also causes the major frame sync confidence counter to be preset to a count of 15 (no confidence). When the frame sync detection circuits recognize a frame sync pattern, they produce a frame sync decode (occurring during the time that bit 341 is at the output of gate U23-6). This allows the next RCLK to decrement the frame sync confidence counter one count (count of 14), causing RFSYNC— to go high (occurring during the time that bit 1 of the next frame is at the output of gate U23-6). RFSYNC— going high releases the bit counter and minor frame counter on TC (D) card 21A5 to operate (bit counter was held preset at a bit 1 count). This action is timed so that as the next RCLK clocks the bit counter to a bit 2 count, bit 2 is on the SDATA line. Once frame sync confidence is established by a count of 14 or less, each coincidence of an RCLK and R341BT— causes the frame sync counter to either decrement or increment one count. If a frame sync decode is present, the counter will decrement one count; otherwise, it will increment one count. The counter may be decremented to a minimum count of 0 (0000), which represents maximum confidence.

(3) Operation of the major frame confidence counter is similar to the operation of the frame sync confidence counter just described. A maximum count of 15 represents a no-confidence condition, with RMSYNC and SYNC 8 being high and RMSYNC— and SYNC 8— being low. RMSYNC enables the phase control circuit on SG D/R card 21A9 (section XI). RMSYNC— inhibits the frame counter on TC (D) card 21A5 and causes the phase-locked loops on the DGP cards to track an internally generated 576 kHz clock. When the frame sync detection circuits recognize a major frame sync pattern (A or A— pattern), they produce a major frame sync decode that directs the major frame sync confidence counter to count down. R341BT enables the counter so that it may be clocked by RCLK and decrement one count (count of 14), causing RMSYNC to go low and RMSYNC— to go high. RMSNYC— going high releases the frame counter on TC (D) card 21A5 to operate and allows the phase-locked loops on the DGP cards to operate normally and track extracted write clocks. RMSYNC going low inhibits operation of the phase control circuit on SG D/R card 21A9. Once major frame sync confidence is established by a count of 14 or less, the counter is enabled by RLBMF— and clocked by RCLK to either decrement or increment one count. If a major frame sync decode is present, the counter will decrement one count; otherwise, it will increment one count. When the counter has decremented to a count of 7, SYNC 8 goes low and SYNC 8— goes high. SYNC 8— going high releases the 3-bit shift register in the decoder section of DVOW card 21A11 to operate and also releases the read and write address counters on DDOW decoder card 21A8. SYNC 8 going low has not effect. The counter may be decremented to a minimum count of 0, which represents maximum confidence. If the counter increments to a count of 8 or more (indicating a decline in confidence), SYNC 8 goes high, activating various alarms as decribed in paragraph 2-15*f*(5).

d. *Destuff Detection Circuits.*

(1) The destuff detection circuits monitor the in-

coming SG data (SDATA) and its complement (SDATA—) to determine if a stuff code action was transmitted by the far-end multiplexer. When a stuff code is detected, the low-level receive delete (RDLTTY) signal is produced and applied to the TC (D) and DDOW decoder cards to initiate a destuff action in the demultiplexer section.

(2) The comparator continually compares the locally generated receive stuff code (RSCODE) with the SDATA— line and the RSCODE— with the SDATA line. When RSCODE is the same as SDATA— or RSCODE— is the same as SDATA, the output from the comparator is low and inhibits the comparator counter. When RSCODE is different from SDATA— and RSCODE— is different from SDATA, the output from the comparator is high and provides and enabling input to the comparator counter. Even though the comparator is continually making comparisons, only those comparisons made during the 11-bit times containing the frame synchronization and stuff pattern are recognized by the comparator counter.

(3) At the end of minor frame 2 of each frame, the comparator counter is preset to zero by the receive stuff request strobe (RSREST—). The receive frame code enable time (RFCET) signal is applied to the counter during the 11-bit times when the frame synchronization and stuff pattern is present on the SDATA and SDATA— lines. If the output of the comparator is high when RFCET is applied, the comparator counter will be incremented one count when clocked by RCLK.

(4) When the comparator counter contains a count of 6 or more, it produced the low-level receive delete (RDLTTY) signal. The signal is applied to the destuff request activity monitor and is routed to the TC (D) and DDOW decoder cards to initiate a destuff action.

(5) The destuff request activity monitor produces a continuous low-level receive diagnostic enable priority 4 (RDEP4) signal during normal operation. When no RDLTTY signals are produced over a given period of time (error condition), the RDEP4 signal goes high. When RDEP 4 goes hgih, the TC (D) card, in turn, produces a low-level receive diagnostic alarm priority (RDAP24—) signal that is applied back to the FS card and causes diagnostic indicator DS1 to light. Additional alarm indicators are also activated as described in paragarph 2-15*f*(4).

2-46. Theory of Operation

(fig. FO-11)

a. General. This paragraph describes the detailed operation of the circuits on FS card 21A7. The theory of operation is divided into the three functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Frame sync detection circuits (*b* below).

(2) Frame sync maintenance circuits (*c* below).

(3) Destuff detection circuits (*d* below).

NOTE

The sheet number references in *b* through *d* below refer to figure FO-11.

b. Frame Sync Detection Circuits.

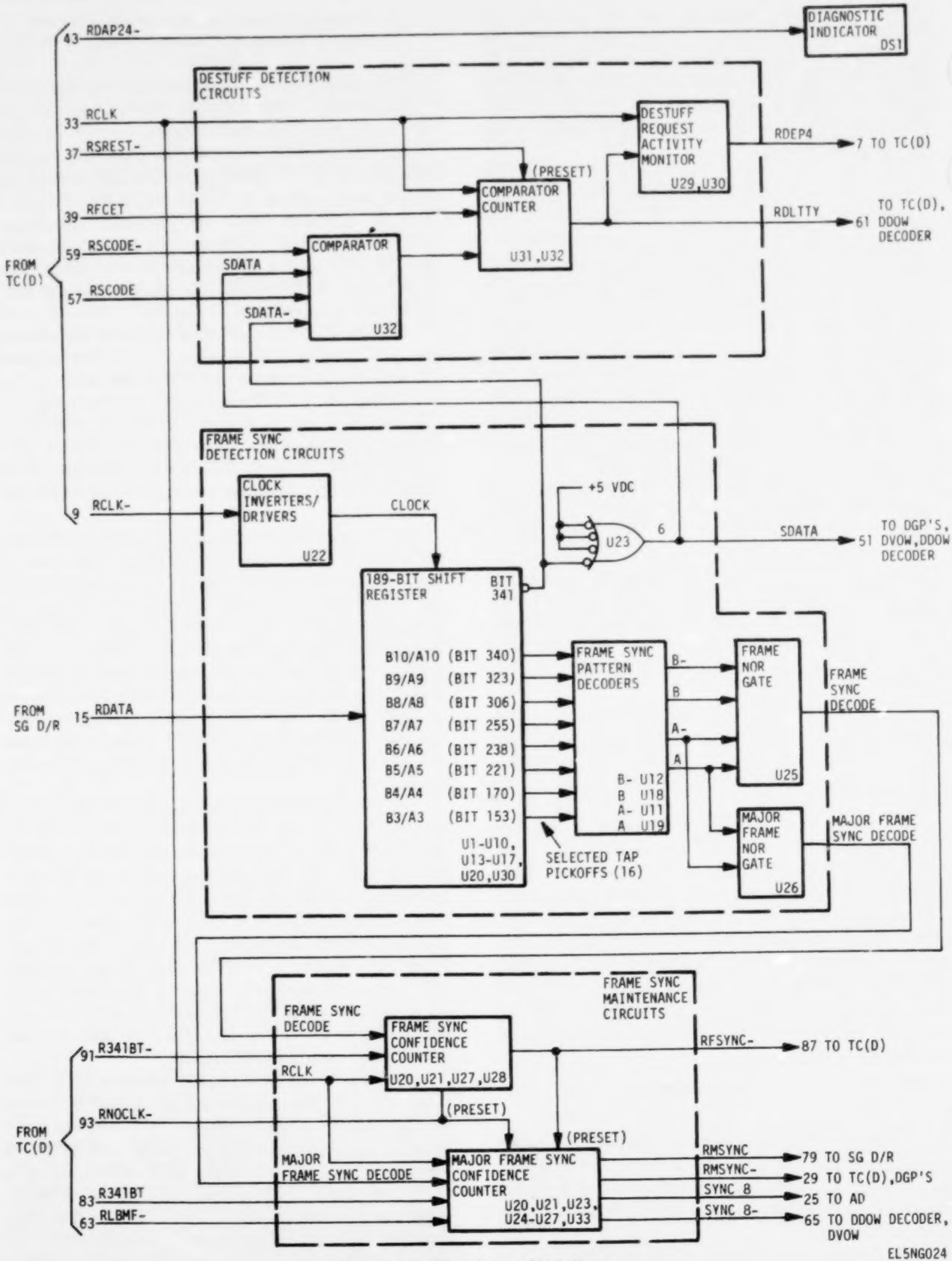
(1) The incoming receive data (RDATA), applied through card pin 15 (sheet 2), are clocked through the 189-bit shift register by the receive clocks (RCLK—) from TC (D) card 21A5. In 96-channel operation, RCLK— is at a 4915.2 kHz rate. In 48-channel operation, RCLK— is at a 2457.6 kHz rate. RCLK— is inverted by gates U22-6 and U22-8 and simultaneously clocks each stage of the shift register.

(2) The RDATA applied to the card are clocked into J-K flip-flop U30-6 (sheet 2), the first stage of the shift register, whose pin U30-6 output is applied to flip-flop U4-6, the second stage of the shift register. The output at pin U30-7 is the SDATA— which is applied to comparator U32-8 (*d* below). Gate U23-6 inverts SDATA— to SDATA for outputting to other cards of the demultiplexer section, as well as to comparator U32-8.

(3) A simplified diagram of the 189-bit shift register is shown in figure 2-25. The figure identifies the components that make up the shift register and shows the 16 tap pickoffs of the shift register. The 16 tap pickoffs represent a logic 1 and a logic 0 output for each of the eight O/H bit locations being monitored. Eight of the tap pickoffs are selected and connected to each of the four pattern decoders shown at the bottom of figure 2-25. The components of the 189-bit shift register are shown on sheets 2, 3, and 4 of figure FO-11, and the pattern decode gates are shown on sheet 6.

(4) The eight tap pickoffs applied to each of the pattern decoders (fig. 2-25) are representative of one of the four possible sync patterns contained in a frame (B—, B, A—, or A). Each pattern is shown to the left of its pattern decode gate (A3 or B3 on top). At the time that a frame is positioned in the shift register so that the bits from the tap pickoffs represent a frame/major frame sync pattern, one of the four pattern decoders will decode the appropriate pattern. The decode action (output of one of four pattern decoders going low) lasts for one bit time. At the time that a decode action occurs, bit 341 is on the SDATA line.

(5) Each of the four pattern decoders (U12, U18, U11, and U19) is an eight-input gate (sheet 6). U12-8 decodes the B— pattern, while U18-8 decodes the B pattern. U11-8 decodes the A— pattern, while U19-8 decodes the A pattern. The B— or B pattern occurs in all frames except the last frame of each major frame, when the A— or A pattern occurs. The B or A pattern indicates that a stuff action was transmitted by the far-end multiplexer. Similarly, a B— or A— pattern


43 RDAP24-
DIAGNOSTIC INDICATOR DS1
DESTUFF DETECTION CIRCUITS
33 RCLK
37 RSREST-
DESTUFF REQUEST ACTIVITY MONITOR U29,U30
RDEP4
7 TO TC(D)
(PRESET)
COMPARATOR COUNTER U31,U32
39 RFCET
RDLTTY
61 TO TC(D), DDOW DECODER
59 RSCODE-
COMPARATOR U32
SDATA
FROM TC(D)
57 RSCODE
SDATA-
FRAME SYNC DETECTION CIRCUITS
+5 VDC
9 RCLK-
CLOCK INVERTERS/ DRIVERS U22
CLOCK
U23
6
SDATA
51 TO DGP'S, DVOW,DDOW DECODER
189-BIT SHIFT REGISTER
BIT 341
B10/A10 (BIT 340)
B9/A9 (BIT 323)
B8/A8 (BIT 306)
B7/A7 (BIT 255)
B6/A6 (BIT 238)
B5/A5 (BIT 221)
B4/A4 (BIT 170)
B3/A3 (BIT 153)
U1-U10, U13-U17, U20,U30
FRAME SYNC PATTERN DECODERS
B- U12
B U18
A- U11
A U19
B-
B
A-
A
FRAME NOR GATE U25
FRAME SYNC DECODE
MAJOR FRAME NOR GATE U26
MAJOR FRAME SYNC DECODE
FROM SG D/R
15 RDATA
SELECTED TAP PICKOFFS (16)
FRAME SYNC MAINTENANCE CIRCUITS
FRAME SYNC DECODE
FRAME SYNC CONFIDENCE COUNTER U20,U21,U27,U28
91 R341BT-
RCLK
RFSYNC-
87 TO TC(D)
93 RNOCLK-
(PRESET)
(PRESET)
FROM TC(D)
MAJOR FRAME SYNC DECODE
MAJOR FRAME SYNC CONFIDENCE COUNTER U20,U21,U23, U24-U27,U33
83 R341BT
63 RLBMF-
RMSYNC
79 TO SG D/R
RMSYNC-
29 TO TC(D),DGP'S
SYNC 8
25 TO AD
SYNC 8-
65 TO DDOW DECODER, DVOW

EL5NG024

Figure 2-24. FS card 21A7, block diagram.

indicates that no stuff action was transmitted.

(6) When a B—, B, A—, or A pattern is decoded, the resulting high-level output from U25-8 (sheet 6), representing a frame sync decode, is routed through backplane jumper FSCT01 as a down signal to frame sync confidence counter U28 (sheet 5). In turn, when an A— or A pattern is decoded, the resulting high-level output from U26-12 (sheet 6), representing a major frame sync decode, is routed through backplane jumper FSCT02 as a down signal to major frame sync confidence counter U24.

c. *Frame Sync Maintenance Circuits.*

(1) Frame sync confidence counter U28 (sheet 5) can be decremented to a minimum count of 0 (0000) represents maximum confidence) or it can be incremented to a maximum count of 15 (1111) (represents no confidence). The maximum/minimum output from pin U28-12 initiates a count inhibit function when counter U28 attempts to cycle past a maximum or minimum count. The maximum/minimum output goes high, holding U21-8 low, which causes U20-8 to apply a high inhibit to enable input pin U28-4. This configuration permits the counter to count between 1111 and 0000 as described in the following discussion.

(2) When counter U28 contains a maximum count of 15 (1111), a no-confidence condition exists and the RFSYNC— output from gate U27-8 is low. The low output from U27-8 inhibits operation of the bit counter and minor frame counter on TC (D) card 21A5 and is applied through inverter U20-12 (sheet 6), gate U26-8, and flip-flop U33-6 to preset major frame sync confidence counter U24 to a maximum count (no confidence). Also, the low output of U27-8 (sheet 5) is applied as an enable input to pin U21-10. The counter remains in this state until a frame sync decode occurs (*b*(6) above). Application of a low-level RNOCLK— signal presets U28 to a maximum count (no-confidence condition).

(3) When a frame sync decode occurs, the high-level input to pin U28-5 (sheet 5) (FSCT01) directs U28 to count down. At this time, the maximum/minimum output from pin U28-12 is low, causing U20-8 to be low, which enables counter U28. This allows the next RCLK to decrement U28 one count to a count of 14 (1110), causing the RFSYNC— output of U27-8 to go high. RFSYNC— going high releases the bit counter and minor frame counter on TC (D) card 21A5 to operate and also releases major frame sync confidence counter U24 (sheet 6) to operate.

(4) Once frame sync confidence is established by a count of 14 or less, each R341BT— applied through U21-8 and U20-8 (sheet 5) enables counter U28 to be clocked by RCLK. U28 will decrement one count if a frame sync decode exists (input to pin U28-5 high) or will increment one count if no frame sync decode is present.

(5) Operation of major frame sync confidence counter U24 (sheet 6) is similar to the operation of frame sync confidence counter U28 ((1) through (4) above). When U24 contains a maximum count of 15 (1111), a no-confidence condition exists, with RMSYNC and SYNC 8 being high and RMSYNC— and SYNC 8— being low. U24 will be preset to a maximum count (no confidence) by the action of U20-12, U26-8, and U33-6 when frame sync confidence is not established (input to pin U20-13 low). Additionally, U24 will be preset to a maximum count if the RNOCLK— input to pin U33-1 is low. RMSYNC enables the phase control circuit on SG D/R card 21A9. RMSYNC— inhibits the frame counter on TC (D) card 21A5 and causes the phase-locked loops on the DGP cards to track an internally generated 576 kHz clock.

(6) When a major frame sync decode occurs, the resulting high-level input to pin U24-5 (sheet 6) (FSCT02) directs U24 to count down. At this time, the maximum/minimum output from U24-12 is low and enables one-half of U21-6. The high-level RMSYNC signal enables one input of gate U27-6, while the other input of U27-6 is enabled by R341BT. The resulting low-level output of U27-6 completes enabling of U21-6, causing a low-level enable input to pin U24-4. This allows the next RCLK to decrement U24 one count to a count of 14 (1110), causing RMSYNC to go low and RMSYNC— to go high. RMSYNC— going high releases the frame counter on TC (D) card 21A5 to operate and allows the phase-locked loops on the DGP cards to operate normally and track extracted write clocks. RMSYNC going low inhibits operation of the phase control circuit on SG D/R card 21A9 and also inhibits gate U27-6. Enabling of U24 will now be controlled by the receive last bit of major frame (RLBMF—) signal.

(7) Once major frame sync confidence is established by a count of 14 or less, each RLBMF— applied through U21-6 and U20-10 enables counter U24 to be clocked by RCLK. U24 will decrement one count if a major frame sync decode exists (input to pin U24-5 high) or will increment one count if no major frame sync decode is present. When U24 has decremented to a count of 7, the SYNC 8 output goes low and the SYNC 8— output from U26-6 goes high. SYNC 8— going high releases the 3-bit shift register in the decoder section of DVOW card 21A11 to operate and also releases the read and write address counters on DDOW decoder card 21A8. The counter may be decremented to a minimum count of 0, which represents maximum confidence. If U24 increments to a count of 8 or more (indicating a decline in confidence), SYNC 8 goes high, activating various alarms as described in paragraph 2-15*f*(5).

d. *Destuff Detection Circuits.*

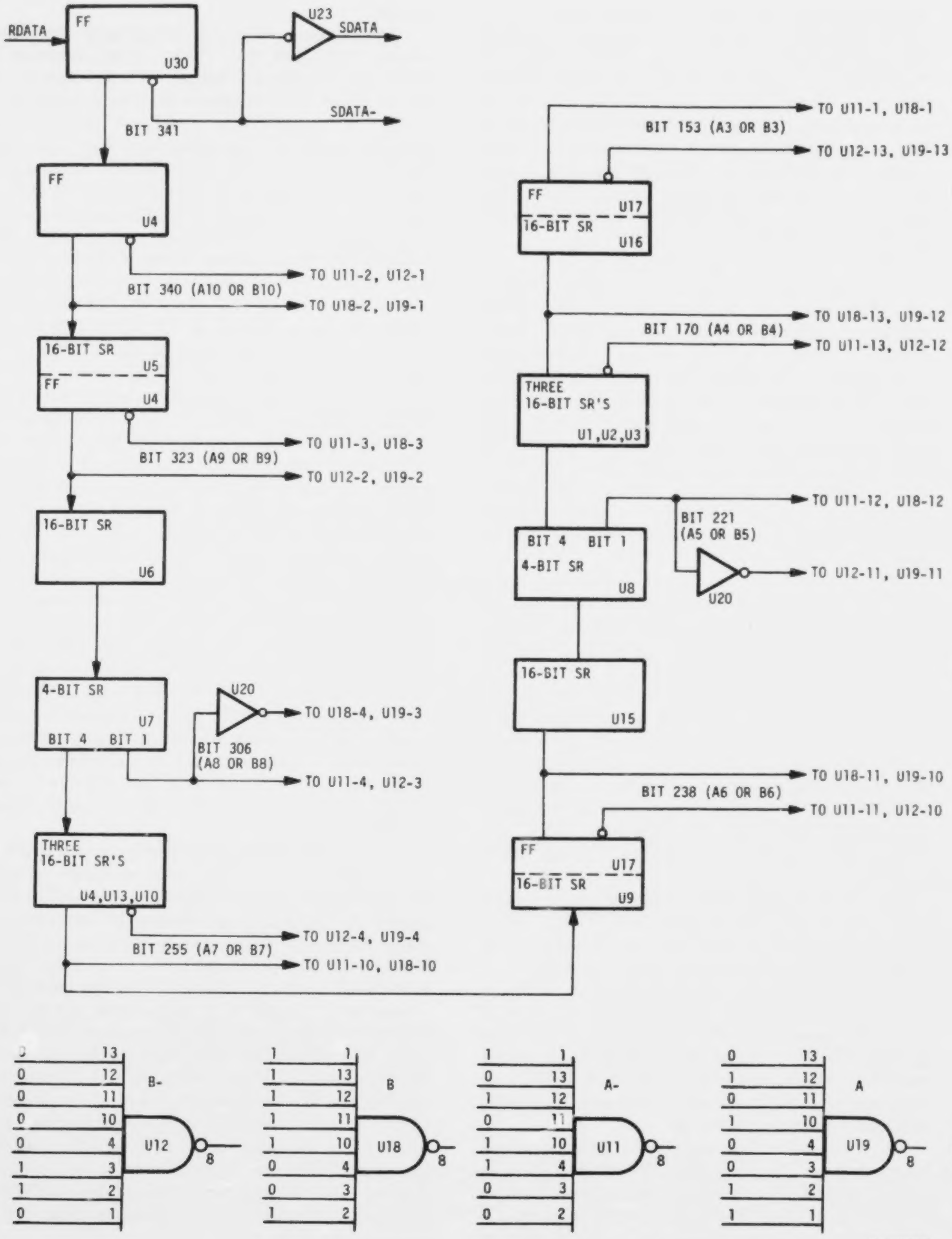

RDATA
FF
U30
U23
SDATA
SDATA-
BIT 341
FF
U4
TO U11-2, U12-1
BIT 340 (A10 OR B10)
TO U18-2, U19-1
16-BIT SR
U5
FF
U4
TO U11-3, U18-3
BIT 323 (A9 OR B9)
TO U12-2, U19-2
16-BIT SR
U6
4-BIT SR
U7
BIT 4
BIT 1
U20
TO U18-4, U19-3
BIT 306
(A8 OR B8)
TO U11-4, U12-3
THREE
16-BIT SR'S
U4,U13,U10
TO U12-4, U19-4
BIT 255 (A7 OR B7)
TO U11-10, U18-10
TO U11-1, U18-1
BIT 153 (A3 OR B3)
TO U12-13, U19-13
FF
U17
16-BIT SR
U16
TO U18-13, U19-12
BIT 170 (A4 OR B4)
TO U11-13, U12-12
THREE
16-BIT SR'S
U1,U2,U3
TO U11-12, U18-12
BIT 221
(A5 OR B5)
BIT 4
BIT 1
4-BIT SR
U8
U20
TO U12-11, U19-11
16-BIT SR
U15
TO U18-11, U19-10
BIT 238 (A6 OR B6)
TO U11-11, U12-10
FF
U17
16-BIT SR
U9
B-
U12
0 13
0 12
0 11
0 10
0 4
1 3
1 2
0 1
8
B
U18
1 1
1 13
1 12
1 11
1 10
0 4
0 3
1 2
8
A-
U11
1 1
0 13
1 12
0 11
1 10
1 4
0 3
0 2
8
A
U19
0 13
1 12
0 11
1 10
0 4
0 3
1 2
1 1
8
EL5NG025

Figure 2-25. 189-bit shift register and pattern decode gates, simplified diagram.

(1) Comparator U32-8 (sheet 4) performs two parallel compare functions. The locally generated RSCODE is compared with the SDATA— line (pin U32-10) and the RSCODE— is compared with the SDATA line (pin U32-1). When RSCODE is the same as SDATA— or RSCODE- is the same as SDATA, the output of U32-8 is low. Conversely, when RSCODE is different from SDATA— and RSCODE— is different from SDATA, the output of U32-8 is high. The output of U32-8 is routed through backplane jumper FSCT03 as an enable/inhibit input to comparator counter U31 (sheet 5). Even though U32-8 is continually making comparisons, only those comparisons made during the 11-bit times containing the frame synchronization and stuff pattern are recognized by U31.

(2) Comparator counter U31 is preset to a count of 0 at the end of minor frame 2 of each frame by RSREST—. RFCET is applied as an enable input to pin 10 of U31 during the 11 bit times when the frame synchronization and stuff pattern is present on the SDATA and SDATA— lines. If the output of comparator U32-8 (FSCT03) is high when RFCET is applied, U31 will be incremented one count when clocked by RCLK. When U31 reaches a count of 6 (0110), the RDLTTY output from U32-6 goes low (indicates recognitin of a stuff code in the received SG), causing a destuff action to be initiated by the demultiplexer section.

(3) The destuff request activity monitor (sheet 5) consists of J-K flip-flop U30-10 and one-shot U29-13. The output of the flip-flop is clocked low by RCLK when RDLTTY is low. When counter U31 is preset and the output of U32-6 goes high, the next RCLK clocks U30-10 high. The positive transition from U30-10 triggers U29-13. In normal operation, the duty cycle of U29-13 is sufficient to last until it is retriggered. If the duty cycle of U29-13 expires before it is retriggered, the high-level RDEP4 signal is produced and applied to TC (D) card 21A5. In turn, the TC (D) card produces the low-level RDAP24— signal that causes indicator DS1 (sheet 1) to light. Refer to paragraph 2-15*f*(4) for an overall discussion relating to the destuff activity monitor.

Section XIII. GROUP TRAFFIC MONITOR (GTM) CARD 21A2

2-47. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the GTM card. There is one GTM card (21A2) in the TD-976/G. The card converts the eight PCM group inputs to TTL levels, sequentially examines the eight input group data lines for traffic and the eight output group data lines for traffic and a dummy pattern, and generates a repetitive 7-bit activity pattern. The block diagram discussion in paragraph 2-48 is based on the block diagram in figure 2-26. The detailed theory of operation in paragraph 2-49 is based on the GTM card schematic diagram in figure FO-12.

2-48. Block Diagram Discussion

(fig. 2-26)

a. General. The block diagram discussion is divided into seven functional circuit descriptions as follows:

(1) The line receivers (*b* below), of which there are eight, convert the incoming PCM group inputs to TTL levels and generate a reset strobe each time there is a data transition from a logic 0 to a logic 1.

(2) The scan interval generator (*c* below) controls the length of time each input group or output group data line is examined, controls advancing of the address counter, and controls reading out the status of the group data traffic monitor and the dummy pattern detector and counter.

(3) The address counter (*d* below) controls the group data and timing selectors and provides group frame scan address bit outputs to AD card 21A1.

(4) The group data and timing selectors (*e* below), in response to outputs of the address counter, select the input group or output group line to be examined.

(5) The group data traffic monitor (*f* below) monitors the selected input group or output group data line for the presence of traffic (activity).

(6) The dummy pattern detector and counter (*g* below) searches the output group data line connected to it for the presence of a dummy pattern.

(7) The activity pattern generator (*h* below) generates two repetitive 7-bit activity patterns.

b. Line Receivers. Each of the eight line receivers converts an incoming PCM group input (NRZ format, where a logic 1 is approximately 0 v and a logic 0 is approximately −2 v to TTL levels (NRZ format, where a logic 1 is approximately +5 v and a logic 0 is approximately 0 v). The respective input group data (IGRP1D through IGRP8D) outputs of the line receivers are routed to the appropriate DGP card and to the input group data selector (*e* below). Each positive transition out of a line receiver (data transition from a logic 0 to a logic 1) triggers an associated timing extractor one-shot to produce a nominal 100-nanosecond negative reset strobe (RST—). The RST1— through RST8— outputs are routed to the appropriate DGP card, where they control creation of extracted 576 kHz timing for each group data input.

c. Scan Interval Generator. The scan interval generator determines the scan interval (amount of time) during which the data lines for a given group will be connected to the group data traffic monitor. Additionally, for output groups, the scan interval generator determines the time that the data and timing lines for a given group will be connected to the dummy pattern detector and counter.

(1) The group scan generator has an approximate 9.7-millisecond duty cycle during which time the selected input or output group data line will be examined. When the group scan generator times out, it triggers the group frame monitor strobe one-shot to produce both positive and negative pulses of approximately 2 microseconds duration. The second positive transition of the 576 KHZ 1 signal after time-out of the group scan generator triggers it into a new duty cycle (scan interval).

(2) The group frame monitor strobe (GFMST) (2-microsecond positive pulse) allows AD card 21A1 to read and store the status of the good status (GS) and dummy sync (DS) lines. The trailing edge of the 2-microsecond positive pulse triggers reset one-shot U1. The trailing edge of the 2-microsecond negative pulse (negative-to-positive transition) clocks the address counter, causing it to increment one count.

(3) Reset one-shot U1, when triggered on, produces an approximate 2.7-microsecond negative pulse that resets the dummy pattern confidence counter to zero and clears the dummy pattern detector.

d. Address Counter. The address counter is advanced one count at the start of each scan interval. It advances 16 counts (eight input groups and eight output groups) and then repeats the cycle. Its group frame scan address bit outputs (GF1, 2, 4, 8 and 8—0 cause the group data and timing selectors to select the next sequential group and are also routed to AD card 21A1, informing that card which group is being processed by the GTM card. During equipment power turn-on, the power on reset (PRS—) negative pulse resets the address counter to zero. At the end of the 16-count cycle, the group frame monitor terminal count (GFMTC—) output is produced, which resets the alarm clear circuits on AD card 21A1.

e. Group Data and Timing Selectors. The group data and timing selectors, in response to address counter outputs, sequentially select the eight input groups and eight output groups.

(1) Input group data selector U23 sequentially selects and inverts the eight input group data lines (counts 1 through 8 of address counter) for application to the group data traffic monitor.

(2) Output group data selector U25 and output group timing selector U24 sequentially select and invert the eight output group data lines and their related timing lines (counts 9 through 16 of address counter). The selected data line is applied in parallel to the group data traffic monitor and the dummy pattern detector and counter. The selected timing line is applied only to the dummy pattern detector and counter.

(3) Idle group selector U22 sequentially selects the activity select (ACT) lines to appear at its two outputs as the IDLE and IDLE— signals. ACT 1 is selected during counts 1 and 9 of the address counter, ACT 2 is selected during counts 2 and 10, and so on. If a given group is not being used (inactive), as determined by its card-mounted switch on the related DGP card being placed to OFF, its ACT line will be at a high level. In turn, when that group is selected by the selector, the IDLE output will be high and the IDLE— output will be low. These IDLE and IDLE— outputs force a good status condition to be stored by AD card 21A1 for that group. This action inhibits alarms for groups not being used.

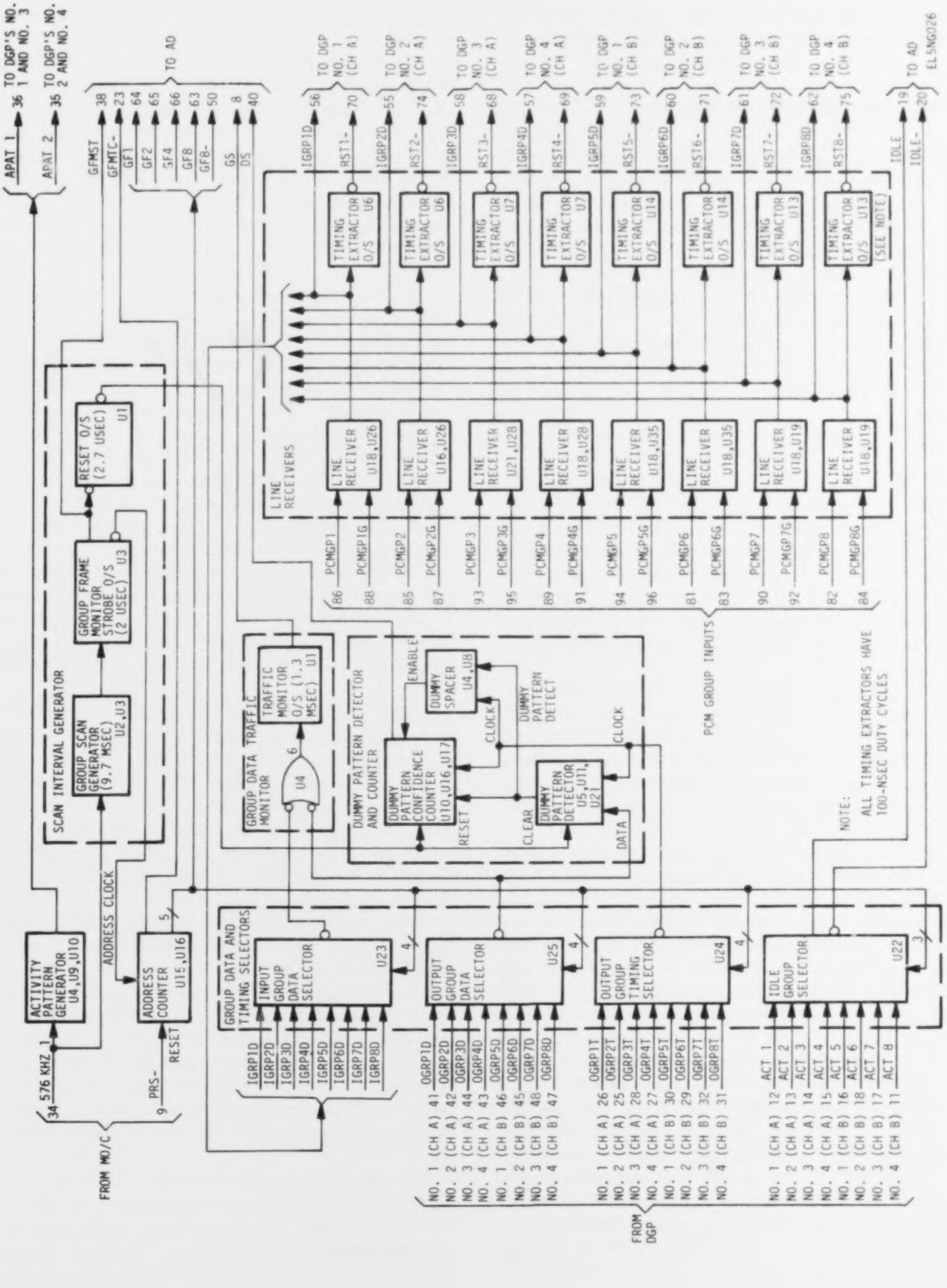
f. Group Data Traffic Monitor. The group data traffic monitor monitors the selected input group or output group data line for the presence of traffic (activity). Each data transition from a logic 0 to a logic 1 retriggers traffic monitor one-shot U1. In normal operation, there are sufficient data transitions to keep U1 retriggered and its good status (GS) output high. However, if traffic for the selected group is not present, U1 will time out and the GS output will go low. This status will be stored by AD card 21A1, causing the related INPUT ALARMS or OUTPUT ALARMS indicators on the front panel and the RAU to light.

g. Dummy Pattern Detector and Counter. The dummy pattern detector and counter searches the output group data line connected to it for a dummy pattern (a unique repetitive 7-bit pattern) that may have been inserted by a far-end multiplexer in place of data.

(1) Data bits are consecutively clocked into the dummy pattern detector, which is made up of a shift register (U5), inverters (U21), and a gate (U11). When a dummy pattern is detected, the dummy spacer enables the dummy pattern confidence counter. The dummy patern detect signal directs the counter to increment one count at the next clock. Thereafter, the dummy spacer enables the confidence counter every 7th clock (when another dummy pattern is expected).

(2) The confidence counter will increment one count if a dummy pattern is detected or will decrement one count if a dummy pattern is not detected. When the counter reaches a count of 8, the dummy sync (DS) signal is generated and routed to AD card 21A1. The AD card stores this status and causes the DUMMY SIGNAL indicators on the front panel and the RAU to light. At the start of each scan interval, the dummy pattern confidence counter is reset to zero and the shift register in the dummy pattern detector is cleared.

h. Activity Pattern Generator. The activity pattern generator is clocked by the 576 KHZ 1 input and gen-



FROM MO/C
34 576 KHZ 1
9 PRS-
RESET
ACTIVITY PATTERN GENERATOR U4,U9,U10
ADDRESS COUNTER U15,U16
ADDRESS CLOCK
5
SCAN INTERVAL GENERATOR
GROUP SCAN GENERATOR (9.7 MSEC) U2,U3
GROUP FRAME MONITOR STROBE O/S (2 USEC) U3
RESET O/S (2.7 USEC) U1
APAT 1 36 TO DGP'S NO. 1 AND NO. 3
APAT 2 35 TO DGP'S NO. 2 AND NO. 4
GFMST 38
GFMTC- 23
GF1 64
GF2 65
GF4 66
GF8 63
GF8- 50
GS 8
DS 40
TO AD
GROUP DATA TRAFFIC MONITOR
TRAFFIC MONITOR O/S (1.3 MSEC) U1
U4
6
DUMMY PATTERN DETECTOR AND COUNTER
DUMMY PATTERN CONFIDENCE COUNTER U10,U16,U17
DUMMY SPACER U4,U8
DUMMY PATTERN DETECTOR U5,U11,U21
ENABLE
CLOCK
DUMMY PATTERN DETECT
RESET
CLEAR
DATA
LINE RECEIVERS
LINE RECEIVER U18,U26
LINE RECEIVER U16,U26
LINE RECEIVER U21,U28
LINE RECEIVER U18,U28
LINE RECEIVER U18,U35
LINE RECEIVER U18,U35
LINE RECEIVER U18,U19
LINE RECEIVER U18,U19
86 PCMGP1
88 PCMGP1G
85 PCMGP2
87 PCMGP2G
93 PCMGP3
95 PCMGP3G
89 PCMGP4
91 PCMGP4G
94 PCMGP5
96 PCMGP5G
81 PCMGP6
83 PCMGP6G
90 PCMGP7
92 PCMGP7G
82 PCMGP8
84 PCMGP8G
PCM GROUP INPUTS
TIMING EXTRACTOR O/S U6
TIMING EXTRACTOR O/S U6
TIMING EXTRACTOR O/S U7
TIMING EXTRACTOR O/S U7
TIMING EXTRACTOR O/S U14
TIMING EXTRACTOR O/S U14
TIMING EXTRACTOR O/S U13
TIMING EXTRACTOR O/S U13 (SEE NOTE)
IGRP1D 56
RST1- 70
TO DGP NO. 1 (CH A)
IGRP2D 55
RST2- 74
TO DGP NO. 2 (CH A)
IGRP3D 58
RST3- 68
TO DGP NO. 3 (CH A)
IGRP4D 57
RST4- 69
TO DGP NO. 4 (CH A)
IGRP5D 59
RST5- 73
TO DGP NO. 1 (CH B)
IGRP6D 60
RST6- 71
TO DGP NO. 2 (CH B)
IGRP7D 61
RST7- 72
TO DGP NO. 3 (CH B)
IGRP8D 62
RST8- 75
TO DGP NO. 4 (CH B)
IDLE 19
IDLE- 20
TO AD
GROUP DATA AND TIMING SELECTORS
INPUT GROUP DATA SELECTOR U23
OUTPUT GROUP DATA SELECTOR U25
OUTPUT GROUP TIMING SELECTOR U24
IDLE GROUP SELECTOR U22
4
4
4
3
IGRP1D
IGRP2D
IGRP3D
IGRP4D
IGRP5D
IGRP6D
IGRP7D
IGRP8D
NO. 1 (CH A) 41 OGRP1D
NO. 2 (CH A) 42 OGRP2D
NO. 3 (CH A) 44 OGRP3D
NO. 4 (CH A) 43 OGRP4D
NO. 1 (CH B) 46 OGRP5D
NO. 2 (CH B) 45 OGRP6D
NO. 3 (CH B) 48 OGRP7D
NO. 4 (CH B) 47 OGRP8D
NO. 1 (CH A) 26 OGRP1T
NO. 2 (CH A) 25 OGRP2T
NO. 3 (CH A) 28 OGRP3T
NO. 4 (CH A) 27 OGRP4T
NO. 1 (CH B) 30 OGRP5T
NO. 2 (CH B) 29 OGRP6T
NO. 3 (CH B) 32 OGRP7T
NO. 4 (CH B) 31 OGRP8T
NO. 1 (CH A) 12 ACT 1
NO. 2 (CH A) 13 ACT 2
NO. 3 (CH A) 14 ACT 3
NO. 4 (CH A) 15 ACT 4
NO. 1 (CH B) 16 ACT 5
NO. 2 (CH B) 18 ACT 6
NO. 3 (CH B) 17 ACT 7
NO. 4 (CH B) 11 ACT 8
FROM DGP
NOTE:
ALL TIMING EXTRACTORS HAVE 100-NSEC DUTY CYCLES
EL5NG026

Figure 2-26. GTM card 21A2, block diagram.

erates two continuous activity patterns (APAT 1 and APAT 2). Each activity pattern is 7 bits long (1011000) (last bit in time shown on left) and is repetitive. APAT 2 lags APAT 1 by three bit times.

2-49. Theory of Operation.

(fig. FO-12)

a. General. This paragraph describes the detailed operation of the circuits on GTM card 21A2. The theory of operation is divided into the seven functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Line receivers (*b* below).
(2) Scan interval generator (*c* below).
(3) Address counter (*d* below).
(4) Group data and timing selectors (*e* below).
(5) Group data traffic monitor (*f* below).
(6) Dummy pattern detector and counter (*g* below).
(7) Activity pattern generator (*h* below).

NOTE

The sheet number references in *b* through *h* below refer to figure FO-12.

b. Line Receivers (sheets 4 and 5). There are eight identical line receivers and timing extractor one-shots—one for each of the eight possible PCM group inputs. Therefore, the following discussion relating to the line receiver and timing extractor one-shot associated with the PCM group 1 input is applicable for the other seven.

(1) Comparator U26-1 and inverter U18-6 form the line receiver for the PCM group 1 input (PCMGP1). The line receiver converts the PCM NRZ input (logic 1 is approximately 0 v and a logic 0 is approximately −2 v) to a TTL NRZ format (logic 1 is approximately +5 v and a logic 0 is approximately 0 v).

(2) Zener diode VR1, together with resistors R18 and R21, develop and approximate −1 v threshold level at noninverting input pin U26-12. This threshold level prevents low-level noise on the incoming PCM line from being processed as data by the comparator. When a logic 1 (0 v) is applied to pin U26-13, the output at U26-1 is slightly negative (less than 1 v), causing U18-6 to produce a TTL logic 1 output. When a logic 0 (−2 v) is applied to pin U26-13, the output at U26-1 is approximately +3 v, causing U18-6 to produce a TTL logic 0 output.

(3) Each positive-going transition at U18-6 (data transition from a logic 0 to a logic 1) triggers U6-4 to produce a nominal 100-nanosecond negative reset strobe (RST1—). RST1— is used on the associated DGP card to control creation of an extracted 576 kHz clock that is synchronized with the incoming PCM data.

c. Scan Interval Generator. Figure 2-27 is a timing diagram showing the end of one scan interval and the start of a new scan interval. Reference should be made to the timing diagram throughout the following discussion.

(1) While a scan interval is in process, the output of U3-13 (sheet 2) is high (U3-13 was triggered on at the start of the scan interval). When U3-13 times out after approximately 9.7 milliseconds, its output goes low and is routed through backplane jumper GTMCT06 to the K input of flip-flop U2-10. This allows the next positive transition of the 576 KHZ 1 clock to toggle U2-10 reset (U2-10 was set due to the high-level input to its K pin at the start of the scan interval).

(2) The negative transition at U2-10 triggers U3-5 into a nominal 2-microsecond duty cycle. The positive pulse output from U3-5 is the group frame monitor strobe (GFMST) that enables AD card 21A1 to read and store the status of the good status (GS) and dummy sync (DS) outputs of the card (card pins 8 and 40, respectively, on sheet 3). The next positive transition of the 576 KHZ 1 clock toggles U2-10 (sheet 2) set, which triggers U3-13 to start a new scan interval.

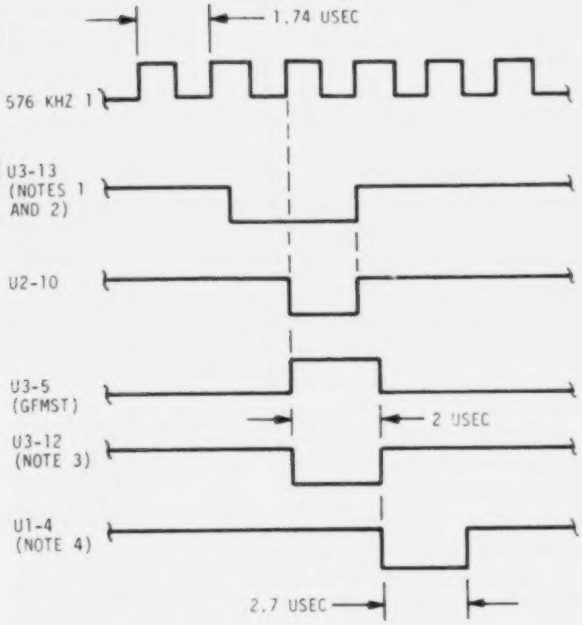
(3) The negative transition at the end of the U3-5 positive pulse output triggers U1-4 into a nominal 2.7-microsecond duty cycle. The positive transition at the end of the U3-12 negative pulse output clocks the address counter (*d* below), causing it to increment one count. The negative pulse output of U1-4 routed through backplane jumper GTMCT02 to preset counter U17 (sheet 3) to zero and to clear shift register U5.

d. Address Counter. Address counter U15 (sheet 2) is clocked (incremented one count) by the positive transition from U3-12 (fig. 2-27) that is routed through backplane jumper GTMCT03. The binary outputs of U15 (pins 14, 13, 12, and 11) cause idle group selector U22, output group timing selector U24, output group data selector U25 (sheet 3), and input group data selector U23 to select the addressed group. The binary outputs are also routed to AD card 21A1 as the group frame scan address bits (GF1, 2, 4, 8, and 8—) to inform the AD card which group is being processed by the GTM card.

e. Group Data and Timing Selectors.

(1) Input group data selector U23 (sheet 3), in response to address counter U15, sequentially selects and inverts the eight input group data lines (counts 1 through 8 of address counter) for application to gate U4-6. The input group data lines (IGRP1D through IGRP8D) are the outputs of the line receivers (sheets 4 and 5).

(2) Output group data selector U25 (sheet 3) and output group timing selector U24 (sheet 2), in response to address counter U15, sequentially select and invert the eight output group data lines (OCRP1D through OGRP8D) and their associated output group timing



NOTES:

1. U3-13 TIME-OUT (POSITIVE-TO-NEGATIVE TRANSITION) OCCURS RANDOMLY WITH RESPECT TO 576 KHZ 1.
2. U3-13 NEGATIVE-TO-POSITIVE TRANSITION STARTS NEW SCAN INTERVAL.
3. U3-12 NEGATIVE-TO-POSITIVE TRANSITION CLOCKS ADDRESS COUNTER U15.
4. U1-4 NEGATIVE OUTPUT CLEARS SHIFT REGISTER U5 AND RESETS COUNTER U17.

EL5NG027

Figure 2-27. Scan interval generator timing diagram.

lines (OGRP1T through OGRP8T). The output group data and timing lines are from the output sections of the respective DGP cards and are selected during counts 9 through 16 of the address counter. The selected output group data line is applied to gate U4-6 (sheet 3) and to shift register U5. The selected output group timing line is applied only to shift register U5.

(3) Idle group selector U22 (sheet 2), in response to address counter U15, sequentially selects the activity select (ACT) lines that are to appear at its two outputs. ACT 1 is selected during counts 1 and 9 of address counter U15, ACT 2 is selected during counts 2 and 10, and so on. If a given group is inactive (its card-mounted switch on DGP card placed to OFF), its ACT line will be high. In turn, when that group is selected by the selector, the IDLE output will be high and the IDLE— output will be low. These IDLE and IDLE— outputs force a good status condition to be stored by AD card 21A1 for that group. This action inhibits alarms for groups that are inactive.

f. Group Data Traffic Monitor (sheet 3). Gate U4-6 and one-shot U1-5 make up the group data traffic monitor. The selected input group data line (U23-14) or selected output group data line (U25-14) is applied through U4-6 to the input of U1-5. Each data transition from a logic 0 to a logic 1 retriggers U1-5. In normal operation, there are sufficient data transitions to keep U1-5 retriggered and its GS output will be high at the end of the scan interval when it is stored in the AD card. However, if there is a loss of traffic for a given group, U1-5 will time out and its GS output will be low at the end of the scan interval when it is stored in the AD card. This will cause the related INPUT ALARMS or OUTPUT ALARMS indicators on the front panel and the RAU to light.

g. Dummy Pattern Detector and Counter.

(1) Data bits from the selected output group data line (U25-14) are consecutively clocked into shift register U5(sheet 3). Without a dummy pattern being detected, the output of gate U4-8 is low, which holds dummy spacer U8 preset at a count of 2 (0010). When an inverted dummy pattern (1011000) (last bit in time shown on left) is contained in U5, the output of gate U11-8 will go low. This causes U4-8 to go high, and on the next clock, U8 will be preset to a count of 10 (1010). The low outputs of U11-8 (routed through backplane jumper GTMCT05) also directs counter U17 to count up, and the low output of U8-11 (U8 has not yet been preset) applied through backplane jumper GTMCT01, gate U10-4, and inverter U16-8 enables counter U17 to increment one count.

(2) Seven clocks later, another 7 bits of data will have been shifted into U5 (U5 should now contain another dummy pattern) and dummy spacer U8 will have advanced seven counts (now contains a count of 0000). The low output of U8-11 again enables counter U17 to either increment (dummy pattern detected) or decrement (no dummy pattern detected) one count. Additionally, the low output of U8-11 will cause U8, at the next clock, to preset once again to a count of 10 (1010). The above process repeats until the end of the scan interval. Counter U17 is inhibited from cycling past a count of 15 (1111). If U17 has advanced to a count of 8 or more by the end of the scan interval, the dummy sync (DS) output is high and will be stored by AD card 21A1. This will cause the DUMMY SIGNAL indicators on the front panel and the RAU to light. The negative pulse output from U1-4 (sheet 2) is routed through backplane jumper GTMCT02 to preset counter U17 to zero and clear shift register U5 so that they can begin another dummy pattern search in the next scan interval.

h. Activity Pattern Generator (sheet 2). Shift register U9, together with gates U4-3 and U10-7, form the activity pattern generator that is clocked by the 576 KHZ 1 input to produce the two continuous activity patterns (APAT 1 and APAT 2). Each activity pattern is 7 bits long (1011000) (last bit in time shown on left) and is repetitive. APAT 2 lags APAT 1 by three bit times.

Section XIV. ALARM DETECTOR (AD) CARD 21A1

2-50. General

This section contains separate block diagram and theory of operation discussions of the functional circuits on the AD card. There is one AD card (21A1) in the TD-976/G. The AD card monitors various signals and functions within the TD-976/G, and if the required signals and functions are not detected, controls sounding of an audible alarm on the front panel and/or lighting of visual alarm indicators on the front panel and the RAU. Additionally, orderwire control circuits process incoming orderwire calls to light the CALL indicators on the front panel and the RAU and sound the audible alarm on the front panel to alert the operator that an orderwire call is being received by the TD-976/G. The block diagram discussion in paragraph 2-51 is based on the AD card block diagram in figure 2-28. The theory of operation in paragraph 2-52 is based on the AD card schematic diagram in figure FO-13.

2-51. Block Diagram Discussion

(fig. 2-28)

a. General. The block diagram discussion is divided into 10 functional circuit descriptions as follows:

(1) The input gates (*b* below) enable status regarding the eight input groups and the eight output groups to be entered into storage.

(2) The input group status storage and alarm drivers (*c* below) store input group status and provide the status on separate lines to INPUT ALARMS indicators on the front panel and the RAU.

(3) The output group status storage and alarm drivers (*d* below) store output group status and provide the status on separate lines to OUTPUT ALARMS indicators on the front panel and the RAU.

(4) The dummy storage, combiner gates, and driver (*e* below) store output group status relating to whether a dummy pattern was received by the demultiplexer section for one or more groups and provide an output to the DUMMY SIGNAL indicators on the front panel and the RAU.

(5) The alarm clear circuits (*f* below) clear the status storage circuits upon equipment power turn-on and selectively clear them after certain faults are detected.

(6) The traffic and fault gates (*g* below) provide outputs to an audible alarm modulator/driver and also drive the CABLE SIGNAL and EQUIP ALARM indicators on the front panel and the RAU.

(7) The audible alarm modulator/driver (*h* below), under certain fault conditions, creates a square wave signal that causes the audible ALARM horn on the front panel to produce an alternating on-off beeping sound.

(8) The orderwire control circuits (*i* below) light orderwire call indicators and initiate a continuous tone from the audible ALARM horn in response to incoming orderwire calls.

(9) The sync/RNOCLK gates (*j* below) selectively light front panel, RAU, and circuit card indicators when demultiplexer section timing is lost or when major frame synchronization is not maintained by the demultiplexer section.

(10) The alarm test driver (*k* below) simultaneously enables the various on-card alarm drivers to light all alarm and status indicators on the front panel and the RAU.

b. Input Gates. As explained in section XIII, GTM card 21A2 sequentially examines the eight input group data lines for the presence of traffic, and the eight output group data lines for the presence of traffic and a dummy pattern. The time during which each data line is examined is termed a scan interval. At the end of each scan interval, GTM card 21A2 generates a group frame monitor strobe (GFMST) that enables the AD card to store the status for that group. GTM card 21A2 also generates group frame scan address bits (GF1, 2, 4, 8, and 8—), in binary form, that signify which input or output group data line is being examined.

(1) The strobe/enable gates, in response to GFMST, GF8, and GF8— inputs, control enabling of the status storage circuits. GF8— is a high level during the first eight scan intervals of GTM card 21A2 (input groups 1 through 8 being examined) and allows each GFMST pulse to enable the status storage for the input groups. Conversely, GF8 is a high level during the second eight scan intervals (output groups 1 through 8 being examined) and allows each GFMST pulse to enable the status storage for the output groups and the dummy storage.

(2) The status of each data line examined by GTM card 21A2 is gated through the data gates to the status storage circuits. The IDLE, GS, and DS inputs make up the data that are gated to status storage for the input and output groups. DS and IDLE— make up the data that are gated to the dummy storage. The good status (GS) input is a high level whenever the group being ex-

amined by the GTM card has traffic (activity). The dummy sync (DS) is a high level whenever the output group being examined by the GTM card contains a dummy pattern. If a given group is inactive (corresponding channel switch on DGP card placed to OFF), the IDLE input will be a high level and the IDLE— will be a low level. If the IDLE, GS, and DS inputs are all low (meaning group is active, but no traffic or dummy pattern is detected), the corresponding data output of the data gates will be a high level (for any other combination of inputs, the data output will be a low level). If the IDLE— is a high level and DS is a high level (meaning group is active and a dummy pattern was detected), the corresponding data output to the dummy storage will be a high level (for any other combination of inputs, the data output will be a low level).

c. Input Group Status Storage and Alarm Drivers. Status storage circuit U9, which stores status for the eight input groups, has eight latches that are individually selected for data entry and storage. Incrementing group frame scan address bits (GF1, 2, and 4) sequentially address (select) the eight latches for data entry. Enable lows applied from the strobe/enable gates at the end of scan intervals 1 through 8, in turn, enter the successively applied data levels (low level for good status or high level for bad status) into the sequentially selected latches. In turn, when the stored status for a given input group is a high level (meaning group is active, but no traffic is detected), the input good status (IGS—) output is a high level and causes the appropriate DGP card to insert a dummy pattern in place of data for that group. Additionally, the high level is outputted through the input alarm drivers and causes the corresponding INPUT ALARMS indicators on the front panel and the RAU to light, signifying a loss of traffic for that input group (para 2-15*b*).

d. Output Group Status Storage and Alarm Drivers. Status storage circuit U11, which stores status for the eight output groups, operates like circuit U9 (*c* above). Enable lows applied from the strobe/enable gates at the end of scan intervals 9 through 16, in turn, enter the successively applied data levels (low level for good status or high level for bad status) into the sequentially selected latches. When the stored status for a given output group is a high level (meaning group is active, but no traffic or dummy pattern is detected), the resulting output applied through the output alarm drivers causes the corresponding OUTPUT ALARMS indicators on the front panel and the RAU to light, signifying a loss of traffic for that output group (para 2-15*c*).

e. Dummy Storage, Combiner Gates, and Driver. Dummy storage circuit U4 operates like output group status storage circuit U11, except that its data input is on a different line and provides status relating to whether a dummy pattern was detected in the output group data. The same enable pulses that enter output group status also enter dummy status into U4 after scan intervals 9 through 16. Four combiner OR gates converge dummy storage circuit U4's stored levels into a single output line. When an output group has recurring dummy patterns instead of normal data traffic, the corresponding U4 latch is set. The resulting high-level dummy lamp (DMLPS) output causes the DUMMY SIGNAL indicators on the front panel and the RAU to light, signifying that a dummy pattern has been detected in one or more output groups (para 2-15*e*).

f. Alarm Clear Circuits. The alarm clear circuits selectively clearly all or part of the status storage circuits upon equipment power turn-on and when certain faults are detected. Clearing of a status storage circuit prevents the associated alarm indicators from lighting (para 2-15*g*).

(1) During equipment power turn-on, the low-level power on reset (PRS-) input causes status storage circuits U9, U11, and U4 to be cleared. These circuits remain cleared until GTM card 21A2 completes its first series of 16 scan intervals and generates the group frame monitor teminal count (GFMTC-) signal to reset the alarm clear circuits.

(2) A transmit diagnostic fault (TDFALT) input from the multiplexer section causes only U9 to be cleared. A receive diagnostic fault (RDFALT input from the demultiplexer section causes U11 and U4 to be cleared.

g. Traffic and Fault Gates. Three gate circuits provide outputs to the audible alarm modulator/driver. Additionally, two of the gate circuits also drive the CABLE SIGNAL and EQUIP ALARM indicators on the front panel and the RAU.

(1) The group input traffic gates monitor input group status levels from the eight input alarm drivers. Whenever a bad status condition (loss of traffic for and input group) exists for any input group, the group input traffic gates provide a low-level input to gate U10-6.

(2) The cable output traffic gates monitor the transmit error (XMTERR) signal from the driver section of SG D/R card 21A9. When there is no SG output from SG D/R card 21A9, XMTERR goes high, enabling the cable output traffic gates to produce the SG cable lamp (SGCLPS) signal that causes the CABLE SIGNAL indicators on the front panel and the RAU to light. The cable output traffic gates also provide a low-level input to gate U10-6 whenever the XMTERR input is high (para 2-15*d*).

(3) The diagnostic fault gates monitor the TDFALT and RDFALT lines. Whenever either line is active (high), indicating a detected fault in the multiplexer or demultiplexer section, the diagnostic fault gates produce the equipment lamp (EQLPS) signal

that causes the EQUIP ALRAM indicators on the front panel and the RAU to light. The diagnostic fault gates also provide a low-level input to gate U10-6 when either the TDFALT or RDFALT line is high (para 2-15*f*).

h. Audible Alarm Modulator/Driver. This circuit operates the audible ALARM horn on front panel 21A14 to produce either a continuous sound or an alternating on-off beeping sound. An active orderwire call signal (low) causes the ALARM horn to produce a continuous sound. A diagnostic fault input initiates a delay through gate U10-6. If the diagnostic fault input is still active after delay timeout, the circuit modulates its audible alarm (AALRM—) output signal with a square wave. The square wave causes the ALARM horn to produce an alternating on-off beeping sound.

(1) Delay one-shot U27 turns on for a 1.3-second duty cycle when triggered by the leading edge of a fault detect high from gate U10-6. The triggered one-shot's complementary outputs go to latch U20 (low) and gate U25 (high).

(2) Latch U20 provides a conditioning low to gate U25, while one-shot U27 delays initiation of an alarm tone. Normally, a U10-6 low holds the latch reset to inhibit gate U25 with a high. However, upon fault detection and triggering of U27, a U27 low sets the latch and a U27 high inhibits the gate. If the fault clears within 1.3 seconds, a U10-6 low resets latch U20 as soon as U27 times out so that the ALARM horn cannot be activated. Conversely, if the fault persists beyond U27 timeout, a U27 output low enables a gate U25 output high. This high lets the audible alarm modulator generate a 1.25 Hz square wave that causes the ALARM horn to produce an alternating on-off beeping sound.

(3) The audible alarm modulator consists of flip-flop U20 and its controlling gates U1 and U15. Gate U1 monitors alarm enable inputs from the alarm test driver and diagnostic fault inputs from gate U15. In turn, gate U15 monitors an audible alarm reset switch (AARSSW) input and the fault detect level from gate U25-4. Normally, the control gates maintain the flip-flop in a reset state, holding the circuit's AALRM— output high. An alarm test or detected fault low goes high through gate U1 and lets the flip-flop toggle at a 2.5 Hz rate. The toggling activity produces a 1.25 Hz square wave output to gate U6-12.

(4) Multivibrator U28 oscillates at a 2.5 Hz rate and supplies its output through the limiter/buffer to clock audible alarm modulator flip-flop U20. VR1 limits the square wave output of the multivibrator to a TTL compatible level. The TTL level square wave inverts and restores through buffers U25 and U18 to the clock input of audible alarm modulator flip-flop U20.

(5) Gate U6-12 inverts either active input (square wave from U20 or high from order wire gates) to drive the audible alarm drivers. In turn, the audible alarm drivers produce the AALRM— output. A continuous AALRM— low (orderwire call signal) produces a continuous sound from the ALARM horn. Intermittent AALRM— lows (fault alarm signal) produce an alternating on-off beeping sound from the ALARM horn.

i. Orderwire Control Circuits.

(1) Six gates monitor orderwire call and alarm test inputs and respond with enable outputs for off card use.

(*a*) Gate U10 outputs a high when DDCAL—, DVCAL—, or AVCAL— is low. The U10 output high forces the audible alarm dirver's AALRM—— output low to produce a continuous sound from the ALARM horn. The U10 high also enables the console audible alarm switch (CNSAUD—) output from Q1.

(*b*) Gate U26 inverts an active digital data call (DDCAL—) low to a digital data call signal (DDCALS) high. The high lights the TTY CALL indicator on RAU 21A15.

(*c*) Gates U26 and U21 simultaneously invert an active digital voice call (DVCAL—) low to digital voice and remove digital voice call signal (DVCALS and RDVCALS) highs. DVCALS lights the VOICE O.W. SYSTEM CALL indicator on front panel 21A14. RDVCALS lights the VO ORDW SYSTEM CALL indicator on RAU 21A15.

(*d*) Two gates U17 simultaneously invert an active analog voice call (AVCAL—) low to analog and remote analog voice call signal (AVCALS and RAVCALS) highs. AVCALS lights the VOICE O.W. CABLE CALL indicator on front panel 21A14. RAVCALS lights the VO ORDW CABLE CALL indicator on RAU 21A15.

(2) Console audible alarm switch Q1 puts its CNSAUD— output low when a DDCAL—, DVCAL—, or AVCAL— low is received on the AD card. CNSAUD— goes through RAU 21A15 to an external orderwire control panel, where it can be used to operate a call indicator or alarm.

j. Sync/RNOCLK Gates. These gates monitor the SYNC 8 input from FS card 21A7 and the RNOCLK input from TC (D) card 21A5.

(1) The SYNC 8 input is active (high) whenever the four-stage major frame sync confidence counter on FS card 21A7 has incremented eight or more counts from its maximum confidence condition (para 2-15*f*(5)). The RNOCLK input is active (high) whenever the clock detector on TC (D) card 21A5 times out because the receive master clock (RMASCLK) is not being supplied by SG D/R card 21A9 (para 2-15*f*(3)).

(2) If either of the above inputs is active, the sync/RNOCLK gates produce the SG sync lamp (SGSLPS) signal that causes the FRAME ALARM indicators on the front panel and the RAU to light. Additionally, the RDEP2 output causes TC (D) card

21A5 to create the RDFALT signal that is returned to the AD card. The RDFALT input causes U11 and U4 to be cleared (*f*(2) above), the EQUIP ALARM indicators on the front panel and the RAU to light (*g*(3) above), and the audible ALARM horn to produce an alternating on-off beeping sound (*h* above).

k. Alarm Test Driver. An active (high) internal alarm test (INAT) or external alarm test (EXAT) enables the alarm test driver. Pressing the ALARM TEST switch on the front panel puts INAT high; placing the LAMP switch on the RAU to TEST puts EXAT high. Either high enables the alarm test driver, which causes all front panel and RAU indicators to light. Additionally, the audible ALARM horn on the front panel is enabled to produce an alternating on-off beeping sound.

2-52. Theory of Operation

(fig. FO-13)

a. General. This paragraph describes the detailed operation of the circuits on AD card 21A1. The theory of operation is divided into the 10 functional circuit descriptions established in the block diagram discussions, as listed below.

(1) Input gates (*b* below).

(2) Input group status storage and alarm drivers (*c* below).

(3) Output group status storage and alarm drivers (*d* below).

(4) Dummy storage, combiner gates, and driver (*e* below).

(5) Alarm clear circuits (*f* below).

(6) Traffic and fault gates (*g* below).

(7) Audible alarm modulator/driver (*h* below).

(8) Orderwire control circuits (*i* below).

(9) Sync/RNOCKL gates (*j* below).

(10) Alarm test driver (*k* below).

NOTE

The sheet number references in *b* through *k* below refer to figure FO-13.

b. Input Gates. The input gates translate successively applied control, timing, and scanned status signal combinations into status levels and corresponding strobe outputs. A strobe occurs as each scan interval ends. The strobes sequentially enter input group, output group, and dummy status levels into applicable status storage circuits (*c*, *d*, and *e* below).

NOTE

GTM card 21A2 sequentially examines input groups 1 through 8 for the presence of traffic, and then output groups 1 through 8 for the presence of traffic and a dummy pattern. If traffic is present on the group line being examined, the good status (GS) input is high. If a dummy pattern is detected on the output group line being examined, the dummy sync (DS) input is high. If a given group is inactive (corresponding switch on DGP card placed to OFF), the IDLE input will be high and the IDLE— input will be low when that group is examined by the GTM card. The GTM card scans the various group lines in the binary order of its on-card generated group frame scan address bits (GF1, 2, 4, and 8). Timing is such that each scan interval (time during which an input or output group line is examined) lasts about 10 milliseconds. The GTM card generates a 2-microsecond group frame monitor strobe (GFMST) pulse one each scan interval ends. The GF1, 2, 4, and 8 binary signals address AD card status storage circuits for GFMST entry of scanned status levels into specific locations (1 through 8) of each storage circuit.

(1) Strobe enable gates U18-3 and U18-6 (sheet 3) generate short-duration negative pulses in response to GF 8 and GFMST signals from the GTM card. Each negative pulse (strobe) enters an input group, output group, or dummy status level into a GF1, 2, and 4 addressed storage location.

(*a*) A GF8— high conditions gate U18-3 so that it can invert eight successive GFMST strobes while input group status storage circuit U9's address inputs (GF1, 2, and 4) increment during scan intervals 1 through 8. Each gate pin U18-3 strobe pulse briefly enables U9 (sheet 4) during one address input count to enter a scanned input group status level into an addressed U9 location (1 of 8). After eight counts (and U9 strobes), GF8— goes low and inhibits gate U18-3. At the same time, GF8 goes high to gate U18-6.

(*b*) A GF8 high conditions gate U18-6 (sheet 3) so that it can invert eight successive GFMST strobes to output group status and dummy storage circuits U11 and U4, respectively. The gate outputs the pulses as the address inputs to U11 and U4 increment during scan intervals 9 through 16. Each gate pin U18-6 strobe pulse simultaneously enters a scanned output group status level into an addressed U11 location and enters a scanned dummy status level into an addressed U4 location.

(2) Data gates U25-12 and U18-8 (sheet 3) translate scanned status and condition inputs from the GTM card into active status output levels. Successive status outputs are sequentially entered into addressed and strobed locations of storage circuits U9 (sheet 4), U11, and U4.

(*a*) Gate U25-12 (sheet 3) monitors GS, DS, and IDLE signal combinations that are successively applied to its inputs. If a scanned input group is active (IDLE low at pin U25-1) and has normal traffic, a GS high at pin U25-14 inhibits the gate for an output pin U25-12 low. When the scan interval ends, a strobe

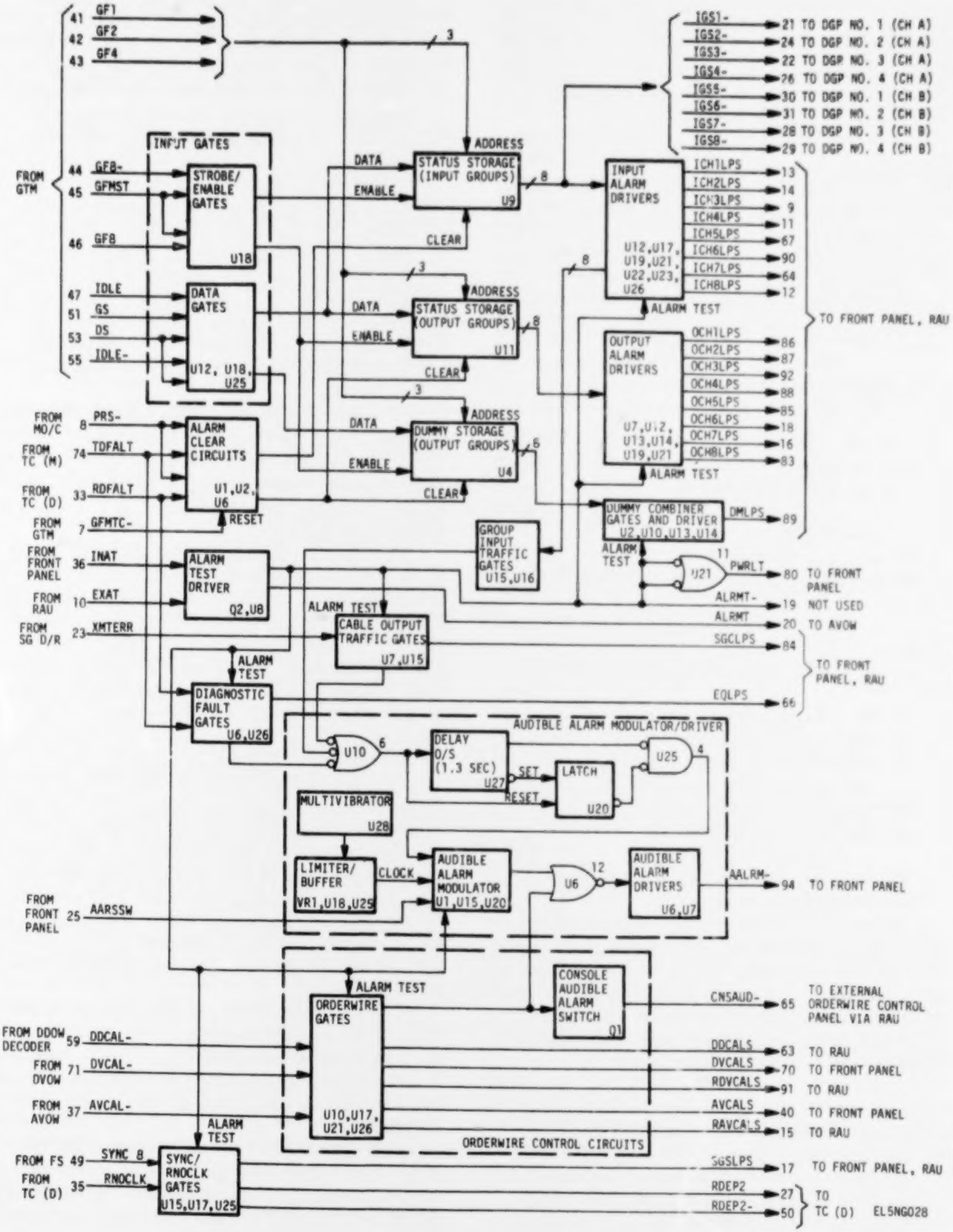

41 GF1
42 GF2
43 GF4
3
IGS1- 21 TO DGP NO. 1 (CH A)
IGS2- 24 TO DGP NO. 2 (CH A)
IGS3- 22 TO DGP NO. 3 (CH A)
IGS4- 26 TO DGP NO. 4 (CH A)
IGS5- 30 TO DGP NO. 1 (CH B)
IGS6- 31 TO DGP NO. 2 (CH B)
IGS7- 28 TO DGP NO. 3 (CH B)
IGS8- 29 TO DGP NO. 4 (CH B)
INPUT GATES
ADDRESS
FROM GTM
44 GFB-
45 GFMST
46 GFB
STROBE/ ENABLE GATES U18
DATA
ENABLE
STATUS STORAGE (INPUT GROUPS) U9
CLEAR
8
INPUT ALARM DRIVERS U12,U17, U19,U21, U22,U23, U26
ICH1LPS 13
ICH2LPS 14
ICH3LPS 9
ICH4LPS 11
ICH5LPS 67
ICH6LPS 90
ICH7LPS 64
ICH8LPS 12
ALARM TEST
TO FRONT PANEL, RAU
47 IDLE
51 GS
53 DS
55 IDLE-
DATA GATES U12, U18, U25
3
ADDRESS
DATA
ENABLE
STATUS STORAGE (OUTPUT GROUPS) U11
CLEAR
8
OUTPUT ALARM DRIVERS U7,U12, U13,U14, U19,U21
OCH1LPS 86
OCH2LPS 87
OCH3LPS 92
OCH4LPS 88
OCH5LPS 85
OCH6LPS 18
OCH7LPS 16
OCH8LPS 83
ALARM TEST
FROM MO/C 8 PRS-
FROM TC (M) 74 TDFALT
FROM TC (D) 33 RDFALT
FROM GTM 7 GFMTC-
ALARM CLEAR CIRCUITS U1,U2, U6
RESET
3
ADDRESS
DATA
ENABLE
DUMMY STORAGE (OUTPUT GROUPS) U4
CLEAR
6
DUMMY COMBINER GATES AND DRIVER U2,U10,U13,U14
DMLPS 89
GROUP INPUT TRAFFIC GATES U15,U16
ALARM TEST
11
U21
PWRLT 80 TO FRONT PANEL
ALRMT- 19 NOT USED
ALRMT 20 TO AVOW
FROM FRONT PANEL 36 INAT
FROM RAU 10 EXAT
ALARM TEST DRIVER Q2,U8
FROM SG D/R 23 XMTERR
ALARM TEST
CABLE OUTPUT TRAFFIC GATES U7,U15
SGCLPS 84
TO FRONT PANEL, RAU
ALARM TEST
DIAGNOSTIC FAULT GATES U6,U26
EQLPS 66
AUDIBLE ALARM MODULATOR/DRIVER
U10
6
DELAY O/S (1.3 SEC) U27
SET
RESET
LATCH U20
U25
4
MULTIVIBRATOR U28
LIMITER/ BUFFER VR1,U18,U25
CLOCK
AUDIBLE ALARM MODULATOR U1,U15,U20
U6
12
AUDIBLE ALARM DRIVERS U6,U7
AALRM- 94 TO FRONT PANEL
FROM FRONT PANEL 25 AARSSW
ALARM TEST
CONSOLE AUDIBLE ALARM SWITCH Q1
ORDERWIRE GATES U10,U17, U21,U26
CNSAUD- 65 TO EXTERNAL ORDERWIRE CONTROL PANEL VIA RAU
FROM DDOW DECODER 59 DDCAL-
FROM DVOW 71 DVCAL-
FROM AVOW 37 AVCAL-
DDCALS 63 TO RAU
DVCALS 70 TO FRONT PANEL
RDVCALS 91 TO RAU
AVCALS 40 TO FRONT PANEL
RAVCALS 15 TO RAU
ORDERWIRE CONTROL CIRCUITS
ALARM TEST
FROM FS 49 SYNC 8
FROM TC (D) 35 RNOCLK
SYNC/ RNOCLK GATES U15,U17,U25
SGSLPS 17 TO FRONT PANEL, RAU
RDEP2 27
RDEP2- 50
TO TC (D)
EL5NG028

Figure 2-28. AD card 21A1, block diagram.

pulse from gate U18-3 ((1)(*a*) above) enters the low into the addressed U9 (sheet 4) storage location. The strobe enters a high if the scanned input group has no traffic (GS low at pin U25-14). Gate U25-12 similarly provides low and high outputs when a scanned output group is active and has or does not have traffic, respectively. However, the gate still provides a low if the scanned output group has recurring dummy patterns instead of normal traffic. In this case, a DS high at pin U25-15 inhibits the gate to put its output low. If the scanned output group does not have traffic or dummy patterns, coinciding IDLE, GS, and DS lows enable a pin U25-12 high. When the scan period ends, a strobe pulse from gate U18-6 ((1)(*b*) above) enters the output of U25-12 into the addressed U11 storage location.

(*b*) Gate U18-8 (sheet 3) provides dummy status information through inverter U12-2 to dummy storage circuit U4. If a scanned active output group has recurring dummy patterns (at least eight counted by GTM card during a scan interval), coinciding IDLE— and DS highs enable a gate pin U18-8 low. This low goes high through U12-2 to U4.

c. Input Group Status Storage and Alarm Drivers (sheet 4).

(1) U9 has eight addressable set/reset latches in which status for the eight input groups is stored. Data enable gate U25-12 (*b*(2)(*a*) above) successively provides scanned input group status levels to data input pin U9-13. Incrementing GF1, 2, and 4 inputs at address pins U9-1, -2, and -3 sequentially select latches 1 through 8 of U9. As each latch is selected, a strobe pulse (low) from gate U18-3 (*b*(1)(*a*) above) to enable pin U9-14 enters the applied status level into the selected latch. A status low (scanned input group is active and has traffic, or is inactive) resets the latch; a status high (input group active but without traffic) sets the latch. The set condition puts the corresponding U9 output pin high to an input alarm driver. A scanned input group 1 fault, for example, sets U9's bit 1 latch and puts the pin U9-4 input good status group 1 (IGS1-) output high. IGS1— is routed to the channel A input section of DGP No. 1 card 21A6. There, IGS1— causes a dummy pattern to be selected for transmission as group 1 data. The alarm clear circuits (*f* below) clear U9 upon equipment power turn-on and when a transmit diagnostic fault is detected.

(2) The input alarm drivers consist of one inverter and a two-input OR gate for each output from status storage circuit U9. Each inverter inverts a status output level to an OR gate, which restores it to an input channel lamp (ICH1LPS through ICH8LPS) output level. For example, U23-2 inverts the input group channel 1 status level from pin U9-4. When high, the status level goes low through U23-2 and restores to a gate pin U22-11 ICH1LPS high. This high initiates audio and visual alarms (para 2-15*b*) for input group 1. The eight input inverters also provide status signals to group input traffic gate U16-8 (*g*(1) below). A common alarm test line (*k* below) to the eight input alarms OR gates provides a means for lighting all INPUT ALARMS indicators during alarm testing.

d. Output Group Status Storage and Alarm Drivers (sheet 3).

(1) Status storage circuit U11 operates like circuit U9 (*c*(1) above), except that it stores status for the eight output groups. Data enable gate U25-12 (*b*(2)(*a*) above) provides the scanned output group status levels to pin U11-13. Strobe enable gate U18-6 (*b*(1)(*b*) above) enters the successively applied status levels into U11's bit latches following scan intervals 9 through 16, in turn. The stored levels go to eight inverter/OR gate output alarm drivers.

(2) The output alarm drivers operate like the input alarm drivers (*c*(2) above), except that they provide output channel lamp (OCH1LPS through OCH8LPS) outputs. A high output lights the corresponding group OUTPUT ALARMS indicators (para 2-15*c*).

e. Dummy Storage, Combiner Gates, and Driver (sheet 3).

(1) Dummy storage circuit U4 operates like output group storage circuit U11, except that data enable gate U18-8 (*b*(2)(*b*) above) provides group dummy status levels to U4 through inverter U12-2. The same strobes (from gate U18-6) enter scanned output group and dummy status levels into U11 and U4, respectively, following scan intervals 9 through 16, in turn. U4's eight stored level outputs go to combiner gates.

(2) Four combiner gates (U2-12, U2-7, U2-9, and U10-12) converge dummy storage circuit U4's stored level outputs into a single output line. For example, gate U2-12 inverts the pin U4-4 output group 1 dummy status level, and gate U10-12 restores it to dummy driver U13-12. The driver inverts the group 1 dummy status level to a dummy lamp (DMLPS) output at gate pin U14-11. When any output group has recurring dummy patterns instead of data, the corresponding U4 latch is set. The resulting U4 output high ultimately puts DMLPS high. A DMLPS high lights DUMMY SIGNAL indicators on the front panel and the RAU (para 2-15*e*).

f. Alarm Clear Circuits (sheet 2). Four 2-input OR gates (U1-3, U1-6, U2-4, and U6-9) make up the alarm clear circuits. The circuits clear all or part of the storage status circuits to prevent indicators from lighting during equipment power turn-on and when certain faults are detected.

(1) Two of the alarm clear circuit gates (U1-6 and U1-3) are wired as a set/reset latch. Upon equipment power turn-on, a pin U1-5 PRS— low from MO/C card 21A4 sets the latch. The resulting pin U1-6 high inverts through gates U2-4 and U6-9 and simultaneous-

ly clears status storage circuits U4, U9, and U11. The high persists and inhibits all INPUT ALARMS OUTPUT ALARMS, and DUMMY SIGNAL indicators while GTM card 21A2 cycles through its first series of 16 scan intervals. Upon completing the first series of scan intervals, the GTM produces the group frame monitor terminal count (GFMTC—) signal to latch pin U1-2. The low resets the latch for a pin U1-6 low output. This low inhibits gates U2-4 and U6-9. The gates' output highs release the three status storage circuits for operation.

(2) Gates U2-4 and U6-9 also monitor receive diagnostic fault (RDFALT) and transmit diagnostic fault (TDFALT) signals from TC (D) and TC (M) cards 21A5, respectively. TDFALT goes high when a fault is detected on the MO/C or TC (M) card. A TDFALT high inverts through gate U6-9 and clears input group status storage circuit U9. RDFALT goes high when a fault is detected on the FS, SG D/R, or TC (D) card. An RDFALT high inverts through gate U2-4 and clears output group status and dummy storage circuits U11 and U4. Either clear action turns off any alarm indicator that may be lit by a stored status high from the affected storage circuit.

g. Traffic and Fault Gates. Three gate circuits provide diagnostic fault detect outputs to the audible alarm modulator's delay circuit (*h*(1) below). If the detected fault persists for longer than 1.3 seconds, the modulator circuit sounds the audible ALARM horn. Two of the gate circuits also directly drive two alarm indicators on front panel 21A14 and RAU 21A15.

(1) Group input traffic gate U16-8 (sheet 4) monitors the eight input group alarm status lines from input group alarm drivers (*c*(2) above). When an input fault is detected, the status line to gate U16-8 goes low. This low goes high through U16-8 and low again through U15-13 to delay activate gate U10-6 (sheet 5).

(2) Cable output traffic gate U7-3 (sheet 5) monitors a transmit error (XMTERR) status signal. A traffic monitor circuit on SG D/R card 21A9 puts XMTERR high when the card's SG output bipolar pulses cease or do not occur frequently enough. The XMTERR high goes low through U15-10 to delay activate gate U10-6 and to gate U7-3. Gate U7-3 restores the low to an SG sync lamp (SGCLPS) high. The SGCLPS high lights the CABLE SIGNAL indicators on the front panel and the RAU and initiates an alternating on-off beeping sound from the audible ALARM horn (para 2-15*d*).

(3) Diagnostic fault gate U6-4 (sheet 2) monitors RDFALT and TDFALT signals from TC (D) and TC (M) cards 21A5. A fault in the multiplexer section causes TDFALT to go high, while a fault in the demultiplexer section causes RDFALT to go high. Either high (RDFALT or TDFALT) goes low through gate U6-4 to delay activate gate U10-6 (sheet 5) and to gate U26-11. Gate U26-11 restores the low to an equipment lamp (EQLPS) high. The EQLPS high lights th EQUIP ALARM indicators on the front panel and th RAU and initiates an alternating on-off beeping sound from the audible ALARM horn (para 2-15(*f*)).

h. Audible Alarm Modulator/Driver. This circuit operates the audible ALARM horn on front pan 21A14 to produce either a continuous sound or an alternating on-off beeping sound. An active digital data, digital voice, or analog voice call (DDCAL—, DVCAL—, or AVCAL—) low causes the ALARM horn to produce a continuous sound. An active input group fault (*g*(1) above), XMTERR (*g*(2) above), or TDFALT or RDFALT (*g*(3) above) first intiates a delay. If the input is still active after delay time out, the circuit modulates its audible alarm output with a square wave. The square wave causes the ALARM horn to produce an alternating on-off beeping sound. An alarm test signal (*k* below) also causes an alternating on-off beeping sound to be produced by the ALARM horn.

(1) Delay one-shot U27 (sheet 5) turns on for a 1.3-second duty cycle when triggered by the leading edge of a high from delay activate gate U10-6. The triggered one-shot's pin U27-12 low and pin U27-5 high outputs go through backplane jumpers ADCT03 and ADCT02 to latch U20-9 and gate U25-4 (sheet 2).

(2) Set/reset latch U20-9 (sheet 2) provides a conditioning low to gate U25-4 while one-shot U2 (sheet 5) delays initiation of an alarm tone. Normally, a pin U10-6 low (no fault detected level) holds latch U20-9 reset so as to inhibit gate U25-4 with a high. However, upon fault detection and triggering of U27, an ADCT03 low from U27-12 sets the latch; an ADCT02 high from U27-5 inhibits gate U25-4. If the fault clears within 1.3 seconds, a low from gate U10-6 resets latch U20-9 as soon as U27 times out so that the ALARM horn cannot be activated. Conversely, if the fault persists for longer than 1.3 seconds, U20-9 remains set, allowing a pin U27-5 timeout low (through ADCT02) to enable a gate pin U25-4 high. This high lets the audible alarm modulator generate a 1.25 Hz square wave that causes the ALARM horn to produce an alternating on-off beeping sound.

(3) The audible alarm modulator consists of flip-flop U20-6 and its controlling gates U1-8 and U15-3 (sheet 2). U1-8 monitors alarm enable inputs from the alarm test driver (*k* below) and gate U15-3. Gate U15-3 monitors an audible alarm reset switch (AARSSW) level (normally high) and the output of gate U25-4. Normally, a low from U25-4 (no persisting fault detected) differs from the AARSSW (high) input, and U15-3 maintains a high output to gate pin U1-9. If an alarm test is not in progress, gate pin U1-10 is also high, inhibiting the gate. The resulting low to flip-flop J pin U20-2 maintains the flip-flop in

a reset state. If either input to gate U1-8 goes low, the resulting high to J pin U20-2 lets the flip-flop toggle at a 2.5 Hz rate. The toggling activity produces a pin U20-6 1.25 Hz square wave output to gate U6-12 ((6) below). Pressing the front panel ALARM TEST switch puts gate pin U1-10 low to immediately initiate an alternating on-off beeping sound from the ALARM horn. Gate U15-3 puts gate pin U1-9 low to initiate an alternating on-off beeping sound from the ALARM horn when input pin U15-1 goes high after a persisting fault is detected. Pressing the ALARM RESET switch puts pin U15-2 low and terminates the beeping sound. Now, when the status changes (fault no longer exists), the output of U25-4 goes low. This causes U15-3 to go low (pin U15-2 is low due to previous pressing of ALARM RESET switch) and initiates an alternating on-off beeping sound from the ALARM horn. Pressing the ALARM RESET switch puts pin U15-2 high and terminates the beeping sound.

(4) Multivibrator U28 (sheet 5) oscillates at a 2.5 Hz rate in response to its reversing polarity feedback inputs. The multivibrator's pin U28-9 output level feeds back to voltage divider R10, R9 and to RC circuit R7, C11. When U28-9 switches states (high out, for example), about one-third of the output level appears as a reference level at the R10, R9 junction and non-inverting pin U28-6. At the same time, the high output starts charging capacitor C11 in a positive direction through resistor R7. The C11 charge level at inverting pin U28-7 exceeds the pin U28-6 reference high in about 200 milliseconds and switches the multivibrator to the opposite (low out) state. During the next half-cycle, an output low charges C11 in a negative direction through R7 until the inverting pin U28-7 level decreases to the pin U28-6 reference low. U28's switching activity produces a 2.5 Hz square wave output to a limiter/buffer.

(5) Zener diode VR1 (sheet 5) limits the positive portion of the square wave output of U28 to approximately +3.3 v. Resistor R12 limits VR1 current. The square wave inverts and restores through buffer U25-9, U18-11. The U18-11 2.5 Hz square wave signal goes out through backplane jumper ADCT01 to clock input pin U20-4 of the audible alarm modulator flip-flop ((3) above).

(6) Gate U6-12 (sheet 2) merges active on-off beeping or continuous enable signals to series-connected audible alarm drivers U6-7 and U7-8. Either active input (square wave from flip-flop U20-6 or high from orderwire gate U10-8) inverts through U6-12, restores through U6-7, and inverts again to an output pin U7-8 audible alarm (AALRM—) signal. A continuous AALRM— low (orderwire call signal) produces a continuous sound from the ALARM horn. Intermittent AALRM— lows (change in fault status) produce an alternating on-off beeping sound.

i. Orderwire Control Circuits (sheet 2).

(1) Six OR gates monitor orderwire call and alarm test inputs and respond with enable outputs for off-card use.

(*a*) Gate U10-8 outputs a high when its DDCAL—, DVCAL—, or AVCAL— input is a low. The pin U10-8 high causes the audible alarm drivers to produce a continuous AALRM— output (*h*(6) above). The high also causes Q1 to produce the console audible (CNSAUD—) output ((2) below).

(*b*) Gate U26-3 inverts an active DDCAl— low to a digital data call signal (DDCALS) high. A DDCALS high lights the TTY CALL indicator on RAU 21A15.

(*c*) Gates U26-8 and U21-6 simultaneously invert an active DVCAL— low to digital voice and remote digital voice call signal (DVCALS and RDVCALS) highs, respectively. DVCALS lights the VOICE O.W. SYSTEM CALL indicator on front panel 21A14. RDVCALS lights the VO ORDW SYSTEM CALL indicator on RAU 21A15.

(*d*) Gates U17-3 and U17-8 simultaneously invert an active AVCAL— low to analog and remote analog voice call signal (AVCALS and RAVCALS) highs, respectively. AVCALS lights the VOICE O.W. CABLE CALL indicator on front panel 21A14. RAVCALS lights the VO ORDW CABLE CALL indicator on RAU 21A15.

(2) Console audible alarm switch Q1 grounds its collector console audible (CNSAUD—) output when a DDCAL—, DVCAL—, or AVCAL— signal is received on the AD card. Gate U10-8 ((1)(*a*) above) inverts the call signal low to a high. Applied through resistor R6, the high forward biases transistor Q1 fully on. Q1 switch-on puts the collector CNSAUD— output low (near ground). CNSAUD— goes through RAU 21A15 to an external orderwire control panel (if used). There, CNSAUD— can be used to operate a call indicator or audible alarm horn.

j. Sync/RNOCLK Gates (sheet 5). Gates U25-7, U17-11, and U15-6 make up the sync/RNOCLK gates circuit. Gate U25-7 monitors a receive no clock signal (RNOCLK) from TC (D) card 21A5 and a receive major frame sync level 8 (SYNC 8) signal from FS card 21A7.

(1) The SYNC 8 input is active (high) whenever the four-stage confidence counter on FS card 21A7 has incremented eight or more counts from its maximum confidence condition. The RNOCLK input is active (high) whenever the clock detector on TC (D) card 21A5 times out because RMASCLK is not being supplied by SG D/R card 21A9. Refer to figure FO-2 and paragraph 2-15*f*(5) and (3), respectively, for system level discussions related to SYNC 8 and RNOCLK diagnostic circuits.

(2) If either of the above inputs is active, it is inverted by U25-7 and restored by U17-11 to produce

the SG sync lamp (SGSLPS) output that causes the FRAME ALARM indicators on the front panel and the RAU to light. U15-6 restores the RDEP2 output, which causes TC (D) card 21A5 to create the RDFALT signal that is returned to the AD card. The RDFALT signal causes U11 and U4 to be cleared (*f*(2) above), the EQUIP ALARM indicators on the front panel and the RAU to light (*g*(3) above), and the audible ALARM horn to produce an alternating on-off beeping sound (*h* above).

k. Alarm Test Driver (sheet 2). Transistor Q2 and series-connected inverters U8-8 and U8-6 make up the alarm test driver circuit. An active internal alarm test (INAT) or external alarm test (EXAT) high enables Q2. Pressing the ALARM TEST switch on the front panel puts INAT high; placing the LAMP switch on the RAU to TEST puts EXAT high. Either high applied through a scaling resistor (R15 or R16) forward biases Q2 fully on. A Q2 collector low inverts to a pin U8-8 alarm test (ALRMT) high. The ALRMT high enables AVOW card cable fault drivers to light CABLE FAULT 1, 2, 4, 8, and 16 indicators on front panel 21A14. ALRMT also goes low through inverter U8-6 to all AD card alarm drivers and to audible alarm modulator activate gate U1-8 (*h*(3) above). The output high of U1-8 immediately lets a flip-flop modulate the ALARM horn to produce an alternating on-off beeping sound. Each alarm driver's output high lights its corresponding indicators on front panel 21A14 and on RAU 21A15. The cable power lamp test (PWRLT) high from U21-11 lights the POWER IN and POWER OUT indicators on the front panel.

Section XV. POWER GENERATION AND DISTRIBUTION

2-53. General

This section contains a detailed block diagram discussion of the overall power generation and distribution circuits in the TD-976/G. This section also contains the block diagram discussion and detailed theory of operation of the circuits in power supply 21A12. Paragraph 2-54 contains the block diagram discussion of the overall power generation and distribution circuits shown in figure 2-29. The power supply block diagram is shown in figure 2-30, and the supporting block diagram discussion is contained in paragraph 2-55. The detailed theory of operation of the power supply is contained in paragraph 2-56 and is based on the power supply schematic diagram in figure FO-14.

2-54. Overall Power Generation and Distribution Block Diagram Discussion

(fig. 2-29)

a. The 115-volt ac source power is applied through a power cable connected to POWER IN connector J26 on the rear of the TD-976/G. The POWER IN connector is physically a part of the rfi filter that is mounted on the rear of the card file. The rfi filter filters out any rf that may be on the applied 115 v ac input, and its ACHOT and ACNEUT outputs are routed to the POWER SUPPLY switch on front panel 21A14. When the POWER SUPPLY switch is placed to ON, ac power is routed through two 3A SLO-BLO 115 VAC fuses as the ACHOTO and ACNEUTO 115 v ac input to power supply 21A12. The POWER AC indicator on the front panel is lighted and remains lit as long as ACHOTO and ACNEUTO are present.

b. When ac power is applied to the power supply, the dc power supply circuits produce regulated +5 v, +12 v, −12 v, and −4.4 v dc output voltages. As shown in figure 2-29, these dc voltages and dc returns are routed to terminals (E4 through E9) on the backplane assembly in the card file. The +5 v and +12 v dc outputs are also routed from the backplane assembly to the front panel as described in *d* below.

c. On the backplane assembly, the +5 v, +12 v, and −12 v dc output voltages are each connected to a bus bar that makes contact with the appropriate power pins of plug-in circuit card connectors J31 through J45. The +5 v bus bar connects to E4 and makes contact with pins 97 through 100 of connectors J31 through J45. The +12 v bus bar connects to E7 and makes contact with pins 1 and 2 of each of the connectors. The −12 v bus bar connects to E8 and makes contact with pins 3 and 4 of each of the connectors. The −4.4 v is distributed to pins 93 and 94 of connectors J35 through J40 from a six-terminal bus bar connected to E9. The dc returns connect to E5 and E6 and make contact with pins 5, 6, 95, and 96 of connectors J31 through J45. The power ground is also routed from E6 to the ground pin of POWER IN connector J26.

d. The +12 v dc applied to the front panel provides the power to energize the audible ALARM horn when it is enabled. The +12 v dc also creates the INAT signal when the ALARM TEST switch is pressed to initiate an alarm test as described in paragraph 2-15*i*. The +5 v dc applied to the front panel provides power to the components on the circuit card assembly and to light POWER DC indicator DS5 when it is enabled.

e. The dc output monitor in the power supply produces the dc indicator enable signal that causes the POWER DC indicator on the front panel to light when all four dc output voltages are normal. When one or more of the dc output voltages are faulty, the dc output monitor circuit removes the dc indicator enable signal. This action turns off the POWER DC indicator to indicate a faulty dc output voltage.

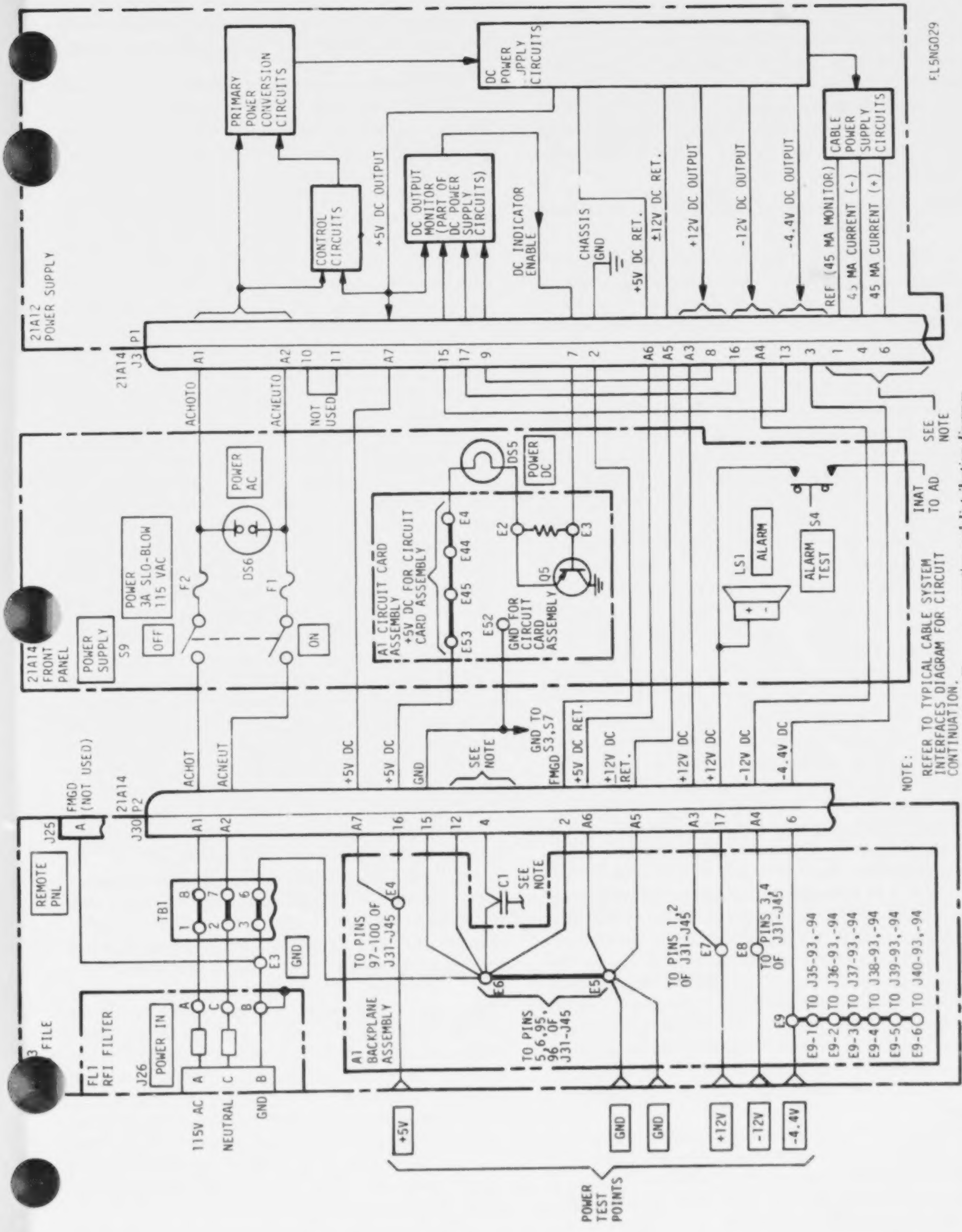

21A12 POWER SUPPLY
PRIMARY POWER CONVERSION CIRCUITS
DC POWER SUPPLY CIRCUITS
CABLE POWER SUPPLY CIRCUITS
CONTROL CIRCUITS
DC OUTPUT MONITOR (PART OF DC POWER SUPPLY CIRCUITS)
+5V DC OUTPUT
DC INDICATOR ENABLE
CHASSIS GND
+5V DC RET.
±12V DC RET.
+12V DC OUTPUT
-12V DC OUTPUT
-4.4V DC OUTPUT
REF (45 MA MONITOR)
45 MA CURRENT (-)
45 MA CURRENT (+)
FL5NG029
P1
21A14 J3
A1 A2 10 11 A7 15 17 9 7 2 A6 A5 A3 8 16 A4 13 3 1 4 6
ACHOTO
ACNEUTO
NOT USED
SEE NOTE
21A14 FRONT PANEL
POWER SUPPLY
S9
OFF
ON
POWER 3A SLO-BLOW 115 VAC
F2
F1
DS6
POWER AC
DS5
POWER DC
A1 CIRCUIT CARD ASSEMBLY +5V DC FOR CIRCUIT CARD ASSEMBLY
E53 E45 E44 E4
E52
GND FOR CIRCUIT CARD ASSEMBLY
E2 E3
Q5
LS1
ALARM
S4
ALARM TEST
INAT TO AD
GND TO S3,S7
SEE NOTE
ACHOT
ACNEUT
+5V DC
+5V DC
GND
FMGD
+5V DC RET.
±12V DC RET.
+12V DC
+12V DC
-12V DC
-4.4V DC
FMGD (NOT USED)
21A14 P2
J30
J25
A
A1 A2 A7 16 15 12 4 2 A6 A5 A3 17 A4 6
REMOTE PNL
TB1
1 8 2 7 3 6
E3
GND
C1
SEE NOTE
TO PINS 97-100 OF J31-J45
E4
E6
E5
TO PINS 5,6,95, 96 OF J31-J45
TO PINS 1,2 OF J31-J45
E7
E8
TO PINS 3,4 OF J31-J45
E9
E9-1 TO J35-93,-94
E9-2 TO J36-93,-94
E9-3 TO J37-93,-94
E9-4 TO J38-93,-94
E9-5 TO J39-93,-94
E9-6 TO J40-93,-94
A1 BACKPLANE ASSEMBLY
3 FILE
FL1 RFI FILTER
J26
POWER IN
A C B
115V AC
NEUTRAL
GND
+5V
GND
GND
+12V
-12V
-4.4V
POWER TEST POINTS
NOTE:
REFER TO TYPICAL CABLE SYSTEM INTERFACES DIAGRAM FOR CIRCUIT CONTINUATION.

Figure 2-29. Overall power generation and distribution diagram.

f. The cable power supply circuits in the power supply produce the regulated 45-milliampere current that powers the cable system as described in the cable power distribution discussion in paragraph 2-60. The cable power supply also produces a REF (45 ma monitor) signal that is applied to the AVOW card as part of the cable system test function as described in paragraph 2-61.

2-55. Power Supply 21A12 Block Diagram Discussion

a. General. As described in the overall power generation and distribution block diagram discussion (para 2-54), the power supply is powered by an ac input from an external source. The power supply can operate when the applied ac input is within the limits of 115 ± 11.5 v, 60 ± 3.0 or 50 ± 2.5 Hz.

(1) *Physical description* (fig. 2-30). The power supply components are mounted on the heat sink assembly as shown in figure 2-30. The high-power components, such as the series regulators, are mounted directly on the heat sink assembly. The low-power electrical components are mounted on one printed circuit board (21A12A1) that is physically attached to the heat sink assembly. The cover for the power supply is held to the heat sink assembly by four sets of screws and washers. The heat sink assembly contains 12 captive screws that secure the power supply to the TD-976/G case. There are no electrical components mounted on the cover.

(2) *Electrical description* (fig. 2-31). The power supply produces four regulated dc voltages (+5, +12, −12, and −4.4) that power the electrical components on the plug-in circuit cards and assemblies in the TD-976/G. The power supply also contains cable power supply circuits that generate the constant 45-milliampere current to power the cable system. As described below, the power supply contains monitor circuits that activate a crowbar switch that shuts down the power supply when the +5 v dc output is determined to be in an overvoltage or overcurrent condition. There is also a monitor circuit for the 45-milliampere cable current output. The monitor circuit activates a crowbar switch that effectively shorts out the 45 (+) to the 45 (−) ma output when the cable system opens or when an overcurrent condition is detected. The block diagram discussion is divided into four circuit descriptions: Control circuits (*b* below), primary power conversion circuits (*c* below), dc power supply circuits (*d* below), and cable power supply circuits (*e* below).

b. Control Circuits. The control circuits monitor the +5 v dc output and generate gate-on pulses that maintain the +5 v dc output at ±0.25 volts. By regulating the +5 v dc output, the other three dc output voltages are also regulated proportionately, since all four of the dc voltages are developed from the secondary windings of power transformer T2 in the dc power supply circuits.

(1) The 115 v ac input is applied to control transformer T1 to produce two stepped-down ac voltages that are applied to the rectifier/filter and the ramp generator. The rectifier/filter produces the dc voltages (+V and −V) that power the control circuits. The 5-volt regulator produces a regulated dc voltage that is applied as a threshold voltage to the +5-volt comparator. The threshold voltage is the key reference voltage that determines the actual output voltages from the dc power supply circuits. The +5-volt comparator compares the +5 v dc output with the threshold voltage and produces a difference voltage that is applied as the dc bias control voltage to the level detector. The dc bias control voltage increases when the +5 v dc output decreases, and decreases when the +5 v dc output increases.

(2) The ramp generator produces a positive-going ramp voltage to the level detector during each half-cycle of the 115-volt ac applied to the circuits. The ramp voltage is summed with the dc bias control voltage to produce a drive pulse output from the level detector. The summed voltages applied to the level detector eventually reach a crossover voltage level that biases the level detector into conduction to produce a negative-going drive pulse. The point in time that the crossover point occurs depends on the amplitude of the dc bias control voltage. The more positive the dc bias control voltage, the sooner the crossover point is reached. In turn, the less positive the dc bias control voltage, the longer is the time it takes to reach the crossover point during the time the ramp signal is being generated. Each drive pulse from the level detector drives the optical isolator into conduction. When the optical isolator conducts, the gate switch is turned on and produces a gate-on pulse that is applied to the primary power conversion circuits.

(3) In summary, a decrease in the +5 v dc output causes the gate-on pulses to occur earlier during each half-cycle of 115-volt ac applied to the circuits. An increase in the +5 v dc output causes the gate-on pulses to occur later during the time that a half-cycle of 115-volt ac is applied. As described in *c* below, the time that a gate-on pulse is generated determines the amount of energy that will be supplied to the power supply circuits. The dc regulation is controlled by the gate-on pulses, which will gate in the exact amount of energy necessary to produce the regulated dc output power within the established tolerances. The turn-on control circuit produces turn-on back-bias voltage that prevents the level detector from producing maximum drive pulses when the 115 v ac input is initially applied to the power supply.

(4) When power is initially applied, it is possible

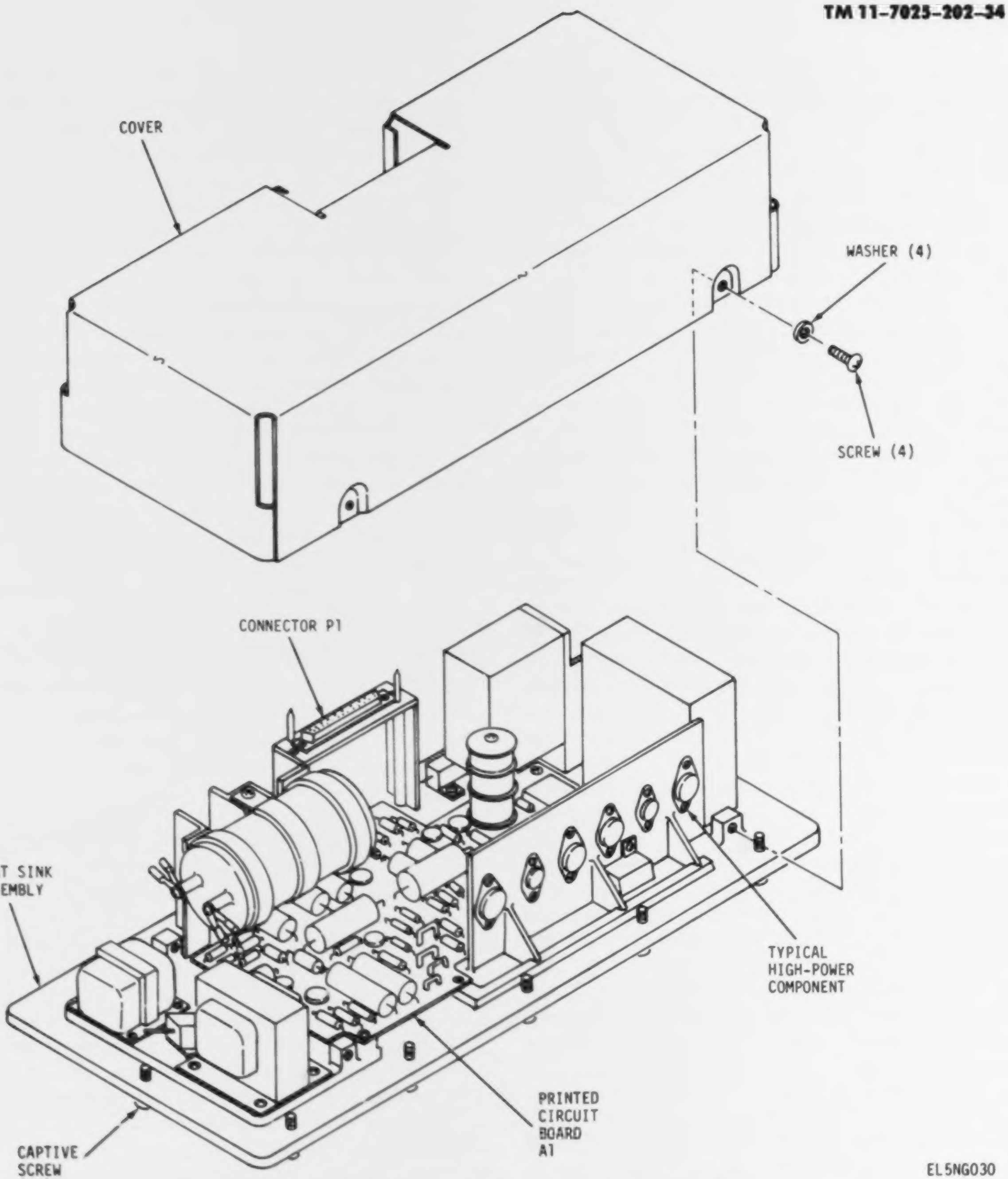

COVER
WASHER (4)
SCREW (4)
CONNECTOR P1
HEAT SINK ASSEMBLY
TYPICAL HIGH-POWER COMPONENT
PRINTED CIRCUIT BOARD A1
CAPTIVE SCREW (12)
EL5NG030

Figure 2-30. Power supply 21A12, major component location diagram.

that the +5-volt comparator would sample no, or an extremely low, +5 v dc output and produce a maximum dc bias control voltage to the level detector. This urn-on configuration prevents a possible overcurrent r overvoltage condition from being initiated during the initial power-up time. The primary power conversion circuits (c below) will sense an overvoltage or overcurrent condition and gate on the crowbar switch, which, in turn, will inhibit the gate switch. This action turns off the power supply (the dc outputs and the 45 ma output) and holds it in that state until the 115 v ac input is interrupted.

c. *Primary Power Conversion Circuits.* These circuits convert the applied 115 v ac input into squared 20 kHz drive pulses that are routed to the power transformer in the dc power supply circuits. These circuits effectively regulate the dc outputs by controlling the amount of energy (voltage level) in the drive pulses applied to power transformer T2. In the primary power conversion circuits, the silicon controlled rectifiers (SCR's) are gated on and accept incoming power until the half-cycle sine wave passes through zero. In normal operation, the time that the gate-on signal is applied with respect to the start of a half-cycle of the sine wave remains fairly constant as long as the power requirements of the circuits in the TD-976/G remain stable. When the power requirements increase, the +5 v dc output starts to decrease, and as described in *b* above, the gate-on pulse occurs earlier. The result is an earlier gate-on time for the SCR's in the bridge circuit so that they conduct for a longer period of time (until sine wave crosses zero). This results in more power being applied through the bridge circuit. When less power is needed, the gate-on pulse occurs later and the SCR's conduct for less time, decreasing the amount of power applied to the filter circuits. The output of the filter circuits is a dc voltage that is routed through an overcurrent monitor to the 20 kHz chopper. When the overcurrent monitor detects an overcurrent condition, an overcurrent gate is generated that inhibits the gate switch in the control circuits. This is done by gating on the crowbar switch, which will remain in conduction until the 115 v ac input is interrupted. The overvoltage monitor also causes the gate switch to be inhibited when an overvoltage condition is detected. The 20 kHz chopper produces the 20 kHz drive pulses to the power transformer in the dc power supply circuits. The amplitude of the drive pulses is proportional to the dc voltage applied to the chopper from the SCR/diode bridge and filter circuits.

d. DC Power Supply Circuits. The dc power supply circuits produce +5, +12, −12, and −4.4 v dc output voltages from the 20 kHz drive pulses applied to power transformer T2. The power transformer produces two stepped-down ac voltages and one stepped-up ac voltage. The stepped-up 390 v ac output is applied to the cable power supply circuits (*e* below). The 26 v ac output is applied to the ± 12-volt rectifier circuits, and the 6 v ac output is applied to the +5-volt rectifier circuit and the −4.4-volt rectifier circuit. The +dc and −dc outputs from the ±12-volt rectifier circuits are filtered through the +12-volt filter circuit and −12-volt filter circuit to produce the +12 v dc and −12 v dc outputs. The dc output of the +5-volt rectifier circuit is filtered through the +5-volt filter circuit to produce the +5 v dc output. In turn, the dc output from the −4.4-volt rectifier circuit is filtered through the −4.4-volt filter circuit to produce the −4.4 v dc output.

e. Cable Power Supply Circuits. The cable power supply circuits produce the constant 45-milliampere cable current to the front panel when the power supply is on (POWER SUPPLY switch is placed to ON). The cable power supply circuits cannot be turned off when the power supply is turned on. However, when the POWER CABLE switch on the front panel is placed to OFF, the 45 ma current (+) and (−) outputs are connected together, effectively shorting out the cable current outputs. The 390 v ac input is rectified into high-voltage dc by the high-voltage rectifier circuit. The dc is filtered through the high-voltage filter circuit and applied through the 45 ma current sensor to the series regulators. The 45 ma current sensor produces a control voltage that regulates the current through the regulators at 45 ± 0.5 milliamperes. The 45 ma current (+) output is routed directly to the front panel. The 45 ma current (−) output is applied through the over/undercurrent monitors to the front panel. When the output current exceeds a nominal 54 milliamperes or drops below a nominal 32 milliamperes, the over/undercurrent monitor generates a gate enable signal to the crowbar switch. The gate enable signal gates on the crowbar switch, which places a low impedance load across the 45 ma current (+) and 45 ma current (−) outputs to effectively short out the cable current outputs. The crowbar remains on until either the 115 v ac input is interrupted or the POWER CABLE switch is placed to OFF.

2-56. Theory of Operation

a. General. This paragraph describes the detailed theory of operation of the circuits in power supply 21A12. The theory of operation is divided into the four functional circuit descriptions established in the block diagram discussion, as listed below.

(1) Control circuits (*b* below).
(2) Primary power conversion circuits (*c* below).
(3) DC power supply circuits (*d* below).
(4) Cable power supply circuits (*e* below).

NOTES

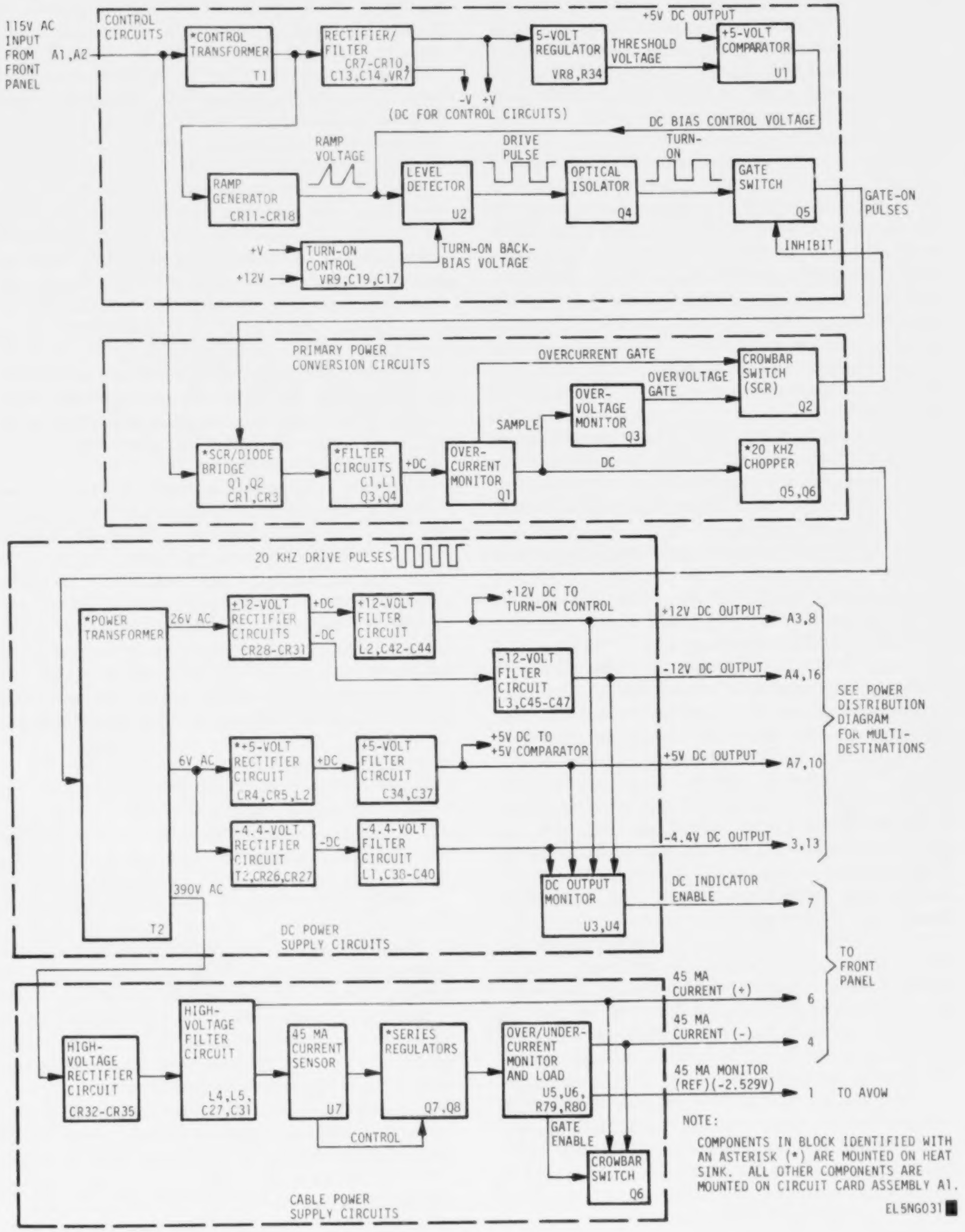
The sheet number references in *b* through *e* below refer to figure FO-14.

In the following discussion, components mounted on the circuit card assembly are prefixed by "A1." Components mounted on the heat sink are identified without a prefix. For example, Q4 is on the heat sink and A1Q4 is on the circuit card assembly.

b. Control Circuits.

(1) The 115 v ac input is applied through P1-A1 and P1-A2 (sheet 1) to the primary of control transformer T1 (sheet 2). Transformer T1 produces a 26-volt, center-tapped, ac signal to rectifier/filter circuit A1CR7 through A1CR10, A1VR7, and associated RC components. The circuit produces dc control voltages (+V and −V) that are approximately +16 v and −16 v dc. The +V and −V outputs supply operating power for the control circuits.

(2) The ac output from T1 is also applied to ramp generator A1CR11 through A1CR18. The circuits produce a positive-going ramp voltage through A1R37 during one half-cycle of the ac sine wave and a posi-


115V AC INPUT FROM FRONT PANEL
A1,A2
CONTROL CIRCUITS
*CONTROL TRANSFORMER T1
RECTIFIER/ FILTER CR7-CR10, C13,C14,VR7
-V
+V
(DC FOR CONTROL CIRCUITS)
5-VOLT REGULATOR VR8,R34
THRESHOLD VOLTAGE
+5V DC OUTPUT
+5-VOLT COMPARATOR U1
DC BIAS CONTROL VOLTAGE
RAMP VOLTAGE
DRIVE PULSE
TURN-ON
RAMP GENERATOR CR11-CR18
LEVEL DETECTOR U2
OPTICAL ISOLATOR Q4
GATE SWITCH Q5
GATE-ON PULSES
INHIBIT
+V
+12V
TURN-ON CONTROL VR9,C19,C17
TURN-ON BACK-BIAS VOLTAGE
PRIMARY POWER CONVERSION CIRCUITS
OVERCURRENT GATE
CROWBAR SWITCH (SCR) Q2
OVERVOLTAGE GATE
OVER-VOLTAGE MONITOR Q3
SAMPLE
*SCR/DIODE BRIDGE Q1,Q2 CR1,CR3
*FILTER CIRCUITS C1,L1 Q3,Q4
+DC
OVER-CURRENT MONITOR Q1
DC
*20 KHZ CHOPPER Q5,Q6
20 KHZ DRIVE PULSES
*POWER TRANSFORMER T2
26V AC
±12-VOLT RECTIFIER CIRCUITS CR28-CR31
+DC
-DC
+12-VOLT FILTER CIRCUIT L2,C42-C44
+12V DC TO TURN-ON CONTROL
+12V DC OUTPUT
A3,8
-12-VOLT FILTER CIRCUIT L3,C45-C47
-12V DC OUTPUT
A4,16
SEE POWER DISTRIBUTION DIAGRAM FOR MULTI-DESTINATIONS
6V AC
*+5-VOLT RECTIFIER CIRCUIT CR4,CR5,L2
+DC
+5-VOLT FILTER CIRCUIT C34,C37
+5V DC TO +5V COMPARATOR
+5V DC OUTPUT
A7,10
-4.4-VOLT RECTIFIER CIRCUIT T2,CR26,CR27
-DC
-4.4-VOLT FILTER CIRCUIT L1,C38-C40
-4.4V DC OUTPUT
3,13
DC OUTPUT MONITOR U3,U4
DC INDICATOR ENABLE
7
390V AC
DC POWER SUPPLY CIRCUITS
TO FRONT PANEL
45 MA CURRENT (+)
6
45 MA CURRENT (-)
4
HIGH-VOLTAGE RECTIFIER CIRCUIT CR32-CR35
HIGH-VOLTAGE FILTER CIRCUIT L4,L5, C27,C31
45 MA CURRENT SENSOR U7
*SERIES REGULATORS Q7,Q8
OVER/UNDER-CURRENT MONITOR AND LOAD U5,U6, R79,R80
45 MA MONITOR (REF)(-2.529V)
1
TO AVOW
CONTROL
GATE ENABLE
CROWBAR SWITCH Q6
CABLE POWER SUPPLY CIRCUITS

NOTE:

COMPONENTS IN BLOCK IDENTIFIED WITH AN ASTERISK (*) ARE MOUNTED ON HEAT SINK. ALL OTHER COMPONENTS ARE MOUNTED ON CIRCUIT CARD ASSEMBLY A1.

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Figure 2-31. Power supply 21A12, block diagram.

tive-going ramp voltage through A1R40 during the other half-cycle of the ac sine wave. This results in application of a positive-going ramp voltage to the inverting input of level detector A1U2-6 that is relatively in phase with each half-cycle of voltage being applied to the SCR/diode bridge (c(1) below).

(3) +5-volt comparator A1U1-6 (sheet 2) compares the +5 v dc output voltage that is applied through A1R39 and A1R38 to inverting pin A1U1-2 with a reference (threshold) voltage developed at the junction of A1R35 and A1R36. Potentiometer A1R34 is adjusted to set the +5 v dc output of the power supply at +5.0 ± 0.1 v dc. When A1R34 is set, any further change in the +5 v dc output will cause a resulting change in the output of A1U1-6, which, in turn, causes an increase or decrease in the time it takes the ramp voltages to reach the crossover point and change the output of level detector A1U2-6. When the +5 v dc output level decreases, A1U1-6 goes more positive and decreases the time it takes the ramp voltage to reach the crossover point. In turn, when the +5 v dc output level increases, A1U1-6 goes more negative and increases the time it takes the ramp voltage to reach the crossover point.

(4) The noninverting input (pin 3) of level detector A1U2-6 is tied through A1R43 to the +5 v return (ground). When the 115 v ac input is initially applied to the circuits, the charging action of A1C19 by the +V and the following charging of A1C17 by the +12 v dc output places a positive potential to the noninverting input that causes A1U2-6 to require a more positive summed voltaged to be applied to pin A1U2-2 to reach the crossover point. The temporary increase in potential to pin A1U2-3 effectively counters any increase in the output of A1U1-6 that could occur by the absence of a low-level +5 v dc output while the power supply circuits are stabilizing during the power-up phase. This circuit configuration ensures that the regulation circuits do not cause a full on condition and possibly turn the power supply off from an overcurrent or overvoltage condition.

(5) When a ramp voltage is not applied to level detector A1U2-6, capacitor A1C18 receives a positive charge through A1CR22. When a ramp voltage is applied to pin 2 of A1U2-6 and the crossover point is reached, the output from A1U2-6 is driven in a negative direction and forces A1C18 to discharge through the diode in optical isolator A1Q4. This forces A1Q4 into conduction and, in turn, biases gate switch A1Q5 into conduction. When switch A1Q5 conducts, the positive-going gate-on pulse is applied through A1R1 and A1R2 (sheet 1) to gate on SCR's Q1 and Q2 in the primary power conversion circuits.

c. Primary Power Conversion Circuits.

(1) The 115 v ac input is applied to SCR/diode bridge CR1, CR3, Q1, and Q2 (sheet 1). During a given half-cycle of the applied 115-volt ac sine wave, the gate-on signal applied through A1R1 and A1R2 from the control circuits gates on either Q1 or Q2. The SCR that has the positive potential applied to its anode will be gated on. During the next half-cycle of the applied 115-volt ac, the opposite SCR is gated into conduction. When an SCR is gated on, it remains in conduction until the ac sine wave crosses the zero reference level to remove the positive potential holding the SCR in conduction. When either Q1 or Q2 conducts, capacitor C1 is positively charged. When P1-A1 is positive with respect to P1-A2, current flows through CR3, L1, C1, and Q1. When P1-A2 is positive with respect to P1-A1, current flows through CR1, L1, C1, and Q2. The length of time that each SCR conducts determines the portion of the applied ac voltage that is transferred into useful power in the power supply circuits. As established in earlier discussions, when more energy is required to sustain the output voltages, the SCR's are gated on sooner and thus conduct for a longer period of time.

(2) The voltage pulses applied through the SCR/diode bridge are filtered into dc mainly by L1, C1, and A1C9 and current regulators Q3 and Q4 (sheet 1). Current regulators Q3 and Q4 function as an active filter that removes any ripple component on the dc voltage applied to the chopper circuits ((5) below).

(3) The dc current through A1R7 (sheet 1 produces a sensing voltage to overcurrent monitor A1Q1. Excessive current through A1R7 biases A1Q1 into conduction. When the +5 v dc output current exceeds approximately 21 amperes, an overcurrent condition exists and A1Q1 is forced into conduction. When A1Q1 conducts, the voltage developed at the junction of A1R9 and A1R10 forces A1VR3 into conduction. When A1VR3 conducts, the voltage developed across A1R11 gates crowbar switch A1Q2 into conduction. When A1Q2 conducts, the current path through A1R17 produces a low potential at the junction of A1R17 and A1R46 (sheet 2) that disables gate switch A1Q5.

(4) If the +5 v dc output level increases above its nominal value, it does so because a more positive dc supply voltage from C1, Q3, and Q4 (sheet 1) is applied to the chopper circuit. If the +5 v dc output level increases to approximately +7.25 volts, an overvoltage condition exists. At this time, the dc supply voltage applied to the chopper circuit is sufficient to cause overvoltage monitor A1Q3 to conduct. When A1Q3 conducts, the voltage developed at the junction of A1R13 and A1R10 causes A1VR3 to conduct the gate on SCR A1Q2. At this time, the power supply is shut down as described in (3) above.

(5) In normal operation, Q5 and Q6 (sheet 1) in the chopper circuit are alternately turned on and off at a 20 kHz rate. The saturation characteristics of the

transformers control the rate at which the stages are turned on and off. When the power supply is initially turned on, the dc supply voltage applied through A1R18 biases either Q5 or Q6 into conduction. When Q5 or Q6 conducts, either terminal 1 or 3 of transformer T2 (sheet 3) is effectively connected to ground potential. The center tap of the primary winding of T2 is returned to the positive voltage at the junction of A1R7 and A1R8 (sheet 1). The overall result is 20 kHz, 120-volt (typical) drive pulses being applied to the primary winding of T2. The secondary windings of A1T1 are connected to the base circuits of Q5 and Q6 so that only one stage is forward biased when the windings are being saturated. When the transformer saturates, the fields reverse and cause the stage that was off to be biased on. Diodes A1CR5 and A1CR6 prevent the positive voltage at the collectors of Q5 and Q6 from becoming more positive than the dc voltage at the junction of A1R7 and A1R8.

d. DC Power Supply Circuits.

(1) The 20 kHz drive pulses applied to the primary winding of transformer T2 (sheet 3) produce two stepped-down ac voltages and one stepped-up ac voltage. The T2-4, T2-5, and T2-6 outputs produce a center-tapped 26-volt ac voltage that is rectified and filtered to produce the +12 v and −12 v dc outputs. Diodes A1CR28 and A1CR29 produce a dc output that is filtered by inductor A1L2 and capacitors A1C42 through A1C44 (sheet 4) to produce the +12 v dc output. Diodes A1CR30 and A1CR31 produce a dc output that is filtered by inductor A1L3 and capacitors A1C45 through A1C47 to produce the −12 v dc output.

(2) The T2-9, T2-10, and T2-11 outputs produce a center-tapped 12-volt ac voltage that is rectified and filtered to produce the +5 v dc output. Diodes CR4 and CR5 produce a dc output that is filtered by inductor L2 and capacitors A1C34 through A1C37 (sheet 4) to produce the +5 v dc output.

(3) The outputs from T2-9, T2-10, and T2-11 are also used to produce the −4.4 v dc output. The ac voltage is applied to transformer T2 and is rectified into a dc voltage by diodes A1CR26 and A1CR27. The ac output is filtered by inductor A1L1 and capacitors A1C38 through A1C41 to produce the −4.4 v dc output.

e. Cable Power Supply Circuits.

(1) The nominal 390-volt ac output from T2-7 and T2-8 (sheet 3) is applied to diode bridge A1CR32 through A1CR35. The dc output of the diode bridge is filtered by inductors A1L4 and A1L5 and capacitor A1C27. The 45 ma current (+) output is connected to output pin P1-6 (sheet 4). The 45 ma current (−) is routed through the monitor circuits and series regulators to P1-4 as described in (2) below.

(2) The 45 ma current (−) is applied through A1R61, A1R71, and A1R72 to series regulators Q8 and Q7 (sheet 3). Zener diode A1VR11, in series with R3 and R4, provides a fixed 22 volts for A1VR12 in series with A1R74. A stable reference voltage developed at the junction of A1VR12 and A1R74 is applied to the noninverting input of current sensor A1U7-6. This reference voltage is positive 6.2 volts with respect to the junction of A1R61 and A1R71. Potentiometer A1R72 is adjusted so that A1U7-6 generates a control voltage to the series regulators that holds the cable current at 45 ±0.5 milliamperes. When the current increases, a less negative (more positive) voltage is developed at the inverting input of A1U7-6 to produce a more negative back-bias voltage to Q8. This causes the current flow through Q8 to decrease and return the cable current toward 45 milliamperes. Conversely, when the cable current decreases, a forward bias is developed that causes Q8 to conduct heavier. These actions maintain the cable current at 45 milliamperes. In summary, cable current flow is from the negative side of A1C27 (sheet 3) through A1R71, A1R72, A1P5, Q8, Q7, A1P6, A1R79, and A1R80 to P1-4, the 45 ma current (−) output of the power supply. From P1-4, cable current flows through the external cable system, returning to P1-6 and back to the positive side of A1C27. The 45 ma current (−) output is connected to ground in the backplane assembly. Therefore, all voltages developed within the power supply prior to the 45 ma current (−) output are negative with respect to ground.

(3) Over/undercurrent monitors A1U5 and A1U6 (sheet 3) gate on crowbar switch A1Q6 whenever the cable current increases to 54 ±2 milliamperes or decreases to 32 ±1 milliamperes. A1U5 is the overcurrent monitor, while A1U6 is the undercurrent monitor. Resistors A1R64, A1R63, A1R62, A1R65, A1R66, and A1R67 form a voltage divider that controls the operation of A1U5 and A1U6. A1R68 and A1VR13 hold the A1R67 end of the voltage divider at approximately +6.2 v dc. The A1R64 end of the voltage divider is a negative voltage whose value depends on the amount of cable current flow through A1R79 and A1R80. With a nominal 45 ma cable current, the voltage developed across A1R79 and A1R80 and applied to the A1R64 end of the voltage divider is −4.43 volts. Under this normal condition, the voltage developed at the A1R64, A1R63 junction is slightly negative and the voltage developed at the A1R62, A1R65 junction is slightly positive, causing the outputs of A1U5-6 and A1U6-6 to be negative. An overcurrent condition of 54 ma will cause approximately −5.31 volts to be applied to the A1R64 end of the divider, resulting in the A1R62, A1R65 junction becoming slightly negative. This causes the output of A1U5-6 to go positive. Conversely, an undercurrent condition of 32 ma will cause approximately −3.15

volts to be applied to the A1R64 end of the divider, resulting in the A1R64, A1R63 junction becoming slightly positive. This causes the output of A1U6-6 to go positive. A1U5-6 going positive forward biases A1CR36, while A1U6-6 going positive forward biases A1CR37. Either condition develops a voltage across A1R77 that causes A1VR14 to conduct the gate on SCR A1Q6. Capacitor A1C28 and A1R76 hold A1VR14 from being biased into conduction by a random positive transient signal when the power supply is initially turned on. When A1Q6 conducts, the cable current output is shorted out through A1Q6 and A1R81. Crowbar switch A1Q6 remains in conduction until either the POWER CABLE switch is placed to OFF or the 115 v ac input is interrupted by the POWER SUPPLY switch being placed to OFF.

Section XVI. CABLE SYSTEM POWER DISTRIBUTION

2-57. General

This section contains a discussion of cable power distribution in a typical cable system that connects a near-end TD-976/G and a far-end TB-976/G. This section also contains discussions relating to AVOW insertion on and extraction from the cable system and for performing a cable system test to locate a faulty TB-982/G in the cable system. The discussions are based on the circuits shown in the typical cable system diagram in figure FO-15.

a. Cable System Configurations. The cable system contains the near-end TD-976/G, CX-11230/G cables, TC-982/G's (if required), and the far-end instrument, which may be another TD-976/G, a TD-1147/TSC, or an AN/GRC-144. The configuration depicted in figure FO-15 is a typical cable system that uses two TD-982/G's and a TD-976/G as the far-end instrument. The systems planning section in TM 11-7025-202-12 contains more detailed information on cable system configurations.

b. Cable Power.

(1) Each TD-976/G contains a cable power supply (part of power supply 21A12) that can produce a regulated 45-milliampere cable current to power the TD-982/G's when the cable system is longer than one-half mile. When the near-end TD-976/G is in a cable system with a TD-1147/TSC or an AN/GRC-144 as the far-end instrument, the TD-976/G supplies cable power for both the incoming and outgoing SG cables. Cable power is not required in short-run cable systems that do not contain one or more TD-982/G's. Cable systems can extend up to 5 miles, provided the TD-982/G's are installed in series with the cabling at half-mile intervals.

(2) When the near-end TD-976/G is in a cable system that has another TD-976/G as the far-end instrument, one or both TD-976/G's can supply the cable power. This situation is described in paragraph 2-59.

(3) The drive voltage in the cable power supply circuits that maintain the constant 45-milliampere cable current can increase to approximately 400 v dc under certain cable system configurations. As described in the power supply circuit descriptions in section XV, the cable power supply contains a crowbar circuit that shorts out the cable current when monitor circuits in the power supply detect an overcurrent or undercurrent condition.

c. TD-982/G Application.

(1) Each TD-982/G contains two identical printed circuit cards. Each card is called a restorer half. Each restorer half in a TD-982/G receives and restores the cable-attenuated and distorted ½-baud bipolar pulses (SGOUT1 or SGIN1) to full-amplitude and reshaped pulses. This operation ensures that the signals do not lose their intelligence in long-haul cable systems. The circuits in each restorer half are powered by the 45-milliampere cable current.

(2) Each restorer half contains a test resistor in series with the 45-milliampere cable current. The test resistor functions during a cable system test as described in paragraph 2-61. When the restorer half is processing data, the test resistor is effectively paralleled so that it does not appear as a resistive value in series with the cable current path. When the restorer half is faulty (not processing data) or when no bipolar pulses are being applied to the restorer half, the test resistor is not paralleled and appears as a fixed resistance in series with the cable current path.

2-59. Cable Power Distribution

(fig. FO-15)

a. General. When the near-end and far-end instruments are both TD-976/G's, there are three configurations by which cable power can be applied to the cable system:

(1) Near-end TD-976/G is supplying all the cable power in the cable system (both incoming and outgoing SG cables) (*b* below). This is also the power configuration that would be used when the far-end instrument is a TD-1147/TSC or an AN/GRC-144.

(2) Far-end TD-976/G is supplying all the cable power in the cable system (*c* below).

(3) Both TD-976/G's are supplying cable power. In this configuration, each TD-976/G powers its outgoing SG cable (*d* below).

b. Cable Power Distribution With Near-End TD-976/G Supplying Cable Power.

(1) In this configuration, POWER CABLE switch S8 on the near-end TD-976/G is placed to ON and the POWER CABLE switch on the far-end TD-976/G is

placed to OFF. As shown in figure FO-15, in the near-end TD-976/G, the 45 ma (−) current from the power supply is routed through 21A14J3-4 and 21A14P2-4 to ground. The 45 ma (−) current is then applied back through 21A14P2-12 to the POWER CABLE switch. The cable current is routed through contacts 6 and 5 of S8, R11, and VR1 on the front panel, the secondary of T2 on the card file, and the secondary of T1 on the SG D/R card to CABLE IN connector J28.

(2) The cable current through J28 is applied through the cabling and each TD-982/G in the cable system to CABLE OUT connector J27 and the far-end TD-976/G. At the far-end TD-976/G, the cable current is routed through J27, the primary of T3 on the SG D/R card, the primary of T1 on the card file, VR2, contacts 4 and 5 of POWER CABLE switch S8, R11, and VR1 on the front panel, the primary of T2 on the card file, and the primary of T1 on the SG D/R card to CABLE IN connector J28.

(3) The cable current through J28 is applied through the cabling and each TD-982/G in the cable system to CABLE OUT connector J27 on the near-end TD-976/G. The cable current is routed through J27, the primary of T3 on the SG D/R card, T1 on the card file, VR2 and contacts 3 and 2 of S8 on the front panel to the 45 ma (+) current input of the cable power supply. The cable current through VR1 and VR2 on the front panel develop the voltages that light POWER IN indicator DS 3 and POWER OUT indicator DS4 on the front panel of both TD-976/G's.

c. Cable Power Distribution With Far-End TD-976/G Supplying Cable Power. In this configuration, the POWER CABLE switch on the near-end TD-976/G is placed to OFF and the POWER CABLE switch on the far-end TD-976/G is placed to ON. The cable current path for this configuration is through the same basic components as those described in *b* above, with the following exceptions. The cable current path through the near-end TD-976/G is the same as the path for the far-end TD-976/G described in *b* above. The cable current path through the far-end TD-976/G is the same as the path for the near-end TD-976/G described in *b* above.

d. Cable Power Distribution With Both TD-976/G's Supplying Cable Power.

(1) In this configuration, the POWER CABLE switches on both the near-end and far-end TD-976/G's are each placed to ON. The 45 ma current (−) output of each power supply is connected through a common ground return path (21A14J3-4 to 21A14P2-4, which is connected to chassis ground). In turn, the chassis ground in each TD-976/G is connected by the shields in the cable system.

(2) In each TD-976/G, the cable current path is from ground, through 21A14P2-12, contacts 6 and 5 of POWER CABLE switch S8, R11, and VR1 on the front panel, T2 on the card file, and T1 on the SG D/R card to CABLE IN connector J28. The cable current is applied through J28, cabling, and each TD-982/G in the cable system to CABLE OUT connector J27 on the opposite TD-976/G. At the opposite TD-976/G, the cable current is applied through J27, T3 on the SG D/R card, T1 on the card file, VR2 and contacts 3 and 2 of the POWER CABLE switch on the front panel, and 21A14J3-6 to the 45 ma current (+) input of the cable power supply.

e. Cable Discharge Circuits.

(1) The cable discharge circuits are configured to quickly discharge the high-voltage capacitors in the TD-976/G and the capacitance of the cable system when cable power is turned off. The high-voltage capacitors, such as C50 and C55 on the SG D/R card and C1 on the card file, are charged by the drive voltage associated with the cable current that is applied through the TD-976/G in any of the cable power configurations. When the cable current (and drive voltage) is removed, the cable discharge circuits are energized and then discharge the capacitors and the cable system as described in (2) and (3) below.

(2) Both Q1 and Q2 in the cable discharge circuits are turned off when cable current is present and remain off until the cable current source is turned off. In all of the cable power configurations, the cable current through R11 produces a more positive voltage to the base of Q1 than is applied to the emitter of Q1. The positive voltage at the base of Q1 holds Q1 cut off. When Q1 is off, there is no current through R13 and R14 to produce a forward bias (+) voltage to turn on Q2. The voltage drop across CR11 also holds the emitter of Q2 more positive than the base of Q2 to ensure that the stage remains cut off until Q1 conducts. Arc suppressors C10 and C3 prevent transients from biasing Q1 and Q2 into conduction.

(3) When cable current is removed, the cable system starts to discharge through R11, R12, R15, R17, and R16. The negative voltage across R12 biases Q1 into conduction. When Q1 conducts, Q2 is also biased into conduction by the positive voltage developed across R14. When Q2 conducts, R16 and R17 are effectively bypassed to produce a more negative forward bias voltage that makes Q1 conduct heavier. Functionally, the cable discharge circuits discharge the capacitors in the cable system to less than 30 volts within 1 second after cable power is removed.

f. Indicator Alarm Test. The PWRLT input is applied to Q6 on the front panel when the ALARM TEST switch is pressed to initiate an alarm test. The high-level signal from the AD card biases Q6 into conduction. When Q6 conducts, relays K1 and K2 are energized to place +5 v dc and ground across POWER

OUT indicator DS4 and POWER IN indicator DS3. The two indicators remain lit until the ALARM RESET switch is released to remove the PWRLT input to Q6. When Q6 is conducting, the low output from the collector of Q6 is applied through CR22, which forces the output of the dc output monitor circuits to light the POWER DC indicator on the front panel.

2-60. AVOW Insertion On and Extraction from Cable System

(fig. FO-15)

a. The TD-976/G, TD-1147/TCS, and AN/GRC-144 have circuits that transmit and receive analog voice orderwire (AVOW) on the cable system. AVOW card 21A10 in the TD-976/G has transmit circuits that produce the transmit AVOW signals that are applied to the cable system, and receive circuits that process the receive AVOW signals from the cable system.

b. Transmit AVOW Circuits. Analog voice signals (TAVOW1) from the AVOW card are applied to the primary of transformer T1 on the card file. The signals are coupled through T1 and routed to the secondary winding of T3 on the SG D/R card, where the analog voice signals are superimposed on the SG bipolar output from the line drivers. The combined AVOW and SG signals are routed through the cable system as the SGOUT1 signals. The SGOUT1 signals are received by the far-end instrument as the SGIN1 signals. The AVOW signals are effectively routed around the SG circuits in each restorer half in the cable system. This permits the use of the AVOW circuits when there is no SG output from the TD-976/G or a restorer half in the cable system is faulty.

c. Receive AVOW Circuits. The SGIN1 signals from the cable system are applied to the primary of transformer T1 in the SG D/R card. The AVOW (analog) portion of the SGIN1 signals is routed from T1 to T2 on the card file and are coupled through T2 and applied to the receive AVOW circuits on the AVOW card as the RAVOW1 signals.

2-61. Cable System Test

(fig. FO-15)

a. General. The cable system test is performed to locate the faulty TD-982/G in the cable system that is not processing the bipolar pulses. Each TD-976/G contains the cable fault circuits necessary to perform a cable system test. When a TD-976/G is located at each end of the cable system, either unit can perform the cable system test and locate the faulty TD-982/G. As described below, the TD-976/G performing the test must supply all the cable current for the cable system. Also, the far-end instrument must loop the SG back to the TD-976/G performing the cable system test.

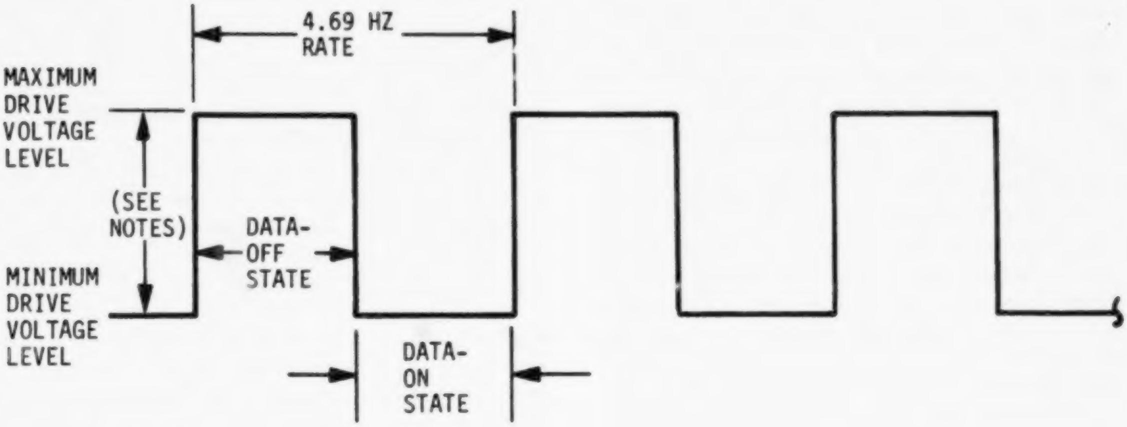
b. Cable System Test Concept.

(1) The TD-976/G that is performing the cable system test sends out bursts of SG pulses that are looped back at the far-end instrument and returned to the TD-976/G. When all restorer halves are functional during the time that data are applied, the test resistor in each restorer half is effectively bypassed and the overall resistance in the cable current path is minimum. During the time span that SG pulses are not being generated, the test resistor in each restorer is effectively in series with the cable current path. At this time, the overall resistance in the cable current path is maximum. When a restorer half is faulty and does not produce an SG output, any further restorer halves down link are held inactive, since they are not receiving any pulses from the faulty restorer half. Therefore, the test resistor in the restorer half that is malfunctioning and the following restorer halves that are inactive remain in series with the cable current path during the complete test period. For example, when restorer half No. 2 in the cable system shown in figure FO-15 is faulty, restorer halves No. 3 and No. 4 are held inactive. This condition effectively places the resistance of the three test resistors in series with the cable current path at all times.

(2) The TD-976/G performing the cable system test alternately sends out SG pulses for approximately 105 milliseconds (data-on state) and then inhibits the generation of SG for approximately 105 milliseconds (data-off state). During the data-off state, all the test resistors are placed in series with the cable current path. In turn, during the data-on state, the test resistors in the restorer halves passing data are bypassed to lower the total resistance of the test resistors in series with the cable current path. This condition of alternating the resistance in series with the cable current path affects the amplitude of the drive voltage for the constant current as described in (3) below.

(3) The cable power supply produces a drive voltage that varies in amplitude as necessary to maintain the 45-milliampere cable current. When the cable current path has maximum resistance placed in series with the cable current path (during data-off state), the drive voltage level is also maximum (more positive). In turn, when the cable current path has minimum resistance placed in series with the cable current path (during data-on state), the drive voltage level is at its minimum level (less positive.) Therefore, as the SG interrupter gates the output of the line drivers through the data-on and data-off states, the drive voltage changes abruptly as shown in figure 2-32. The change in the drive voltage levels between the data-on and data-off states forms the square wave signals shown in figure 2-32. These signals become the CABFLT signals that are applied to the cable fault circuits to determine which restorer half is faulty as described below.

c. Circuit Description.



NOTES:

1. CHANGE IN DRIVE VOLTAGE LEVELS BETWEEN DATA-ON AND DATA-OFF STATES IS DETERMINED BY NUMBER OF RESTORER HALVES THAT ARE PROCESSING DATA.
    A. WHEN ALL RESTORER HALVES ARE OPERATIONAL, THE VOLTAGE DIFFERENTIAL IS MAXIMUM.
    B. WHEN NO RESTORER HALVES ARE OPERATIONAL, THE VOLTAGE DIFFERENTIAL IS MINIMUM.
2. VOLTAGE DIFFERENTIAL DECREASES APPROXIMATELY 2.529 VOLTS FOR EACH RESTORER HALF THAT IS NOT OPERATIONAL.

EL5NG032

Figure 2-32. CABFLT signal waveform diagram.

(1) The POWER CABLE and CABLE TEST switches are placed to ON in the TD-976/G performing the cable system test. This action removes CFNRM—, allowing the SG interrupter on the SG D/R card to operate. This action also removes the ground from C2 to enable the input of the cable test clamp circuit on the SG D/R card.

(2) At the opposite end of the cable system, the TD-976/G has the POWER CABLE switch placed to OFF and the DIGITAL LOOP BACK switch placed to ON. When the far-end instrument is a TD-1147/TSC or an AN/GRC-144, there is no POWER CABLE switch, but either instrument does have the loopback function capability.

(3) In the following descriptions, it is assumed that the near-end TD-976/G is performing the cable system test. At this time, the SGOUT1 signals from the near-end TD-976/G are applied to the cable system

during the data-on state. The SGOUT1 signals are routed down the cable, looped through the far-end instrument, and applied back to the near-end TD-976/G as the incoming SGIN1 signals.

(4) The SG interrupter alternately forces the line drivers into the data-on and data-off states. During the data-off state, all the restorer halves in the cable system are inactive, causing all the test resistors in the restorer halves to be placed in series with the cable current path. This forces the cable power supply to produce a greater drive voltage to maintain the constant 45-milliampere cable current. During the data-on state, the SGOUT1 pulses are processed through the restorer halves until the pulses are applied to the faulty unit. At this time, the restorer halves that are processing data pulses have their test resistors bypassed to decrease the overall resistance in series with the cable current path. The decreased resistance in series with the cable current path causes the cable power supply to decrease the drive voltage to maintain the constant 45-milliampere cable current.

(5) The change in the drive voltage levels to respond to the alternating data-on and data-off states is coupled through R1 and C2 to form an ac square wave input to the cable test clamp circuit. The amplitude of the 4.69 Hz square wave applied through C2 is equal to the difference amplitude of the drive voltage maximum and minimum levels.

(6) The voltage drop across one test resistor is 2.529 volts. Therefore, there is a 2.529-volt decrease in the power voltage level for each restorer half that is processing data pulses during the data-on state. For example, when restorer half No. 4 in figure FO-15 is faulty, restorer halves No. 1, No. 2, and No. 3 process data during the data-on state. In the data-on state, the three test resistors in the three restorer halves are bypassed to cause a decrease of approximately 7.59 volts (3x2.529) in the drive voltage level. Therefore, the amplitude change of the signal level applied through C2 is approximately 7.59 volts ac.

(7) The square wave signals applied through C2 are clamped (referenced to ground) by the cable test clamp circuit. The signals routed through R43 on the SG D/R card are applied as positive-going CABFLT signals to the cable fault circuits on the AVOW card.

(8) Potentiometer R80 in the input of the cable fault circuits is a factory adjustment that is set so that the proper output signals are produced by the cable fault circuits for a given CABFLT signal input level. Based on the amplitude of the applied CABFLT signals, the cable fault circuits produce the appropriate FTLB1, FTLB2, FTLB4, FTLB8, and FTLB16 signals that are applied to the front panel to light the appropriate CABLE FAULT indicators. For example, when restorer half No. 2 is faulty, the cable fault circuits produce a high-level FTLB2 signal. At the front panel, the CABLE FAULT 2 indicator is lit. The CABLE FAULT DETECTION placard on the TD-976/G front cover shows that restorer No. 2 is the faulty unit.

Section XVII. ANALOG VOICE ORDERWIRE (AVOW) CARD 21A10

2-62. General

This section contains separate block diagram and detailed theory of operation discussions of the functional circuits on the AVOW card. There is one AVOW card (21A10) in the TD-976/G. The AVOW card is functionally divided into voice orderwire circuits (AVOW, ring generator, and DVOW) and cable fault circuits. The block diagram discussion in paragraph 2-63 is based on the voice orderwire circuits blocks diagram in figure 2-33 and the cable fault circuits block diagram in figure 2-34. The detailed theory of operation in paragraph 2-64 is based on the AVOW card schematic diagram in figure FO-16.

2-63. Block Diagram Discussion

a. General. The block diagram discussion is divided into four functional circuit descriptions as follows:

(1) The AVOW circuits (*b* below) interface the transmit and receive cable orderwire signals to the transmit and receive cable circuits on SG D/R card 21A9.

(2) The ring generator (*c* below) produces the 1600 Hz ring signal for the AVOW circuits and the DVOW circuits.

(3) The DVOW circuits (*d* below) interface the transmit and receive orderwire signals with the encoder and decoder on DVOW card 21A11.

(4) The cable fault circuits (*e* below) determine if the cable system is operational, and if it is not, identify the faulty TD-982/G pulse form restorer.

b. AVOW Circuits (fig. 2-33).

(1) The AVOW local microphone (MIC) switch and the AVOW local earphone switch are turned on when the LATL— signal from the front panel is applied through U34-9. The LATL— signal also resets the AVOW ring latch if it was in a set condition at the time the signal is applied. The LMIC signals from the local handset are routed through the AVOW local microphone switch and applied to the AVOW transmit amplifiers and the AVOW sidetone generator. The amplified signals from the AVOW transmit amplifiers are applied as TAVOW1 and TAVOW2 signals to the output orderwire transformer mounted on the card file. The analog signals applied to the AVOW sidetone generator are amplified and applied to the AVOW remote earphone switch and the AVOW local earphone switch. With LATL— applied, the AVOW local earphone switch is turned on and the sidetone signals are

applied as LEAR signals to the earphone of the local handset connected to the front panel.

(2) The AVOW remote microphone switch and the AVOW remote earphone switch are turned on when the RATL— signal from the RAU is applied through gate U32-8. The RATL— signal also resets the AVOW ring latch if it was in a set condition at the time the signal is applied. The PRS— signal, which is active during initial power turn-on, ensures that the ring latch is reset. The RMIC signals from the RAU are routed through the AVOW remote microphone switch and applied to the AVOW transmit amplifiers and the AVOW sidetone generator. The signals are processed through the amplifiers and generator as described in (1) above. The signals are routed through the AVOW remote earphone switch and applied to the RAU as REAR signals.

(3) When RATL— and PTT— signals are applied to gate U34-7, the AVOW external orderwire control panel microphone switch is turned on. The CMBUS signals (from an external orderwire control panel) are routed through the AVOW external orderwire control panel microphone switch and applied to the AVOW transmit amplifiers and the AVOW sidetone generator. The analog signals from the external source, via the RAU, are processed through the amplifiers and generator as described in (2) above.

(4) The incoming AVOW signals are decoupled from the cable system at the input orderwire transformer mounted on the card file. The decoupled analog signals are applied as RAVOW1 and RAVOW2 signals to the AVOW ring detector and the AVOW receiver amplifier. The analog signals are amplified through the AVOW receive amplifier and applied to the AVOW local and remote earphone switches. The signals are applied as LEAR signals to the local handset when LATL— is applied to the card. In turn, the signals are applied to the RAU as REAR signals when RATL— is applied to the card.

(5) When the incoming RAVOW1 and RAVOW2 signals contain the 1600 Hz ring signal, the AVOW ring detector produces a signal that causes the AVOW ring switch to produce a set signal to the AVOW ring latch. The switch is inhibited from producing a set signal during the time an outgoing ring signal is present by an inhibit signal that is applied to it from the ring timer. When a set signal is applied to the AVOW ring latch, the AVCAL— signal is produced and applied to the AD card until the latch is reset by RATL— or LATL—.

c. Ring Generator. The ring generator receives a 1.6 kHz input from the MO/C card to produce a 1600 Hz ring signal that is applied to the AVOW circuits or to produce a 1600 Hz signal that is applied as DVRNGS to the DVOW card. The ring generator produces the ring signal to the AVOW transmit amplifiers when AVRNG— is applied to the card. In turn, the generator produces DVRNGS when DVRNG— is applied to the card. The ring timer holds the ring generator active for approximately 250 milliseconds after AVRNG— or DVRNG— is removed from the card. The signal from the ring timer also serves as an inhibit input to the AVOW ring switch as described in *b*(5) above.

d. DVOW Circuits.

(1) The DVOW local microphone switch and the DVOW local earphone switch are turned on when the LDTL— signal from the front panel is applied through gate U34-12. This enables the LMIC signals applied to the card to be routed through the switch and applied as DVMIC signals to the DVOW card. The signals applied through the switch are also processed through the DVOW sidetone generator and applied through the DVOW local earphone switch as LEAR signals to the handset connected to the front panel. With LDTL— applied, the incoming analog DVEAR signals from the DVOW card are routed through the switch and applied as LEAR signals to the front panel.

(2) The DVOW remote microphone switch and DVOW remote earphone switch are turned on when the RDTL— signal from the RAU is applied through U22-6. This enables the RMIC signals applied to the card to be routed through the DVOW remote microphone switch and applied as the DVMIC signals to the DVOW card. The signals applied through the switch are also processed through the DVOW sidetone generator and applied through the DVOW remote earphone switch as REAR signals to the RAU. With RDTL— applied, the incoming analog DVEAR signals from the DVOW card are routed through the switch and applied as REAR signals to the RAU.

(3) The DVOW external orderwire control panel microphone switch is turned on when the RDTL— signal and PTT— signal are applied to gate U34-4. This enables the CMBUS signals applied to the card to be routed through the switch and applied as DVMIC signals to the DVOW card. Since RDTL— is applied, the CMBUS signals are processed through the DVOW card. Since RDTL— is applied, the CMBUS signals are processed through the DVOW sidetone generator and applied through the DVOW remote earphone switch as REAR signals to the RAU. The incoming DVEAR signals routed through the DVOW remote earphone switch are shared by the RAU and the external orderwire control panel.

e. Cable Fault Circuits. During a cable system test, the cable fault circuits detect which restorer in the cable system is faulty by measuring the amplitude of the CABFLT signals. As described below, the cable fault circuits translate the amplitude of the CABFLT signals into a dc reference voltage that determines which of the five fault light bit (FTLB) signals are generated from the circuits. Each of the five FTLB signals

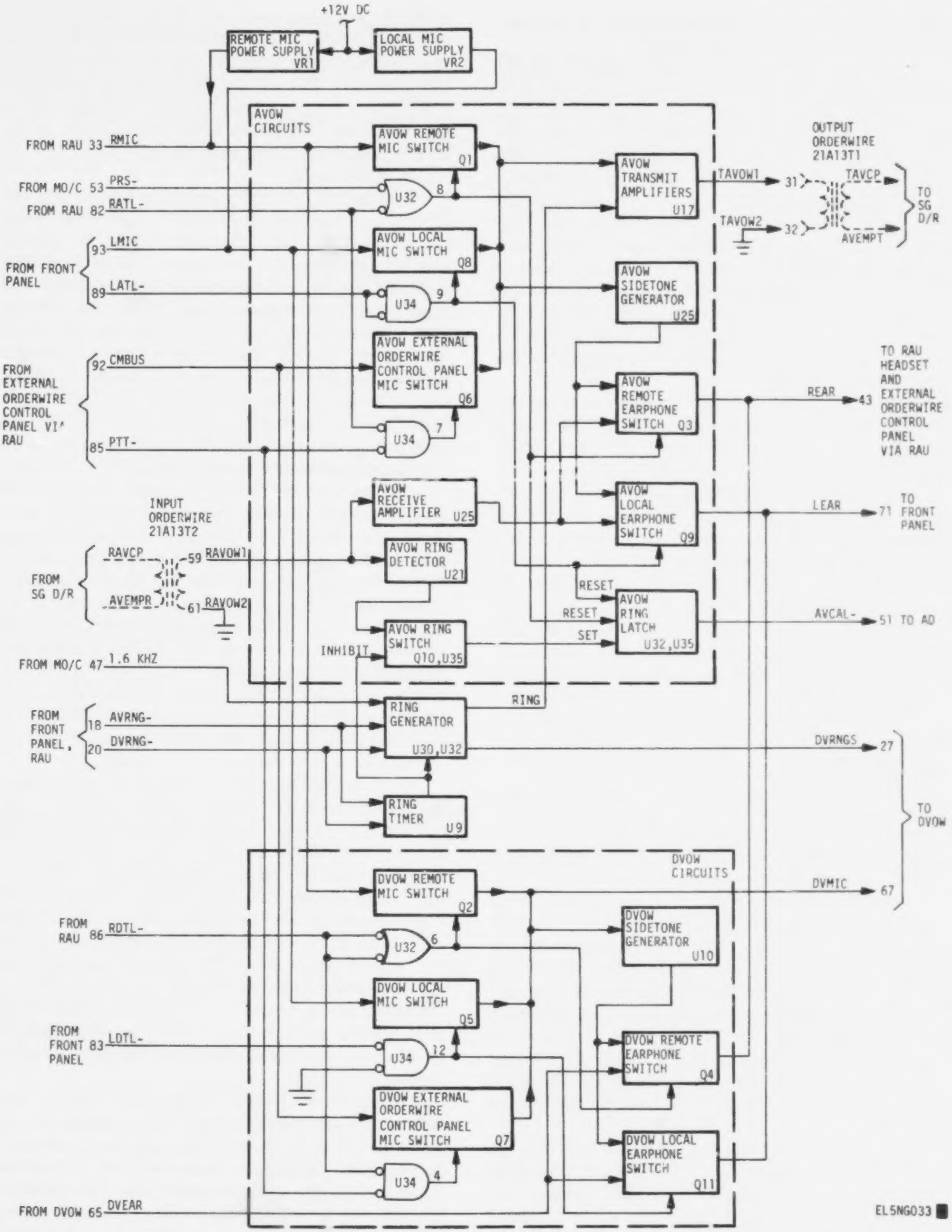

+12V DC
REMOTE MIC POWER SUPPLY VR1
LOCAL MIC POWER SUPPLY VR2
AVOW CIRCUITS
FROM RAU 33 RMIC
FROM MO/C 53 PRS-
FROM RAU 82 RATL-
FROM FRONT PANEL
93 LMIC
89 LATL-
FROM EXTERNAL ORDERWIRE CONTROL PANEL VIA RAU
92 CMBUS
85 PTT-
AVOW REMOTE MIC SWITCH Q1
U32
8
AVOW LOCAL MIC SWITCH Q8
U34
9
AVOW EXTERNAL ORDERWIRE CONTROL PANEL MIC SWITCH Q6
U34
7
AVOW TRANSMIT AMPLIFIERS U17
TAVOW1
TAVOW2
31
32
OUTPUT ORDERWIRE 21A13T1
TAVCP
AVEMPT
TO SG D/R
AVOW SIDETONE GENERATOR U25
AVOW REMOTE EARPHONE SWITCH Q3
REAR
43
TO RAU HEADSET AND EXTERNAL ORDERWIRE CONTROL PANEL VIA RAU
AVOW RECEIVE AMPLIFIER U25
AVOW LOCAL EARPHONE SWITCH Q9
LEAR
71 TO FRONT PANEL
INPUT ORDERWIRE 21A13T2
FROM SG D/R
RAVCP
59
RAVOW1
AVEMPR
61
RAVOW2
AVOW RING DETECTOR U21
RESET
RESET
SET
AVOW RING LATCH U32,U35
AVCAL-
51 TO AD
INHIBIT
AVOW RING SWITCH Q10,U35
FROM MO/C 47 1.6 KHZ
RING
RING GENERATOR U30,U32
FROM FRONT PANEL, RAU
18 AVRNG-
20 DVRNG-
DVRNGS
27
RING TIMER U9
TO DVOW
DVOW CIRCUITS
DVOW REMOTE MIC SWITCH Q2
DVMIC
67
FROM RAU 86 RDTL-
U32
6
DVOW SIDETONE GENERATOR U10
DVOW LOCAL MIC SWITCH Q5
FROM FRONT PANEL 83 LDTL-
U34
12
DVOW REMOTE EARPHONE SWITCH Q4
DVOW EXTERNAL ORDERWIRE CONTROL PANEL MIC SWITCH Q7
DVOW LOCAL EARPHONE SWITCH Q11
U34
4
FROM DVOW 65 DVEAR
EL5NG033

Figure 2-33. AVOW card 21A10 voice orderwire circuits, block diagram.

produced is configured to light one of the CABLE FAULT (1, 2, 4, 8, or 16) indicators on the front panel during a cable system test. The following concept and circuit discussions are based on the cable fault circuits block diagram in figure 2-34.

(1) *Concept discussion.* The comparator, control circuits, up/down counters, and digital-to-analog (D/A) converter operate in a closed-loop configuration under control of the constant dc reference voltage from the peak detector. During cable system test, the summed dc reference voltage and output voltage from the D/A converter will approach a null point where the summed voltage is equal to the threshold voltage applied to the comparator. The null point is defined as the point where the output of the comparator changes from a positive voltage to a negative voltage or vice versa. The output voltage from the D/A converter is a stair-step voltage whose value is representative of the count contained in the the up/down counters. In this circuit configuration, the output voltage does not maintain a constant null condition when it is a finite (constant) voltage level. However, the circuits do reach a stabilized condition when the output voltage settles down and alternates slightly above and below the desired voltage level where the null point should be. The dc reference voltage determines the D/A converter output voltage level that is required to reach the null point. The more positive the dc reference voltage becomes, the more negative (or less positive) the D/A converter output voltage must become to reach the null point. In turn, a higher count is required from the up/down counters to produce a less positive output voltage from the D/A converter. When the circuits reach a stabilized condition, the five most significant bits (MSB's) from the counters are constant outputs. These five bits determine which FTLB signals are produced from the cable fault drivers. As the output voltage from the D/A converter alternates around the null point, the counter up and down commands limit the changes in the up/down counter outputs to the three least significant bits (LSB's). These three bits do not affect the generation of the FTLB signals.

(2) *Circuit discussion.* When a cable system test is not being performed, CFNRM— holds the up/down counters in a preset condition that applies all logic 0's to the cable fault drivers. This prevents any FTLB signals from being produced when a cable system test is not being performed. ALRMT is applied to the cable fault drivers when the ALARM TEST switch on the front panel is pressed. The signal causes the five FTLB signals to be produced as long as the signal is applied to the card. Placing the CABLE TEST switch on the front panel to ON removes the CFNRM— signal and enables the up/down counters. At this time, the CABFLT signals applied to the card are sampled by the peak detector. The peak detector produces the dc reference voltage that is applied to the inverting input of the comparator. The output voltage from the D/A converter is also applied to the inverting input to produce a sum voltage level that is compared with the threshold level applied to the noninverting input of the comparator. The threshold level is set to produce a logic 1 at the A5 output of the up/down counters when the amplitude of the CABFLT signals is approximately zero. A 0-volt input indicates that none of the restorers in the cable system are passing data; therefore, restorer No. 1 is faulty. This configuration also sets up the condition whereby any dc reference voltage applied to the comparator results in a count higher than that required to produce the A5 output (actual count 8). For example, assume that a dc reference voltage is present and the D/A converter has all logic 0's applied from the up/down counters. The sum voltage at the comparator is positive with respect to the threshold voltage and a minus dc voltage is applied to the up/down control selector. This causes the selector to produce an up command to the timing and control logic. The logic, in turn, produces a count up signal that precedes each 3.2 kHz clock that is applied to the up/down counters. The increasing count from the counters produces a less positive output voltage from the D/A converter. This condition produces a less positive sum voltage to the comparator, and at the null point, the comparator output switches from a minus output to a positive output. The positive output results in the start of a count down function that drives the output voltage from the D/A converter more positive. As the circuits reach the stabilized condition, the comparator produces alternating outputs that result in limited up and down counts that only affect the three LSB's of the up/down counters. At this time, the five MSB's (A1 through A5) remain constant logic 1 or logic 0 outputs that are applied to inputs on the five cable fault drivers. Each logic 1 output from the A1 through A5 outputs becomes an FTLB signal to the front panel. The REF signal is a reference voltage from the power supply that maintains a constant relationship between the dc reference voltage and the D/A converter output voltage if the cable current were to vary above or below 45 milliamperes. For example, if the cable current were to increase, the amplitude of the CABFLT signals would be greater for a given fault condition. In turn, the REF signal level also increases to raise the gain factor of the D/A converter by an amount that maintains the proper relationship of the dc reference voltage to the D/A converter output voltage to produce a given null condition.

2-64. Theory of Operation

a. General. This paragraph describes the detailed operation of the circuits on AVOW card 21A10. The theory of operation is divided into the four functional

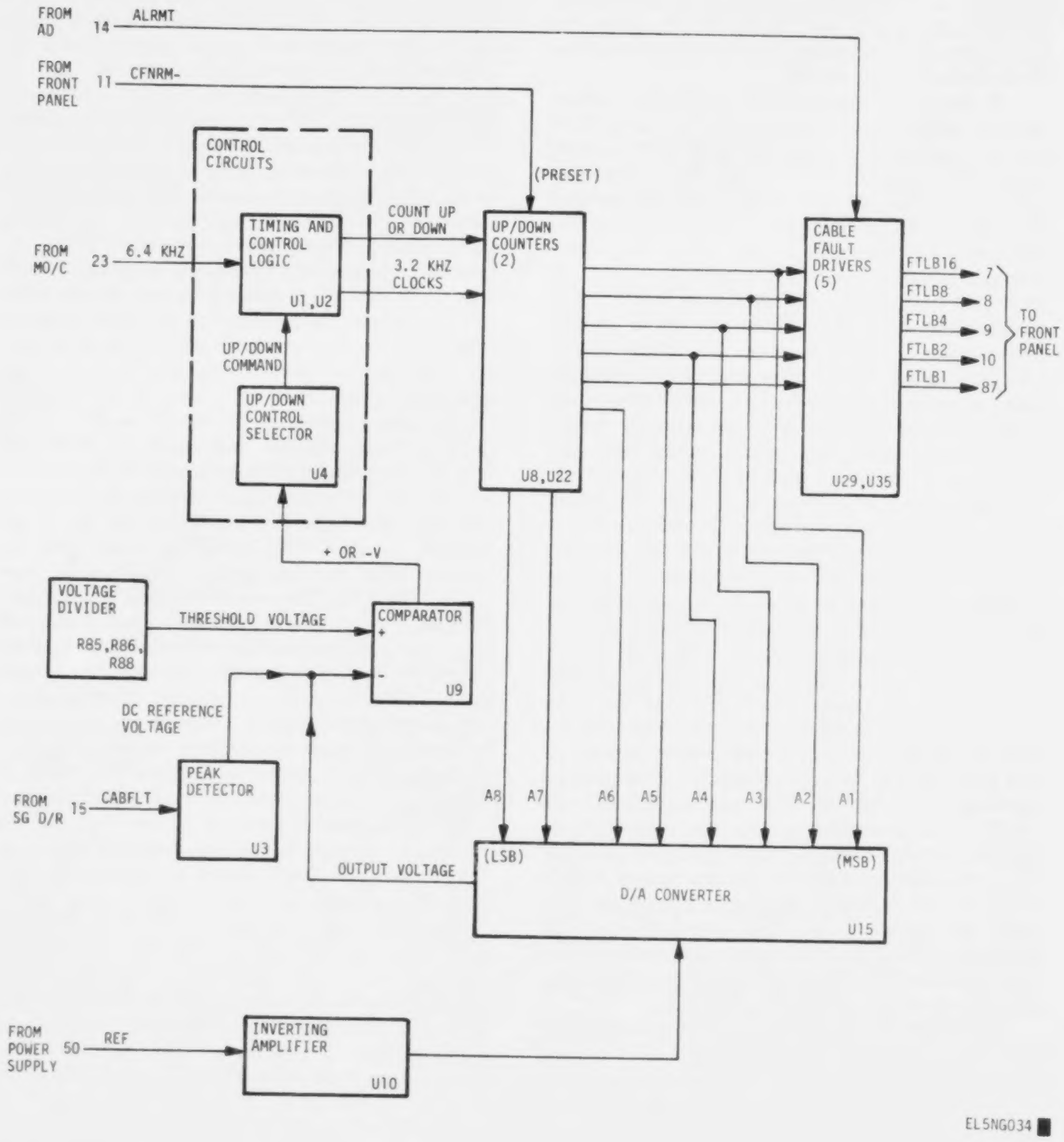

FROM AD
14
ALRMT
FROM FRONT PANEL
11
CFNRM-
CONTROL CIRCUITS
(PRESET)
TIMING AND CONTROL LOGIC
U1,U2
COUNT UP OR DOWN
3.2 KHZ CLOCKS
UP/DOWN COUNTERS (2)
U8,U22
CABLE FAULT DRIVERS (5)
U29,U35
FTLB16
FTLB8
FTLB4
FTLB2
FTLB1
7
8
9
10
87
TO FRONT PANEL
FROM MO/C
23
6.4 KHZ
UP/DOWN COMMAND
UP/DOWN CONTROL SELECTOR
U4
+ OR -V
VOLTAGE DIVIDER
R85,R86, R88
THRESHOLD VOLTAGE
COMPARATOR
+
-
U9
DC REFERENCE VOLTAGE
PEAK DETECTOR
U3
FROM SG D/R
15
CABFLT
OUTPUT VOLTAGE
A8
A7
A6
A5
A4
A3
A2
A1
(LSB)
(MSB)
D/A CONVERTER
U15
FROM POWER SUPPLY
50
REF
INVERTING AMPLIFIER
U10
EL5NG034

Figure 2-34. AVOW card 21A10 cable fault circuits, block diagram.

circuit descriptions established in the block diagram discussion, as listed below.

(1) AVOW circuits (*b* below).
(2) Ring generator (*c* below).
(3) DVOW circuits (*d* below).
(4) Cable fault circuits (*e* below).

NOTE

The sheet number references in *b* through *e* below refer to figure FO-16.

b. AVOW Circuits.

(1) The LATL— signal applied through card pin 89 (sheet 3) forces the output of U34-9 high to bias on

AVOW local microphone switch Q8 and AVOW local earphone switch Q9. LATL— is also applied to pin U35-1 as a reset input ((4) below). The analog LMIC signals applied through card pin 93 are routed through Q8 and applied to AVOW transmit amplifier U17-9 (sheet 2) and AVOW sidetone generator U25-9. The analog signals are amplified through U17-9 and U17-1 and are then routed as the TAVOW1 signal to transformer 21A13T1 on the card file. Potentiometer R18 is a factory adjustment that is set to produce a 3.88-volt (rms) signal at card pin 31 with a 1 kHz, 0.224-volt (rms) signal applied to card pin 33. When a call is initiated, the 1600 Hz ring signal from ring generator U30-11 (sheet 4) is applied through C44, R90, and R31 (sheet 2) to pin U17-7, where the signals are processed into the outgoing TAVOW1 signal. The analog signals processed through U25-9 are applied as the sidetone audio signals to AVOW remote earphone switch Q3 and AVOW local earphone switch Q9 (sheet 3). Since Q9 is biased on by the high output of U34-9, the signals applied to Q9 are routed through card pin 71 as the outgoing LEAR signals. The sidetone signals are routed through Q3 as REAR signals when RATL— is applied to the card as described in (2) below.

(2) The RATL— signal applied through card pin 82 (sheet 2) forces the output of gate U32-8 high to bias on AVOW remote microphone switch Q1 and AVOW remote earphone switch Q3. The high output of U32-8 is also applied to pin U35-15 (sheet 3) as a reset input ((4) below). The analog RMIC signals applied through card pin 33 (sheet 2) are routed through Q1 and applied to AVOW transmit amplifier U17-9 and AVOW sidetone generator U25-9. The signals are processed through these stages as described in (1) above to produce the TAVOW1 and REAR signals. The REAR signals are outputted from card pin 43 since Q3 is biased on. The power on reset signal (PRS—) applied to pin U32-9 produces a high reset signal to pin U35-15 (sheet 3) when power is initially turned on.

(3) When RATL— and PTT— (sheet 3) are applied to gate U34-7, AVOW external orderwire control panel microphone switch Q6 is biased on. This condition permits analog CMBUS signals to be routed through Q6 and applied to AVOW transmit amplifier U17-9 and AVOW sidetone generator U25-9 (sheet 2). The signals are processed through these stages as described in (2) above to produce TAVOW1 and REAR output signals.

(4) The analog RAVOW1 signals from the cable system are applied through card pin 59 (sheet 2) to AVOW receive amplifier U25-1 and AVOW ring detector U21-1 (sheet 3). The signals amplified through U25-1 are applied to switches Q3 and Q9 (sheet 3). The signals are routed through Q9 as the LEAR output when LATL— is applied to the card. The signals are routed through Q3 as the REAR output when RATL— is applied to the card. U21-1 (sheet 3) is a bandpass filter tuned to 1600 Hz. When the applied RAVOW1 input contains the 1600 Hz ring signal, U21-1 detects this condition, causing the output of U21-9 to go positive. This action forward biases CR1, which, in turn, causes Q10 to conduct, placing a low on pin U35-5. The input to pin U35-6 is normally low and is a high inhibit only when a transmit ring signal is being generated. The resulting high output from gate U35-7 drives the output of gate U35-9 low. When the inputs to pins U35-1 and U35-15 are low, the low input from U35-9 drives the output of gate U35-12 high. The high output from U35-12 is inverted by U32-11 to produce the low-level AVCAL— output. The high output from U35-12 is also applied to gate U35-9 to hold the circuit in a latched condition until either LATL— or RATL— is applied to the card. LATL— causes a high reset signal to pin U35-1. RATL— causes a high reset signal to pin U35-15. The latch circuit, consisting of U35-12 and U35-9, cannot be placed in a latched condition when either RATL— or LATL— is applied to the card (orderwire conversion being conducted).

c. *Ring Generator.*

(1) The AVRNG— signal applied through card pin 18 (sheet 4) sets latch U30-3, U30-6 so that one input to gate U30-11 is a high enable signal and one input to gate U30-8 is a low inhibit signal. AVRNG— also places a low on pin U9-3, resulting in a high output from U9-1. When AVRNG— is removed, C41 holds U9-1 high for approximately 250 milliseconds. While U9-1 is high, the applied 1.6 kHz signals are gated through gate U32-3 to the inputs of gates U30-11 and U30-8. Since pin U30-12 is high and pin U30-9 is low, the 1.6 kHz signals are gated through U30-11 to AVOW transmit amplifier U17-9 (*b*(1) above).

(2) The DVRNG—signal applied through card pin 20 (sheet 4) sets the latch so that one input to gate U30-11 is inhibited and one input to gate U30-8 is enabled. As described in (1) above, the 1600 Hz ring signals are applied to both gates. In this condition, the 1600 Hz ring signals are gated through U30-8 and outputted through card pin 27 as DVRNGS.

d. *DVOW Circuits.*

(1) The LDTL— signal applied through card pin 83 (sheet 3) forces the output of U34-12 high to bias on DVOW local microphone switch Q5 and DVOW local earphone switch Q11. The analog LMIC signals are routed through Q5 and outputted as DVMIC signals through card pin 67 to the encoder section of the DVOW card. The signals from Q5 are also applied to DVOW sidetone generator U10-9 (sheet 2). The amplified signals from U10-9 are applied to DVOW remote earphone switch Q4 and DVOW local earphone switch Q11 (sheet 3). Since Q11 is biased on by the LDTL—

input, the analog signals applied to Q11 are routed out through card pin 71 as LEAR signals. The sidetone signals are routed through Q4 when RDTL— is applied to the card as described in (2) below.

(2) The RDTL— signal applied through card pin 86 (sheet 2) forces the output of U32-6 high to bias on DVOW remote microphone switch Q2 and DVOW remote earphone switch Q4. The RMIC signals applied through card pin 33 are routed through Q2 and outputted as DVMIC to the DVOW card. The signals from Q2 are also processed through U10-9 and outputted through Q4 as REAR signals.

(3) When RDTL— and PTT— are applied to gate U34-4 (sheet 3), DVOW orderwire external control panel microphone switch Q7 is biased on. This condition permits analog CMBUS signals to be routed through Q7 and outputted as DVMIC signals through card pin 57 (sheet 2). The signals from Q7 are also processed through U10-9 (sheet 2) and outputted through Q4 as REAR signals.

(4) The incoming DVEAR signals are applied through card pin 65 (sheet 2) to DVOW remote and local earphone switches Q4 and Q11 (sheet 3). When RDTL— is applied to the card and Q4 is biased on, DVEAR signals are outputted through Q4 as REAR signals. The signals are outputted from Q11 as LEAR signals (sheet 3) when LDTL— is applied to the card.

e. Cable Fault Circuits.

(1) The CABFLT signal applied through card pin 15 (sheet 4) is routed through potentiometer R80 to peak detector U3-9. Potentiometer R80 is a factory adjustment that sets the upper level gain of U3-9. During the data off state of the CABFLT signal (fig. 2-32), the positive portion of the signal appears as a positive output at U3-9 and causes C43 and C54 to be charged through CR5. The amount that C43 and C54 are positively charged determines the dc voltage output from U3-1. The output from U3-1 is the dc reference voltage applied to pin 7 of comparator U9-9.

(2) The output voltage from D/A converter U15-4 (sheet 5) is also applied to U9-7 (sheet 4). The voltage from the junction of R85 and R88 is the threshold voltage applied to noninverting input pin U9-6. Potentiometer R86 is a factory adjustment that sets the output from U9-9 to produce a count of 8 (Q3 high) from up/down counter U8 with 0 volt at card pin 15 (no CABFLT signal applied). The high Q3 output (count of 8) from U8 (sheet 5) causes gate U35-4 to produce the FTLB1 signal to the front panel to indicate that restorer No. 1 is faulty. Therefore, whenever a restorer in the cable system, other than restorer No. 1, is faulty, the CABFLT signals produce a dc reference voltage that is more positive than the threshold voltage at pin U9-6, and a count higher than 8 is produced by the up/down counters.

(3) When up/down counters U8 and U22 contain all logic 0 outputs or a count that is lower than what the final count will be, the output voltage from U15-4 that is summed with the dc reference voltage at U9-7 (sheet 4) is more positive than the threshold voltage at pin U9-6. At this time, the output from U9-9 is negative, causing a negative bias to be developed at the junction of CR6 and R93. This causes U4-7 to go positive. The U4-7 output is routed through backplane jumper AVCT01 and U2-8 (sheet 5) to flip-flop U1-10, causing it to be reset. The low output from U1-10 directs up/down counters U8 and U22 to count up.

(4) When the output count from the up/down counters is too high, the sum of the output voltage from pin U15-4 (sheet 5) and the dc reference voltage at pin U9-7 (sheet 4) is less positive than the threshold voltage and causes the output voltage from U9-9 to go positive. This develops a positive bias voltage at the junction of CR7 and R93, causing U4-7 to produce a negative output. In turn, this causes flip-flop U1-10 (sheet 5) to be set and produce a high (count down) output to up/down counters U8 and U22. The output voltage from D/A converter U15-4 is a stair-step voltage that prevents a smooth linear sum voltage from being developed at U9-7. Therefore, the output voltage from U9-9 is always a specific negative or positive output that biases U4-7 to produce a count up (positive) or count down (negative) output, respectively.

(5) The 6.4 kHz clock signals are applied through U2-6 (sheet 5) to clock flip-flop U1-6. The 3.2 kHz clock pulses from U1-6 are gated through gate U2-11 to clock up/down count flip-flop U1-10. The complemented 3.2 kHz clock pulses from U1-7 are gated through gate U2-3 to clock up/down counter U8. Figure 2-35 shows the application of the count up and count down signals and 3.2 kHz clocks to the up/down counters.

(6) The output of U4-7 (sheet 4) is inverted by U2-8 (sheet 5) and applied to the J-K inputs of flip-flop U1-10. When the output of U2-8 goes low, the next 3.2 kHz clock from U2-11 resets the flip-flop, making pin U1-10 low, which directs up/down counters U8 and U22 to count up. Conversely, when the output of U2-8 goes high, the next 3.2 kHz clock sets the flip-flop, making pin U1-10 high, which directs up/down counters U8 and U22 to count down.

(7) Up/Down counters U8 and U22 are cascaded so that the ripple count (RC) output from pin U8-13 clocks U22 each time U8 contains a count of 15. The five MSB's from the counters (Q3 from U8 and Q0 through Q3 from U22) are applied to five gates. Each MSB output that is a logic 1 produces a low FTLB output signal from the appropriate gate.

(8) D/A converter U15 (sheet 5) produces its most positive output voltage (minimum current output)

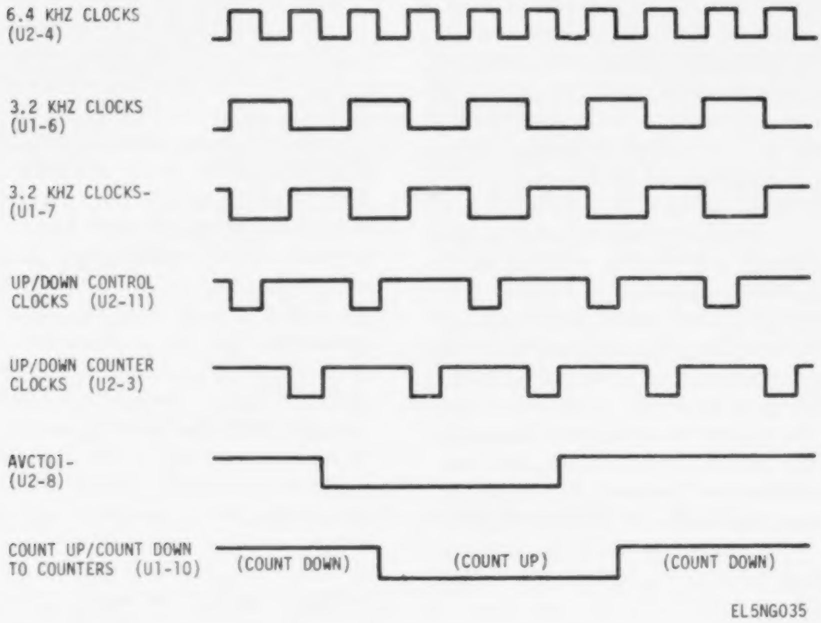


Figure 2-35. Up/Down count control waveform diagram.

when all logic 0's are applied from the up/down counters. In turn, the stage produces its least positive output voltage (maximum current output) when all logic 1's are applied to the inputs. Each time the output count from the up/down counters increases one count or decreases one count, the output voltage is stair-stepped up or down one increment of voltage. The output voltage from U15-4 is stepped up or down one increment at the 3.2 kHz rate at which the up/down counters are clocked. The U15-4 output is applied to U9-7 (sheet 4), where the voltage is summed with the dc reference voltage as described in (3) above.

(9) Inverting amplifier U10-1, which has a gain of unity, determines how much the output voltage level from U15-4 changes each time the count applied to the stage goes up or down one count. The inverting amplifier, in turn, is controlled by the REF signal applied from the power supply to pin U10-3. When the cable current is 45 milliamperes, the REF signal is −2.529 v dc. This is equal to the 2.529-volt change in the voltage level that occurs across one faulty restorer during a cable system test when the CABFLT signal switches from the data on to the data off state. As explained in the overall cable system test discussion (para 2-61), the 2.529 volts are the product of applying a cable current of 45 milliamperes through a 56.2-ohm dropping resistor. Therefore, the REF signal establishes a fixed relationship, or a constant voltage ratio, between the applied CABFLT signal voltage and the output voltage from U15. When the cable current increases or decreases from 45 milliamperes, the REF voltage level changes proportionately to maintain the established ratio between the dc reference voltage and the output voltage of U15. By maintaining a constant relationship between the two voltages, the sum voltage developed at the input to pin 7 of comparator U9-9 will remain the same and cause the correct outputs from the up/down counters when the cable current is above or below 45 milliamperes (within specified cable current tolerances).

Section XVIII. FRONT PANEL 21A14

2-65. General

This section contains discussions of the functional circuits on front panel 21A14. The front panel (fig. 2-7) centralizes TD-976/G operating indicators and controls (except those used for TTY orderwire control) for operator convenience. The POWER and VOICE O.W. controls and indicators are panel mounted, as are the ALARM horn and associated TEST and RESET switches. The indicators are tungsten lamps, except for the POWER AC indicator, which is a neon lamp. The ALARM, SIGNAL, and CABLE FAULT indicators (located in upper center portion of front panel) are light emitting diodes (LED's). The LED indicators are mounted on printed circuit card 21A14A1 attached behind a cutcut in the front panel. A plastic window with indicator names and numbers is attached in front of the panel cutout. Since functional block diagram level discussions of front panel circuits are already detailed in the overall block diagram discussion (section IV), they are not repeated in this section. References to front panel related discussions in section IV are provided in paragraph 2-66. The theory of operation in paragraph 2-67 is based on the front panel and circuit card schematic diagrams in figures FO-17 and FO-18, respectively.

2-66. Block Diagram Discussion References

a. Illustrations. Front panel control switches, indicators, fuses, and jacks are physically shown in figure 2-7. Their functional blocks or schematic symbols are shown on sheet 3 of figure FO-1, where they can be easily related to other TD-976/G functional circuits.

b. Indicators and Switches. The front panel ALARM indicators and their related circuits are discussed in paragraph 2-15*b*, *c*, and *f*. The CABLE SIGNAL and DUMMY SIGNAL indicators are discussed in paragraph 2-15*d* and *e*. The CABLE FAULT indicators and their related circuits are discussed in paragraph 2-63*e*. The VOICE O.W. indicators and switches are included in the discussions of typical voice orderwire call sequences (para 2-16*b* and *d*). The ALARM RESET and ALARM TEST switches, as well as the audible ALARM horn, are discussed in paragraph 2-15*h* and *i*. Refer to paragraph 2-54 for information on the POWER SUPPLY control switch and indicators. Refer to section XVI for information on the POWER CABLE switch and indicators and the CABLE TEST switch.

2-67. Theory of Operation
(figs. FO-17 and FO-18)

a. General. This paragraph describes the detailed operation of the functional circuits on the front panel and its circuit card 21A14A1. The theory of operation is divided into five functional indicator circuit descriptions, as listed below.

(1) ALARMS and SIGNAL indicators (*b* below).
(2) CABLE FAULT indicators (*c* below).
(3) VOICE O.W. CALL indicators (*d* below).
(4) POWER SUPPLY indicators (*e* below).
(5) CABLE POWER indicators (*f* below).

b. ALARMS and SIGNAL Indicators. Power supply 21A12 provides +5 v power through terminal E53 (fig. FO-18, sheet 1) to pullup resistors for all LED indicators on circuit card 21A14A1. AD card 21A1 provides on/off control for the INPUT ALARMS, OUTPUT ALARMS, FRAME ALARM, EQUIP ALARM, CABLE SIGNAL, and DUMMY SIGNAL indicators. The AD card switches its various output drivers on (high) and off (low) to light or turn off related indicators. Normally, all AD card drivers' outputs are low (collectors to ground). These grounds sink all pullup resistors' current through diodes, and the indicators remain turned off. When a fault is detected, the related alarm driver's output goes high (open collector), a pullup resistor's current is diverted through an LED indicator to ground (terminal E52), and the indicator lights. For example, detection of an input group 3 fault puts ICH3LPS high through front panel connector pin P1-11 (fig. FO-17, sheet 1) to circuit card 21A14A1 terminal E36 (fig. FO-18, sheet 1). The ICH3LPS high reverse biases diode CR5 and diverts all resistor R5 current through LED DS5 to ground terminal E52. The diverted current lights INPUT ALARMS 3 indicator DS5.

c. CABLE FAULT Indicators. Cable fault drivers on AVOW card 21A10 control CABLE FAULT 1, 2, 4, 8, and 16 indicators on circuit card 21A14A1 (fig. FO-18, sheet 1). Various combinations of lighted CABLE FAULT indicators denote cable fault detection codes that identify faulty pulse form restorers in the SG cable system.

d. VOICE O.W. CALL Indicators. AVCALS and DVCALS signals from AD card 21A1 control VOICE O.W. CALL indicators DS1 and DS2 (fig. FO-17, sheet 1) through transistors Q3 and Q4 (fig. FO-18, sheet 2). The AVCALS and DVCALS inputs are normally low. The lows hold their related transistors switched off and indicators turned off. Receipt of a voice orderwire call (digital voice for example) puts DVCALS high. Applied through front panel connector pin P1-31 (fig. FO-17, sheet 1) and circuit card 21A14A1 terminal E47 (fig. FO-18, sheet 2), the DVCALS high forward biases transistor Q4 fully on. Q4 switch-on grounds terminal E46 (fig. FO-17, sheet 1) and lights indicator DS2. E44 is the +5 v connection terminal for DS2. Typical voice orderwire call sequences are described in paragraph 2-16*b* and *d*.

e. POWER SUPPLY Indicators.

(1) POWER DC indicator DS5 (fig. FO-17, sheet 1) remains lit while all power supply 21A12 dc voltage outputs are within operating limits. Under this condition, the power supply dc output monitor circuit provides a dc indicator enable low through front panel connector pin J3-7 (fig. FO-17, sheet 2) to circuit card 21A14A1 terminal E3 (fig. FO-18, sheet 2). The low forward biases transistor Q5 fully on, grounds terminal E2 (fig. FO-17, sheet 1), and lights POWER DC indicator DS5. If a power supply +5 v, +12 v, −12 v, or −4.4 v output fails, a dc indicator enable high switches Q5 off and turns off indicator DS5.

(2) POWER AC indicator DS6 (fig. FO-17, sheet 2) lights while POWER SUPPLY switch S9 is placed to ON. In ON position, S9 applies the 115 v ac input from front panel connector pins P2-A1 (ACHOT) and P2-A2 (ACNEUT) through fuses F2 and F1 to DS6. The applied ac voltage lights DS6.

f. POWER IN and POWER OUT Indicators. POWER IN and POWER OUT indicators DS3 and DS4 (fig. FO-17, sheet 1) light while cable power is applied. The detailed operation of front panel POWER CABLE switch S8 and related indicator and cable discharge circuits on circuit card 21A14A1 is described in paragraph 2-59. Relays K1 and K2 (fig. FO-18, sheet 2) remain deenergized, except for testing indicators DS3 and DS4. Pressing ALARM TEST switch S4 (fig. FO-17, sheet 1) puts internal alarm test (INAT) high (+12 v) to AD card 21A1, and the card returns a cable power lamp test (PWRLT) high through P1-45 (fig. FO-17, sheet 1) to terminal E7 (fig. FO-18, sheet 2). The PWRLT high forward biases transistor Q6 fully on, grounds relay coil terminals K1-9 and K2-9, and energizes both relays. Relay K1 contact closures connect +5 v (K1-3 to K1-2 and E9) and ground (K1-7 to K1-8 and E11) across POWER IN indicator DS3, causing the indicator to light. Relay K2 contact closures connect −5 v (K2-3 to K2-2 and E8) and ground (K2-7 to K2-8 and E6) across POWER OUT indicator DS4, causing the indicator to light.

Section XIX. REMOTE ACCESS UNIT (RAU) 21A15

2-68. General

This section contains discussions of the functional circuits in RAU 21A15 and their related circuits within the TD-976/G. The RAU duplicates orderwire controls, all call indications, and most of the alarm indications provided on the TD-976/G front panel. The RAU also provides the only input and output access for the digital data orderwire (TTY) circuits in the TD-976/G. The RAU can be left attached to the TD-976/G or remoted by two interface cables to a console in a communications shelter. Since functional block level discussions of all RAU circuits are already detailed in the overall block diagram discussion (section IV), they are not repeated in this section. Reference to RAU related discussions in section IV are provided in paragraph 2-69. The detailed theory of operation in paragraph 2-70 is based on the RAU schematic diagram in figure FO-19.

2-69. Block Diagram Discussion References

a. Illustrations. The RAU indicators, control, switches, and jacks are physically shown in figure 2-8. Their functional blocks or schematic symbols are interspersed on the TD-976/G overall block diagram (fig. FO-1), where they can be easily related to other TD-976/G functional circuits.

b. Indicators and Switches. The INPUT ALARMS, OUTPUT ALARMS, FRAME ALARM, EQUIP ALARM, CABLE SIGNAL, and DUMMY SIGNAL indicators and their related circuits are discussed in paragraph 2-15*b* through *g*. The discussions are keyed to RAU indicator blocks shown on sheet 3 of figure FO-1. Operation of the VO ORDW indicators and switches and the TTY indicator and switches is included in the discussions of typical orderwire call sequences (para 2-16*b* through *d*). Conditions under which the various RAU indicators are lit and the operation of AD card 21A1 circuits that light the indicators are discussed in paragraph 2-51.

2-70. Theory of Operation

(fig. FO-19)

a. General. This paragraph describes the detailed operation of the functional circuits in RAU 21A15 and their relationships to interfaced circuits in the TD-976/G. The theory of operation is divided into four general functional circuit descriptions, as listed below.

(1) Indicators and control switch (*b* below).
(2) Orderwire switches (*c* below).
(3) Interface connections (*d* below).
(4) TTY orderwire input/output circuits (*e* below).

NOTE

The sheet number references in *b* through *e* below refer to figure FO-19.

b. Indicators and Control Switch. AD card 21A1 provides on/of control for the RAU's 23 light emitting diode (LED) indicators. The AD card switches its various alarm and orderwire call signal drivers on (high) and off (low) to light or turn off related indicators. The RAU gets its LED indicator operating voltage from an external source.

(1) LAMP switch S1 (sheet 2) provides for manual switching control of 24 v dc to enable (ON position),

inhibit (OFF position), or test (momentary TEST position) the RAU indicators. When placed to ON, S1 routes input pin A1J2-5 24 v dc through pins S1-2 and S1-3 to parallel resistors R24, R25, and R26. These resistors drop the applied +24 v to about +12 v at 1-kilohm pullup resistors for VD ORDW CALL indicators and 3.9-kilohm resistors for the remaining indicators. Normally, all AD card alarm driver outputs are low (collectors to ground). These grounds sink all pullup resistor current through diodes, and the indicators stay turned off. When a fault occurs or an orderwire call is received, the related alarm or call driver's output goes high (open collector), the pullup resistor's current is diverted through an LED indicator, and the indicator lights. Receipt of a digital data (TTY) call, for example, causes the AD card's DDCALS output to go high to the cathode of diode CR21. The high reverse biases CR1, diverts R21 current through TTY CALL indicator DS1 to dc ground, and lights DS1.

(2) The LAMP switch OFF position disconnects +24 v power from all RAU indicator circuits. This position is used to keep all indicators turned off when the RAU is remoted from its TD-976/G and the TD-976/G is turned off.

(3) Momentarily placing LAMP switch S1 to TEST applies power (S1-2 to S1-1) to all indicator circuits and puts the external alarm test (EXAT) output high (S1-5 to S1-4). The EXAT high switches on all AD card alarm drivers (open collectors) (para 2-52*k*) and causes all RAU indicators to light.

c. Orderwire Switches (sheet 2).

(1) VO ORDW SYSTEM switch S5 provides ring-talk/listen control for digital voice orderwire (DVOW) calls. A typical DVOW call sequence is described in paragraph 2-16*b*.

(2) VO ORDW CABLE switch S4 provides ring-talk/listen control for analog voice orderwire (AVOW) calls. A typical AVOW call sequence is described in paragraph 2-16*d*.

(3) TTY switches S2 and S3 provide receive-ready and send-ring control signaling, respectively, for digital data (TTY) orderwire (DDOW) calls. A typical DDOW call sequence is described in paragraph 2-16*c*.

d. Interface Connections.

(1) A multiconductor cable interconnects RAU circuit card connector A1J1 (sheets 1 and 2) with the TD-976/G. The A1J1 lines convey input and output alarm signals, dc ground, chassis ground, external control panel signals, DGTL VO XMT jack J4 and DGTL VO RCV jack J5 signals (sheet 1), and orderwire call control signals (sheet 2). J4 and J5 have 620-ohm resistors that automatically provide 600-ohm loads across tip and ring contacts when transmission line plugs are not inserted.

(2) Another cable interconnects RAU circuit card connector A1J2 to an external orderwire control panel. The A1J2 lines (sheet 1) convey external 24 v dc power to RAU indicator circuits (*b* above), remote handset microphone (RMIC) and earphone (REAR) signals, as well as a common dc ground. Three other lines (sheet 1) convey A1J1 signals that are applied directly to A1J2.

(3) DGTL DATA XMT jack J1 and DGTL DATA RCV jack J2 on the RAU (sheet 2) provide for plug-in connection of TTY orderwire transmission cables. TTY access to a TD-976/G can be achieved only through J1 and J2.

e. TTY Orderwire Input/Output Circuits. The RAU has jumper selectable circuits for interfacing 75-baud (Baudot coded) and 1200-baud (ASCII coded) teletype input and output signals. Jumpers P1, P2, P3, and P4 (sheet 2) configure the interfacing circuits for directly routing 1200-baud signals from DGTL DATA XMT jack J1 to DDOW encoder card 21A3, and from the card to DGTL DATA RCV jack jack J2 ((2) below). Jumpers P2, P3, and P4 configure the interfacing circuits for routing 74-baud signals through optical couplers Q1 and Q4 (sheet 2). Q1 and Q4 isolate the high-level (130 v) 75-baud signals that would otherwise damage the DDOW encoder card's logic circuits.

(1) For 75-baud operation, jumpers across P2, P3, and P4 pins A and B place optical couplers Q1 and Q4 in the receive and transmit circuits. Each optical coupler has an infrared light emitting diode (IRLED) and a photodetector. The IRLED radiates infrared energy (light) when dc current flows through it. The photodetector is similar to an ordinary NPN transistor, except that infrared light impinging on the PN junction controls the response.

(*a*) Q1 optically couples DDOW decoder card 21A8's digital data 75-baud output (D750) to a level converter that provides current loop closures across the tip and ring contacts of DGTL DATA RCV jack J1. A D750 low (mark) closes an electron current path from switched-on transsistor Q1 on card 21A8 (para 2-40*d*(1)(c)) through Q1's IRLED (sheet 2) and current limiting resistor R27 to the external 24 v dc source. Infrared light from the IRLED switches on Q1's photodetector and forward biases current loop switch Q3 fully on to close the receive output current loop. Transistors Q2 and Q5, zener diode VR1, and resistors R28 and R29 make up a reference voltage circuit. Q2 and Q5 are wired as a Darlington pair (amplifier) whereby Q2 retrieves most of Q5's emitter/base leakage current and adds it to the common base output. R28 drops the +130 v line voltage to about +20 v; VR1 regulates the +20 v down to about +12 v and holds Q2 switched on. The Q2 emitter voltage, in turn, controls Q5 to hold its emitter and optical coupler pin Q1-3 at about +12 v. Each Q1 switch-on (to provide a current flow (mark) output) connects the Q5 emitter level to the base of Q3. Q3 saturation provides a direct-short current path from J2-1 (ring) through jumper P4-A and -B, Q3 emitter to collector, and back out through jumper P3-B and -A to J2-4 (tip). Current flow in the receive output loop represents a data mark (derived from an SG data logic 0). Conversely, a D750 high blocks current flow through Q1's IRLED, and its related photodetector switches off (causing Q3 to switch off) for no current in the receive output loop (data space derived from an SG data logic 1).

(*b*) Q4 optically couples J1 transmit input loop current signals to DDOW encoder card 21A3. Figure 2-36 is a simplified schematic diagram of related 75-baud transmit circuits in the RAU and on the DDOW encoder card. Current flow in the loop represents a data mark and ultimately produces an SG data logic 0. For a mark, electron current flows from J1-1 (ring) through Q4's IRLED, diode CR25, and jumper P2-B and -A to J1-4 (tip). Resistor R31 across Q4's IRLED and CR25 sets the IRLED's sensitivity by setting current flow through it. IRLED current flow switches Q4's photodetector fully on and grounds its emitter (DDI—) input to the collector (D75I) output. Q4 switch-on puts pin UI7—1 (on DDOW encoder card) low (to DDI—ground on the card). U17 responds to a D75I low with a pin U17-8 high, which goes low through inverter U16-4 (logic 0 for insertion in SG data). Conversely, the absence of current in the transmit input loop (data space) switches Q4 off and opens the collector D75I output line. Opening the line lets DDOW encoder card's resistor R7 raise pin U17-1 high. Assuming the RAU's TTY switch S3 is placed to SEND and the DDOW encoder card's rate select switch jumper P2 is positioned across J2 and J3, U17 pins -12 and -13 are also high. A D75I high inverts through U17-8 and restores to a U16-4 high (logic 1 for insertion in SG data).

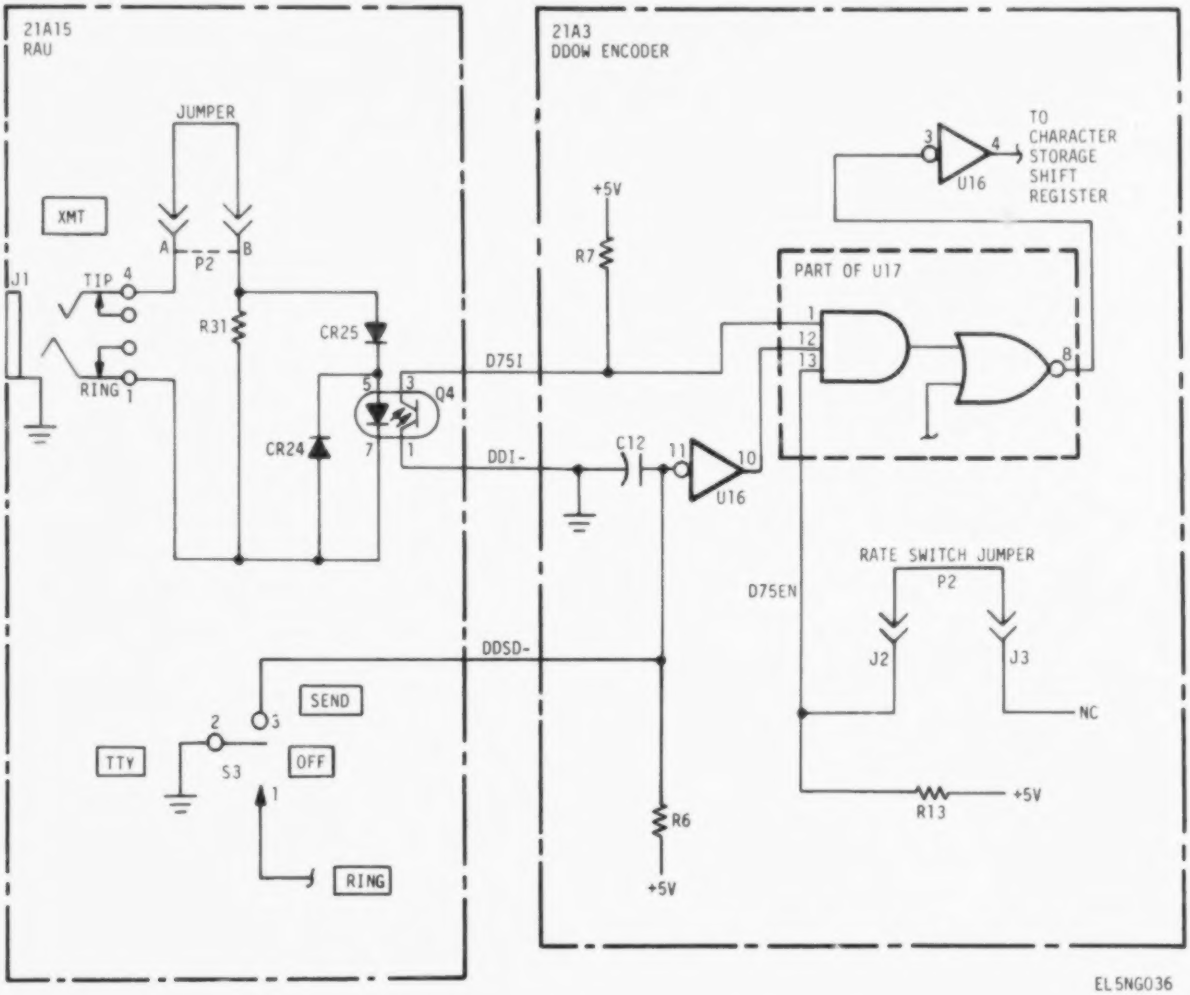

21A15
RAU
JUMPER
XMT
A
B
P2
J1
TIP 4
RING 1
R31
CR25
CR24
5
3
Q4
7
1
D75I
DDI-
DDSD-
SEND
2
3
TTY
S3
OFF
1
RING
21A3
DDOW ENCODER
+5V
R7
3
4
U16
TO
CHARACTER
STORAGE
SHIFT
REGISTER
PART OF U17
1
12
13
8
C12
11
10
U16
RATE SWITCH JUMPER
P2
D75EN
J2
J3
NC
R13
+5V
R6
+5V
EL5NG036

Figure 2-36. TTY data 75-baud interface circuit, simplified schematic diagram.

(2) Jumpers P2-A and -C and P1-A and -C directly connect J1-4 (tip) and J1-1 (ring) 1200-baud signals (sheet 2) to the DDOW encoder card. These low-level (± 6 v) signals are applied across a two-resistor (R20, R21) input voltage divider on the DDOW encoder card. Forward current (mark) through the voltage divider produces a positive voltage at the divider's junction; reverse current (space) produces a negative voltage. The positive and negative voltage levels control a comparator circuit that converts them to TTL compatible levels. The level conversion process is described in paragraph 2-37*b*. Jumpers P4-C and -A and P3-C and -A directly connect DDOW decoder card 21A8's D120 and D120— outputs to J2-1 (ring) and J2-4 (tip). A 1200-baud output level converter (U26, para 2-39*d*(2)(*b*)) on the DDOW decoder card converts TTL logic 0's and 1's to +6 v (mark) and −6 v (space) levels, respectively.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

WARNINGS

High voltage that can cause DEATH or serious injury is present in the TD-976/G.

- The 115-volt ac primary power is always applied to TB1 in the card file and to S9 on the front panel when the power cable is connected between the ac power source and the TD-976/G. Always disconnect the power cable when working in the TD-976/G.
- Cable drive power of 400 volts dc with a constant current of 45 milliamperes may be present in the equipment when the POWER IN and/or POWER OUT indicator is lit. The high voltage can be generated within the unit or the voltage may be applied from another TD-976/G that is connected to the unit being serviced. Ensure that both the POWER IN and POWER OUT indicators are out before working on the equipment.
- Wait at least 15 seconds after cable power is removed from the TD-976/G to ensure that high-voltage capacitors in the unit are discharged.

Section I. GENERAL

3-1. Introduction

This chapter contains visual inspections, tests, troubleshooting, and maintenance procedures authorized for use by maintenance personnel at the direct support maintenance level. Complete repair of the TD-976/G is authorized at the direct support level except for repair of the 11 plug-in circuit card types and the power supply. Repair of a TD-976/G that has confirmed faulty plug-in circuit cards or a faulty power supply is accomplished by replacement of those items. Power supply repair is accomplished by general support maintenance personnel in accordance with the instructions in chapter 4. Repair of plug-in circuit cards is accomplished by depot level maintenance.

3-2. Maintenance Concept

a. Maintenance Techniques. The TD-976/G contains a mixture of solid-state digital logic and analog circuits. Personnel performing troubleshooting and maintenance on the TD-976/G should be familiar with general maintenance and troubleshooting techniques (continuity checks and signal tracing) involving solid-state integrated circuit equipment. Personnel should also have an understanding of the TD-976/G theory of operation as explained in chapter 2. Under normal conditions, isolation and replacement of a faulty plug-in circuit card, power supply, RAU, front panel fuse, or front panel POWER AC indicator will have been performed by organizational maintenance personnel as instructed in TM 11-7025-202-12.

b. Use of Continuity Checks and Signal Tracing Aids.

(1) The detailed schematic diagrams and wiring information in this manual will assist maintenance personnel in performing continuity checks and signal tracing within the TD-976/G. A card extender is available as a troubleshooting aid. Access to the input and output pins and the circuit test points on a plug-in circuit card is provided when the card is installed in the card extender in the TD-976/G.

(2) To aid maintenance personnel in performing signal tracing or continuity checks, the signal names identified in the theory of operation are listed on each input and output pin on the schematic diagrams and in the wire run lists. The signal names are listed and defined in table 1-2. The schematic diagrams are foldout illustrations in the rear of the manual. The wire run lists and supporting wire run information are in section XI. Refer to the list of illustrations for the specific wiring diagrams and schematics contained in this manual.

c. Performance Testing.

(1) Each TD-976/G received from a user will be performance tested as instructed in section III. Each test table in section III checks the operation of one functional group of circuits that perform a specific operation in the TD-976/G. The tests in section III are used as receiving tests to confirm that the unit is faulty and to localize the fault to a functional level. When the fault is narrowed to a functional level, a troubleshooting reference to one of the troubleshooting tables in section IV is provided. After the defective item is located and repaired or replaced, the tests in section III are used as the performance standard test to ensure

that the repaired unit is operational and ready to be returned to the user or to stock.

(2) When a RAU is received from a user for repair, the test and troubleshooting procedures in section VI are used to test and locate the faulty component or wiring. After the unit is repaired, the test procedures in section VI are repeated as the performance standard test to ensure that the RAU is operational and ready to be returned to the user or to stock.

d. Troubleshooting. Each of the troubleshooting tables in section IV is configured to support one of the test procedure tables. The troubleshooting tables contain an "Abnormal indication" column that has one or more entries for each of the normal indications listed in the test procedures. Each abnormal indication in the troubleshooting tables references the step in the associated test procedures where the indication was obtained. This feature produces a quick and direct transition from testing to troubleshooting when a malfunction is detected. The test equipment used in the test procedures are used in the associated troubleshooting procedures.

e. Repair. A faulty power supply or plug-in card detected in the troubleshooting procedures is not repaired at the direct support maintenance level. The plug-in circuit cards are repaired at the depot facility. Power supply repair is performed by the assigned general support maintenance facility. Other faulty conditions detected during the visual inspection or when performing the troubleshooting procedures are repaired by direct support maintenance. The repair procedures for direct support maintenance are in sections VII through X.

3-3. Use of Extender Card

The extender card can be used with each of the plug-in circuit cards mounted in the card file. The extender card extends a plug-in circuit card to allow access to the circuits and the input and output pins of the card. The extender card is not keyed and can be installed in any of the card file slots. Similarly, any of the plug-in circuit cards can be installed in the extender card. Therefore, when installing a plug-in circuit card in the extender card, ensure that the reference designator of the plug-in circuit card matches the reference designator of the card file slot into which the extender card is installed. Perform the procedures in *a* through *e* below to extend a plug-in circuit card.

WARNING

High voltage that can cause death or serious injury may be present on SG D/R card 21A9. Cable drive voltage of up to 400 volts dc with a constant current of 45 milliamperes may be present when the POWER IN and/or POWER OUT indicators on the front panel are lit. Ensure that both the POWER IN and POWER OUT indicators are out before removing SG D/R card 21A9 from the card file.

a. On front panel, ensure that POWER CABLE and POWER SUPPLY switches are off.

b. Ensure that both the POWER IN and POWER OUT indicators are out.

c. Remove plug-in circuit card to be extended from card file.

d. Install extender card in card file and then install plug-in circuit card in extender card. Ensure that both extender card and plug-in circuit card are fully seated.

e. Set POWER SUPPLY and POWER CABLE switches to the positions they were in prior to performing *a* above.

Section II. TOOLS AND TEST EQUIPMENT

3-4. Introduction

This section contains a list of the tools and test equipment authorized for use in performance of direct support maintenance on the TD-976/G. The use of these tools and test equipment is authorized in the maintenance allocation chart in TM 11-7025-202-12.

3-5. Tools and Test Equipment

The tools and test equipment required for maintenance of the TD-976/G are listed in tables 3-1 and 3-2. Table 3-1 contains a list of the test equipment required to perform the direct support test and troubleshooting procedures. Table 3-2 contains a list of the tools used in the maintenance procedures at the direct support level. The following information is listed in each of the tables.

a. Tools or Test Equipment Column. This column lists the official name or the functional name of the tool or test equipment.

b. Military Designation/Manufacturer's Part No. Column. This column lists the manufacturer's part number (followed by the manufacturer's name in parentheses) when the military designation is not assigned or available.

c. NSN or FSCM Column. This column lists the National stock number or the Federal supply code for the manufacturer when the National stock number is not assigned or available. This information is defined and listed in the RPSTL (TM 11-7025-202-34P).

d. Use Column. This column lists a brief application description and paragraph references where the item is used in the procedures.

Table 3-1. Direct Support Test Equipment List

Test equipment	Military designation/manufacturer's part No.	NSN or FSCM	Use
Audio level meter.	TA-885/U	6625-00-255-1083	Test and troubleshooting (para 3-12, 3-13, 3-20, 3-21).
Digital counter.	AN/USM-207A	6625-00-044-3228	Test and troubleshooting (para 3-11, 3-15, 3-25).
Digital multimeter (DMM).	3490A (Hewlett Packard)	6625-01-010-9255	Test and troubleshooting (para 3-9, 3-12, 3-17, 3-20, 3-27).
Digital 4-wire cable set, containing:	70730086-009 (Martin Marietta)	04939 (FSCM)	Test and troubleshooting (both cables) (para 3-13, 3-15), 3-21, 3-23, 3-27).
Cable assembly.	70730085-009		
Cable assembly.	70730085-019		
Extender card.	SM-D-941960 (Martin Marietta)	04939 (FSCM)	Troubleshooting (para 3-10, 3-18.
Handset breakout box.	70730060-009 (Martin Marietta)	04939 (FSCM)	Test and troubleshooting (para 3-12, 3-13, 3-20, 3-21).
Oscilloscope.	OS-261/U	6625-00-127-0079	Test and troubleshooting (para 3-9, 3-11, 3-15, 3-17, 3-19, 3-23, 3-27).
Pattern generator.	SG-1054/G	6625-00-137-7738	Test and troubleshooting (para 3-15, 3-23, 3-27).
PCM loop cable set, containing:	70730081-009 (Martin Marietta)	04939 (FSCM)	Test and troubleshooting:
8 cable assemblies.	70730080-009		(para 3-11, 3-19).
2 cable assemblies.	70730080-019		(para 3-11, 3-12, 3-19, 3-20).
Power supply.	PP-3135/U	6625-00-635-7991	Test and troubleshooting (para 3-15, 3-23, 3-27).
Power supply.	PP-3940A	6130-00-460-2148	Test and troubleshooting (para 3-10, 3-12, 3-13, 3-15, 3-18, 3-20, 3-21, 3-23, 3-27).
Radio frequency cable assembly.	CG-2437/TCC-10FT	5995-00-916-2252	Test and troubleshooting (para 3-11, 3-19).
Radio frequency cable assembly.	CG-2438/TCC-10FT	5995-00-913-0510	Test and troubleshooting (para 3-11, 3-19).
RAU breakout box.	70730020-009 (Martin Marietta)	04939 (FSCM)	Troubleshooting (para 3-27).
RAU feedthru box.	70730000-009 (Martin Marietta)	04939 (FSCM)	Test and troubleshooting (para 3-10, 3-12, 3-15, 3-18, 3-20, 3-21, 3-23).
Resistor, 6800-ohm ± 5-percent, 5-watt (2 required).	None		Test and troubleshooting (para 3-15, 3-23, 3-27).
Signal generator.	SG-970/U	6625-00-145-1193	Test and troubleshooting (para 3-12, 3-13, 3-20, 3-21).

Table 3-1. Direct Support Test Equipment List—Continued

Test equipment	Military designation/manufacturer's part No.	NSN or FSCM	Use
Special electrical cable assembly.	CX-4559/U4-6	5995-00-985-7772	Test and troubleshooting (para 3-9 through 3-15 and 3-17 through 3-23).
TD-976/G breakout box.	70730070-009 (Martin Marietta)	04939 (FSCM)	Test and troubleshooting (para 3-9, 3-11, 3-12, 3-14, 3-17, 3-19, 3-20, 3-22).

Table 3-2. Direct Support Tools List

Tool	Military designation/manufacturer's part No.	NSN or FSCM	Use
Bench top repair center.	PRC-150A (Pace)	3439-00-445-5965	Circuit card and wire repair (para 3-29, 3-33, 3-39, 3-46).
Locking insert tools consisting of:	----	----	Case locking insert replacement (para 3-35).
Extraction tool.	1227-06 (Heli-Coil)	5120-00-245-9539	For 8-32 inserts.
Extraction tool.	1227-6 (Heli-Coil)	5120-00-723-6833	For 1/4-28 inserts.
Insertion tool.	7551-2 (Heli-Coil)	5120-00-237-4669	For 8-32 inserts.
Insertion tool.	7552-4 (Heli-Coil)	5120-00-710-7435	For 1/4-28 inserts.
Tang breakoff tool.	3695-2 (Heli-Coil)	5120-00-776-9519	For 8-32 inserts.
Tang breakoff tool.	3695-4 (Heli-Coil)	5120-00-793-1077	For 1/4-28 inserts.
Connector repair tool kit, containing:	70730090-009 (Martin Marietta)	04939 (FSCM)	
Bushing insertion tool.	600-0107-000 (Teradyne)	31413 (FSCM)	Backplane connector repair (para 3-42).
Certi-crimp.	90289-1 (Amp)	5120-00-124-5429	Backplane connector repair (para 3-43).
Crimp tool.	M22520/1-01	81349 (FSCM)	Connector panel repair (para 3-44).
Crimp tool.	M22520/2-01	5120-00-042-7076	Front panel connector repair (para 3-33).
Crimp turret.	M22520/1-02	81349 (FSCM)	Connector panel repair (para 3-44).
Crimp turret.	M22520/2-08	81349 (FSCM)	Front panel connector repair (para 3-33).
Cut/strip tool.	515654 (Gardner Denver)	24047 (FSCM)	Backplane wire repair (para 3-41).
Extraction tool.	CET-C6B (ITT Cannon)	5120-00-963-7661	Front panel connector repair (para 3-33).
Extraction tool.	MS24256R20	81349 (FSCM)	Connector panel repair (para 3-44).
Extraction tool.	600-0001-000 (Teradyne)	31413 (FSCM)	Backplane connector repair (para 3-42).
Extraction tool.	91084-1 (Amp)	5120-00-126-3205	Backplane connector repair (para 3-43).
Insertion tool.	MS24256A20	81349 (FSCM)	Connector panel connector repair (para 3-44).
Insertion tool.	600-0004-000 (Teradyne)	5120-00-320-4056	Backplane connector repair (para 3-42).
Insertion tool blade.	600-0005-000 (Teradyne)	31413 (FSCM)	Backplane connector repair (para 3-42).
Insertion tool.	600-0007-000 (Teradyne)	31413 (FSCM)	Not used.

Table 3-2. Direct Support Tools List

Tool	Military designation/manufacturer's part No.	NSN or FSCM	Use
Installation/ removal tool, consisting of:	MS18278-1	5120-00-230-3770	
Installation tool.	ATC 1081 (Astro Tool)	29247 (FSCM)	Not used.
Removal tool.	ATC 2076 (Astro Tool)	29247 (FSCM)	Front panel connector repair (para 3-33).
Unwrapping tool.	511203 (Gardner Denver)	24047 (FSCM)	Backplane wire repair (para 3-41).
Wire wrapping tool.	2736AA8 (Gardner Denver)	5130-01-018-2900	Backplane wire repair (para 3-41).
Wrapping bit.	508748 (Gardner Denver)	5120-01-018-2902	Backplane wire repair (para 3-41).
Wrapping sleeve.	507100 (Gardner Denver)	5130-00-459-4485	Backplane wire repair (para 3-41).
Electrical equipment tool kit.	TK-105/G or TK-100/G	5180-00-610-8177 5180-00-605-0079	Common tools for assembly and disassembly.

Section III. TD-976/G INSPECTION AND PERFORMANCE TEST PROCEDURES

3-6. Introduction

This section contains the visual inspection and the performance test procedures for the TD-976/G. The visual inspection procedures are performed on each TD-976/G received for repair by direct support maintenance. The performance test procedures are performed as a receiving test on each TD-976/G received. The performance test procedures are also performed as the performance standards on each repaired TD-976/G to ensure that the unit is ready to be returned to the user or to stock.

a. Visual Inspection Procedures. The visual inspection procedures in paragraph 3-8 are to be performed on each TD-976/G received by direct support maintenance. These procedures consist of a visual inspection of the TD-976/G for missing items or damaged components that should be repaired before energizing the unit and performing the electrical performance tests.

b. Performance Test Procedures. The performance test procedures are dynamic electrical tests that check out the electrical circuits in the TD-976/G. Paragraphs 3-9 through 3-15 contain seven different test procedures. Each of the seven tests checks the operation of one functional group of circuits as described in (1) through (7) below. The test procedures are performed on each received TD-976/G in the sequence listed below until a faulty condition is detected. When a faulty condition is detected in one of the test procedures, a specific troubleshooting procedure in section IV is referenced for isolating the fault. After the faulty condition is identified and repaired, the test procedures will be performed as the performance standards. The performance standards are met when all the test procedures are performed with no faulty indications. At this time, the TD-976/G can be returned to stock or to a user.

(1) *Power Supply Output Test* (para 3-9). This test checks the four dc output voltages and the regulated cable current output of the power supply.

(2) *Alarm and Indicator Lamp Test* (para 3-10). This test checks the visual indicators and audible alarm on the front panel, the visual indicators on the RAU, and light emitting diodes (LED's) on the edges of five of the plug-in circuit cards.

(3) *Data Transfer Test* (para 3-11). This test checks the TD-976/G data multiplexing, demultiplexing and synchronization circuits.

(4) *AVOW Test* (para 3-12). This test checks the AVOW receive and transmit circuits in the TD-976/G and an attached RAU.

(5) *DVOW Test* (para 3-13). This test checks the DVOW receive and transmit circuits in the TD-976/G and an attached RAU.

(6) *Cable Fault Detection Test* (para 3-14). This test checks the cable fault detection circuits in the TD-976/G.

(7) *DDOW Test* (para 3-15). This test checks the DDOW receive and transmit circuits in the TD-976/G and an attached RAU.

c. Test Table Usage. The test procedures in paragraphs 3-9 through 3-15 are presented in test tables. Each test contains three columns as described in (1) through (3) below.

(1) *Step Column.* This column lists the step se-

quence in which the procedures must be performed. As a receiving test, the sequential steps are performed until a faulty condition is detected. When the procedures are used as the performance standards to check a repaired TD-976/G, all the steps must be performed without any abnormal indications occurring.

(2) *Procedure Column*. This column contains the detailed instructions for setting controls on the equipment, for making test equipment connections, and other pertinent actions necessary to obtain the required test conditions.

(3) *Normal Indication Column*. This column describes the normal indication required for each test step. The indication may be a voltage measurement, a waveform displayed on an oscilloscope, or the status (lit or out) of equipment indicators. When a abnormal indication is obtained for a given step, the appropriate troubleshooting procedures in section IV will be performed to isolate the malfunction. When all the tests have normal indications, the TD-976/G is not faulty and can be returned to stock or to a user.

d. Test Techniques. The following general conditions should be considered when performing the test procedures.

(1) All the switches and indicators on the equipments involved in a given test procedures may not be used. The setting of individual switches in a test is not critical until the switch is called out for a specific setting in the procedures.

(2) When a switch is set in a test, do not change the switch position unless directed to do so in a later step. A switch set to a wrong position could cause an erroneous indication in a given test condition.

(3) Check the status of each indicator when directed to do so in the test procedures. Ignore the status of the indicators that are not identified in the test procedures.

(4) Perform the test procedures in the sequence presented in the tables in paragraphs 3-9 through 3-15. Performing the tests in the proper sequence will minimize the troubleshooting effort when an abnormal indication is obtained. The systematic troubleshooting procedures are based on the assumption that the test procedures that occur before a malfunction is detected have been successfully performed. Therefore, certain circuits associated with a given malfunction that were known to have been checked as part of a preceding test may not be considered as the probable malfunction in a following troubleshooting action.

(5) Each test in paragraphs 3-9 through 3-15 contains the test setup procedures necessary to perform the associated test procedures. This allows the user to repair a fault detected in a given test procedure and then repeat that specific test procedure without repeating all the preceding test procedures to confirm that the faulty condition is corrected. This repair check does not replace the requirement to repeat all the tests as the final performance standards to determine if the unit is serviceable.

(6) Audio level meter TA-885/U is used in the AVOW and DVOW tests. This meter measures audio output signal levels in dBm. When the INPUT switch on the audio level meter is set to the TMS BRDG position, the meter has a high input impedance to the test points being measured. Setting the FUNCTION switch to 600 BAL automatically scales the meter to a 600-ohm dBm scale. When the INPUT switch is set to the TMS TERM position and the FUNCTION switch is set to 600 BAL, the meter provides a 600-ohm load to the test points being measured. In the "Normal indication" column of the test procedures tables, the equivalent rms voltage level for each of the dBm indications is listed in parentheses. This permits the user, if necessary, to substitute a high input impedance ac voltmeter for the audio level meter in the tests. When using an ac voltmeter in the procedures where the INPUT switch on the audio level meter is set to the TMS TERM position and the FUNCTION switch is set to 600 BAL, a 600-ohm load resistor must be placed across the test points being measured. This action is noted in the parentheses after the rms indication by the statement "(into 600 ohms)."

3-7. Tools and Test Equipment Required for TD-976/G Inspections and Tests

The tools and test equipment required for inspecting and testing the TD-976/G are listed in table 3-3. The following information is in the table.

a. Tools and Test Equipment Column. This column lists the functional name of the tools and test equipments.

b. Qty Column. This column lists the maximum number of items used in any one of the inspection or test procedures.

c. NSN or Part No. Column. This column contains the NSN of the tools and test equipments. When the NSN is not assigned or available, the manufacturer's part number is listed. When the part number is listed, the manufacture's name is also listed in parentheses.

d. Use Column. This column lists the paragraph numbers where the items are used.

Table 3-3. Tools and Test Equipment Required for TD-976/G Visual Inspections and Test Procedures

Tools and test equipment	Qty	NSN or Part No.	Use (para No.)
Audio level meter TA-885/U.	1	6625-00-255-1083	3-12, 3-13.
Digital counter AN/USM-207A.	1	6625-00-044-3228	3-11.
Digital multimeter (DMM).	1	6625-01-010-9255	3-9, 3-12.
Digital 4-wire cable set, containing:	1	70730086-009 (Martin Marietta)	
Cable assembly.	1	70730085-009	3-13, 3-15.
Cable assembly.	1	70730085-019	3-13, 3-15.
Electronic equipment tool kit TK-105/G.	1	5180-00-610-8177	3-8.
Extender card.	1	SM-D-941960	3-10.
Handset breakout box.	1	70730060-009 (Martin Marietta)	3-12, 3-13.
Oscilloscope OS-261/U.	1	6625-00-127-0079	3-9, 3-11, 3-15.
Pattern generator SG-1054/G.	1	6625-00-137-7738	3-15.
PCM loop cable set, containing:	1	70730081-009 (Martin Marietta)	
Cable asembly.	8	70730080-009	3-11.
Cable assembly.	2	70730080-019	3-11, 3-12.
Power supply PP-3135/U.	1	6625-00-635-7991	3-15.
Power supply PP-3940A.	1	6130-00-460-2148	3-10, 3-12, 3-13, 3-15.
Radio frequency cable assembly CG-2437/TCC-10FT.	1	5995-00-916-2252	3-11.
Radio frequency cable assembly CG-2438/TCC-10FT.	1	5995-00-913-0510	3-11.
RAU feedthru box.	1	70730000-009 (Martin Marietta)	3-10, 3-12, 3-13, 3-15
Resistor, 6800-ohm ± 5 percent, 5-watt.	2	None	3-15.
Signal generator SG-970/U.	1	6625-00-145-1193	3-12, 3-13.
Special electrical cable assembly CX-4559/U4-6.	1	5995-00-985-7772	3-9 through 3-15.
TD-976/G breakout box.	1	70730070-009 (Martin Marietta)	3-9, 3-11, 3-12, 3-14.

3-8. Visual Inspection Procedures

a. Inspection Requirements. The visual inspection procedures in table 3-4 will be performed on each TD-976/G received by direct support maintenance. The visual inspections will be done before performing the electrical tests on the TD-976/G.

b. Repair Requirements. When the power supply or one of the plug-in circuit cards is damaged, the item will be replaced with a known good power supply or plug-in circuit card. Maintenance procedures for repair of a faulty RAU, front cover, front panel, case, and card file are in section VII through IX. Faulty conditions that could effect electrical performance of the equipment should be repaired prior to performing the test procedures in paragraphs 3-9 through 3-15.

c. Inspection Procedures. Perform the inspection procedures listed in table 3-4. Unless the TD-976/G has excessive physical damage that warrants further disassembly, only remove the items for inspection as directed in the procedures.

NOTE

The front cover, top cover, and RAU are removed from the TD-976/G during the inspection procedures. It is necessary that these items remain removed during the performance test procedures. Reinstall front cover, top cover, and RAU after completing the final performance standards.

Table 3-4. TD-976/G Inspection Procedures

Step	Procedure	Inspection
1	Loosen 12 captive screws on top cover; then lift cover from case. Inspect top cover.	*a.* Physical damage to cover. *b.* Missing or damaged captive screws.
2	Loosen 16 captive screws on front cover; then remove cover from case. Inspect front cover.	*a.* Physcial damage to cover components. *b.* Missing or damaged captive screws.
3	Loosen four captive screws on RAU mounted in top of case; then remove RAU from case. Inspect RAU.	*a.* Missing or damaged captive screws. *b.* Mechanical operation of switches. *c.* Missing or damaged boots on switches.

Table 3-4. TD-976/G Inspection Procedures—Continued

Step	Procedure	Inspection
		d. Damaged pins or presence of foreign material in open connectors. *e.* Physical damage to indicators or case.
4	Perform external inspection of front panel.	*a.* Mechanical operation of switches. *b.* Missing or damaged boots on switches. *c.* Physical damage to indicators or panel. *d.* Proper fuses installed in both 3A SLO BLO fuseholders. *e.* Damaged pins or presence of foreign material in open connector.
5	Perform internal inspection of front panel, looking through top of TD-976/G case.	*a.* Broken, frayed, or loose wires on panel and cable harness. *b.* Damaged components on front panel circuit card. *c.* Three connectors on wiring harness are not damaged and are properly connected.
6	Inspect front-interior of card file (without removing plug-in cards or card file from case).	Physical damage.
7	Inspect rear-exterior of card file (this is connector panel on rear of card file).	*a.* Damaged or loose connectors. *b.* Missing or damaged connector covers. *c.* Damaged pins or foreign material in connectors. *d.* Missing, blown, or damaged caps on lightning arresters E1 and E2. *e.* Physcial damage to panel.
8	Inspect plug-in circuit cards. (Remove each card, inspect associated card slides and electrical connector in card file, inspect card, and then carefully reseat card in proper slot in card file.)	*a.* Card slides in card file damaged. *b.* Foreign material or damaged pins in electrical connector in card file. *c.* Heat damaged components on card. *d.* Physcially damaged components. *e.* Damaged printed wiring surfaces on card. *f.* Presence of foreign material on card. *g.* Damaged connector pins on card.
9	Inspect power supply (without removing it from case.)	*a.* Power supply properly installed. *b.* Damaged power supply.
10	Inspect case.	*a.* Missing or damaged handles. *b.* Physical damage. *c.* Damaged electronic shielding gaskets mounted on case under top cover and front cover locations.

3-9. Power Supply Output Test

a. General. This paragraph contains the procedures for testing a power supply while installed in a TD-976/G. A power supply removed from a TD-976/G will be tested as instructed in chapter 4. Subparagraph *b* below contains a brief functional description of the power supply output test.

b. Functional Test Description. The power supply output test checks the outputs of a power supply while it is installed in a TD-976/G. The dc outputs (+5, +12, −12, and −4.4 v dc) are electrically loaded by the TD-976/G and checked for correct voltage levels and that ripple voltages are within limits. The cable current (45 ma) output is checked under nominal minimum and maximum loads supplied by the TD-976/G breakout box. Additionally, operation of the undercurrent crowbar associated with the 45 ma cable current output is checked.

c. Test Equipment Required. Table 3-5 lists the test equipment required to perform the power supply output test.

d. Test Procedures. Perform the procedures in table 3-6 to test a power supply while installed in a TD-976/G. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-17.

Table 3-5. Test Equipment Required for Power Supply Output Test

Test equipment	Qty	NSN or part No.
Cable assembly CX-4559/U4-6.	1	5995-00-985-7772
Digital multiplexer (DMM).	1	6625-01-010-9255
Oscilloscope OS-261/U.	1	6625-00-127-0079
TD-976/G breakout box (Martin Marietta).	1	70730070-009

Table 3-6. Power Supply Output Test

Step	Procedure	Normal indication
	INITIAL SETUP	
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to OFF. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF.	
2	On TD-976/G breakout box, set switches as follows: MODE SELECT to LOAD. LOAD SELECT to MIN. CABLE to ON.	
3	Connect test setup as shown in figure 3-1.	
	DC VOLTAGE CHECK	
4	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	POWER AC and POWER DC indicators light.
5	Sequentially connect DMM to following card file power test points and measure dc levels.	
	+ lead *− lead*	
	+5V GND	+4.75 to +5.25 v dc.
	+12V GND	+11.43 to +13.97 v dc.
	−12V GND	−11.43 to −13.97 v dc.
	−4.4V GND	−3.96 to −4.84 v dc.
6	Sequentially connect oscilloscope between following card file power test points and GND test point, and measure ripple voltages.	
	+5V	Less than 250 mv peak-to-peak.
	+12V	Less than 250 mv peak-to-peak.
	−12V	Less than 250 mv peak-to-peak.
	−4.4V	Less than 400 mv peak-to-peak.
	CABLE CURRENT OUTPUT CHECK	
7	On TD-976/G, set POWER CABLE switch to ON.	*a.* POWER IN and POWER OUT indicators on TD-976/G light. *b.* STATUS CABLE POWER indicator on TD-976/G breakout box lights.
8	Connect DMM to CABLE CURRENT + and − test points on TD-976/G breakout box.	DMM indicates 4.5 ± 0.25 v dc.
9	On TD-976/G breakout box, set LOAD SELECT switch to MAX.	DMM indicates 4.5 ± 0.25 v dc.
10	On TD-976/G breakout box, cycle CABLE switch to OFF and then back to ON.	*a.* POWER IN and POWER OUT indicators on TD-976/G go out and remain out. *b.* STATUS CABLE POWER indicator on breakout box goes out and remains out. *c.* DMM indicates 0.0 ± 0.1 v dc.
11	On TD-976/G, cycle POWER CABLE switch to OFF and then back to ON.	*a.* POWER IN and POWER OUT indicators on TD-976/G light. *b.* STATUS CABLE POWER indicator on breakout box lights. *c.* DMM indicates 4.5 ± 0.25 v dc.
12	On TD-976/G, set POWER CABLE and POWER SUPPLY switches to OFF.	
13	Disconnect test setup and proceed to alarm and indicator lamp test (para 3-10).	

3-10. Alarm and Indicator Lamp Test

a. General. This paragraph contains the procedures for testing the indicator lamps on the front panel, the RAU, and on the edges of five plug-in circuit cards and the audible ALARM horn. Subparagraph *b* below contains a brief functional description of the alarm and indicator lamp test.

b. Functional Test Description. The alarm and indicator lamp test checks that the various indicator lamps on the front panel, the RAU, and the edges of five plug-in circuit cards are capable of lighting. The test also checks operation of the front panel audible ALARM horn. The RAU feedthru box functions to interconnect the RAU to the TD-976/G. Each signal line

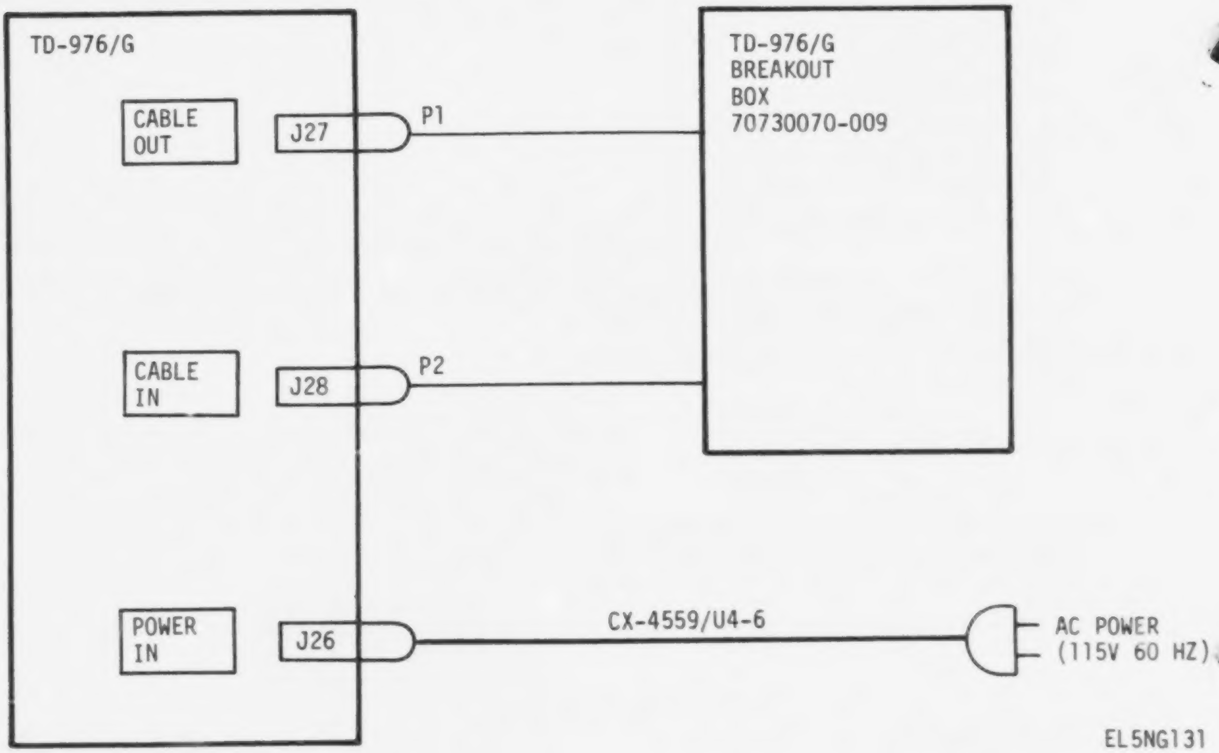

TD-976/G
CABLE OUT
J27
P1
TD-976/G BREAKOUT BOX 70730070-009
CABLE IN
J28
P2
POWER IN
J26
CX-4559/U4-6
AC POWER (115V 60 HZ)
EL5NG131

Figure 3-1. Power supply output test and cable fault detection test setup diagram.

between the TD-976/G and the RAU is brought out to a test point on the RAU feedthru box. Power for the RAU is supplied by a power supply connected to the RAU feedthru box.

c. *Test Equipment Required.* Table 3-7 lists the test equipment required to perform the alarm and indicator lamp test.

d. *Test Procedures.* Perform the procedures in table 3-8 to test the indicator lamps and audible ALARM horn. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-18.

Table 3-7. Test Equipment Required for Alarm and Indicator Lamp Test

Test equipment	Qty	NSN or part No.
Cable assembly CX-4559/U4-6.	1	5995-00-985-7772
Extender card.	1	SM-D-941960
Power supply PP-3940A.	1	6130-00-460-2148
RAU feedthru box (Martin Marietta).	1	70730000-009

Table 3-8. Alarm and Indicator Lamp Test

Step	Procedure	Normal indication
	INITIAL SETUP	
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to ON. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF. DATA RATE switch on edge of MO/C card 21A4 to HI (up position). Eight GROUP switches on edges of DGP cards 21A6 to OFF (down position).	
2	On RAU, set LAMP switch to ON.	
3	Connect test setup as shown in figure 3-2. Leave power supply PP-3940A turned off and set power supply voltage control for minimum (0-volt) output.	
	INDICATOR LAMP CHECK	
4	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	POWER AC and POWER DC indicators light (if indicators do not light, repeat paragraph 3-9). Ignore other indicators that may be lit at this time.
5	Turn on power supply PP-3940A and adjust for 24 v dc output (dial accuracy).	
6	On TD-976/G, press and hold ALARM TEST switch.	*a.* All front panel and RAU visual indicators are lit. *b.* Front panel audible ALARM horn produces an on-off beeping sound.
7	On TD-976/G, release ALARM TEST switch.	*a.* Audible ALARM horn stops sounding. *b.* Various front panel and RAU visual indicators may still be lit. Observe that for each RAU indicator that is lit, the corresponding front panel indicator is also lit.
8	On RAU, set and hold LAMP switch to TEST.	*a.* All front panel and RAU visual indicators are lit. *b.* Front panel audible ALARM horn produces an on-off beeping sound.
9	On RAU, set LAMP switch to ON.	Audible ALARM horn stops sounding.
	CARD EDGE LED CHECK	
10	On TD-976/G, set DIGITAL LOOP BACK switch to OFF and observe LED's on edges of FS card 21A7 and SG D/R card 21A9.	Both LED's are lit.
11	On TD-976/G, momentarily connect a jumper between test points TP1 and TP3 on MO/C card 21A4.	LED on edge of MO/C card lights while jumper is connected.
12	On TD-976/G, momentarily connect a jumper between test points TP1 and Tp2 on TC (M) card 21A5.	LED on edge of TC (M) card lights while jumper is connected.
13	Use extender card (para 3-3) to extend AD card 21A1.	
14	On extender card, connect jumpers between following points: Pin 35 and GND. Pin 49 and GND.	LED on edge of TC (D) card 21A5 lights.
15	On TD-976/G, set POWER SUPPLY switch to OFF.	
16	Remove AD card from extender card, remove extender card from card file, and disconnect jumpers. Reinstall AD card in card file.	
17	Turn off test equipment, disconnect test setup, and proceed to data transfer test (para 3-11).	

3-11. Data Transfer Test

a. General. This paragraph contains procedures for testing the ability of the TD-976/G to create an output SG, to synchronize to and demultiplex the SG, and to process group data. Subparagraph *b* below contains a brief functional description of the data transfer test.

b. Functional Test Description. The functional description of the data transfer test is contained in (1) through (7) below.

(1) The TD-976/G is configured in step 4 of table 3-10 so that an activity pattern is applied as input data for each group. These data inputs are multiplexed into an output SG by the multiplexer section. The multiplexer section also generates the frame syn-

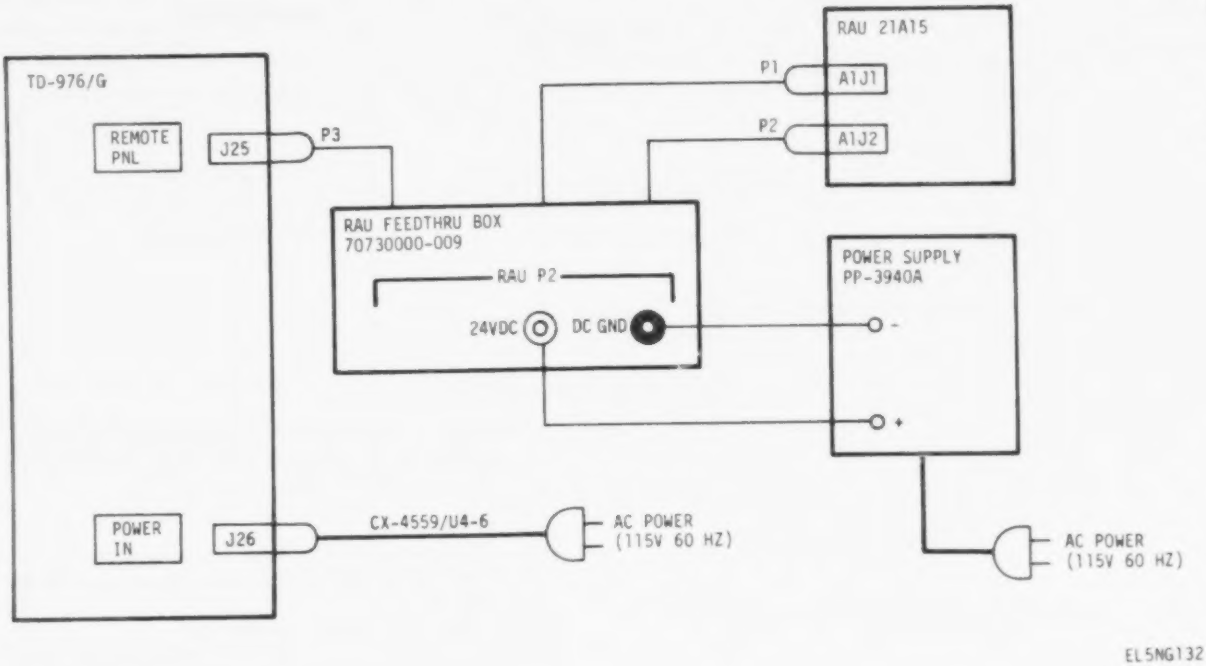


Figure 3-2. Alarm and indicator lamp test setup diagram.

chronization and stuff pattern contained in the O/H portion of the output SG. The output SG, which is in a bipolar format, is then looped back to the demultiplexer section by the TD-976/G breakout box. In the demultiplexer section, the SG is demultiplexed into its composite groups. The major thrust of this specific test is twofold: To determine if the multiplexer section can generate a SG and to determine if the demultiplexer section can synchronize to the SG. A lit CABLE SIGNAL indicator denotes no activity at the SG output of the multiplexer section. A lit FRAME ALARM indicator denotes that the demultiplexer section is unable to acquire frame/major frame synchronization.

(2) Steps 5 and 6 of table 3-10 check the output frequencies of the two oscillators on MO/C card 21A4.

(3) Step 7 of table 3-10 checks the ability of the demultiplexer section to recognize when it is not in frame/major frame synchronization and to light the appropriate indicators which denote that fact. Setting the CABLE switch on the TD-976/G breakout box to OFF interrupts the SG input to the demultiplexer section and places it in an out of sync condition.

(4) Step 8 of table 3-10 checks the ability of the TD-976/G to recognize the condition of no activity on the SG output of the multiplexer section and to light the CABLE SIGNAL indicator and cause the audible ALARM horn to sound. This condition of no activity at the SG output is established by setting the DIGITAL LOOP BACK switch to ON.

(5) Steps 10 through 33 of table 3-10 check the ability of the TD-976/G to accurately process data on an individual group basis. Individually, the PCM input to each group is disconnected, causing the INPUT ALARMS indicator for that group to light. With no PCM input, that group now inserts a dummy pattern as its data into the SG. In turn, the demultiplexed group output is checked by the TD-976/G for the presence of a dummy pattern which, if detected, causes the DUMMY SIGNAL indicator to light. Setting the individual GROUP switch to OFF causes an activity pattern to be applied as input data for that group and extinguishes the INPUT ALARMS and DUMMY SIGNAL indicators.

(6) Steps 34 through 38 of table 3-10 sequentially check the demultiplexed group data and timing output waveforms. The waveforms are checked for amplitude, pulse width, rise and fall times, and phase relationship to each other.

(7) Steps 39 through 49 of table 3-10 check the characteristics of the output SG waveform.

c. Test Equipment Required. Table 3-9 lists the test equipment required to perform the data transfer test.

d. Test Procedures. Perform the procedures in table 3-10 to accomplish the data transfer test. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-19.

Table 3-9. Test Equipment Required for Data Transfer Test

Test equipment	Qty	NSN or part No.
Cable assembly CG-2437/TCC-10 ft.	1	5995-00-916-2252
Cable assembly CG-2438/TCC-10 ft.	1	5995-00-913-0510
Cable assembly CX-4559/U4-6.	1	5995-00-985-7772
Cable assembly (Martin Marietta).	8	70730080-009
Cable assembly (Martin Marietta).	2	70730080-019
Digital counter AN/USM-207A.	1	6625-00-044-3228
Oscilloscope OS-261/U.	1	6625-00-127-0079
TD-976/G breakout box (Martin Marietta).	1	70730070-009

Table 3-10. Data Transfer Test

Step	Procedure	Normal indication
	INITIAL SETUP	
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to OFF. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF. DATA RATE switch on edge of MO/C card 21A4 to HI (up position). Eight GROUP switches on edges of DGP card 21A6 to OFF (down position). CABLE MILES switch on edge of SG D/R card 21A9 to ¼ (counterclockwise position).	
2	On TD-976/G breakout box, set switches as follows: MODE SELECT to LOOP. CABLE to ON.	
3	Connect test setup as shown in figure 3-3.	
	SG OUTPUT AND FRAME SYNC CHECK	
4	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	*a.* POWER AC and POWER DC indicators light (if indicators do not light, repeat paragraph 3-9). *b.* Observe that following front panel indicators are out: FRAME ALARM. EQUIP ALARM. CABLE SIGNAL. DUMMY SIGNAL. INPUT ALARMS 1 - 8. OUTPUT ALARMS 1 - 8.
	OSCILLATOR FREQUENCY CHECKS	
5	Connect digital counter to TP4 (input) and TP1 (ground) on MO/C card 21A4.	Digital counter indicates 9,830,400 ±50 Hz. (If frequency is out of tolerance, adjust oscillator Y2 on MO/C card by performing steps (4) through (6) of paragraph 3-25*b*.)
6	Connect digital counter to TP5 (input) and TP1 (ground) on MO/C card 21A4.	Digital counter indicates 4,608,000 ±20 Hz. (If frequency is out of tolerance, adjust oscillator Y1 on MO/C card by performing steps (8) through (10) of paragraph 3-25*b*.) Disconnect frequency counter.
	FRAME ALARM AND CABLE SIGNAL CHECK	
7	On TD-976/G breakout box, set CABLE switch to OFF.	Audible ALARM horn sounds and following indicators are lit. FRAME ALARM. EQUIP ALARM. LED on edge of SG D/R card 21A9. LED on edge of FS card 21A7.
8	On TD-976/G, set DIGITAL LOOP BACK switch to ON.	CABLE SIGNAL indicator is lit and audible ALARM horn continues to sound.
9	On TD-976/G, set DIGITAL LOOP BACK switch to OFF. On TD-976/G breakout box, set CABLE switch to ON.	Alarm indicators go out and audible ALARM horn stops sounding.

Table 3-10. Data Transfer Test—Continued

GROUP DATA CHECKS

NOTE

Refer to placarding on TD-976/G front cover (previously removed) to locate specific DGP card GROUP switches called out in steps 10 through 33 below.

Step	Procedure	Normal indication
10	On TD-976/G, set GROUP 1 switch on DGP card 21A6 to ON.	INPUT ALARMS 1, OUTPUT ALARMS 1, and DUMMY SIGNAL indicators remain out.
11	Disconnect cable from PCM IN GROUP 1 and PCM OUT GROUP 8 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 1 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
12	On TD-976/G, set GROUP 1 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 1 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
13	On TD-976/G, set GROUP 2 switch on DGP card 21A6 to ON.	INPUT ALARMS 2, OUTPUT ALARMS 2, and DUMMY SIGNAL indicators remain out.
14	Disconnect cable from PCM IN GROUP 2 and PCM OUT GROUP 1 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 2 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
15	On TD-976/G, set GROUP 2 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 2 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
16	On TD-976/G, set GROUP 3 switch on DGP card 21A6 to ON.	INPUT ALARMS 3, OUTPUT ALARMS 3, and DUMMY SIGNAL indicators remain out.
17	Disconnect cable from PCM IN GROUP 3 and PCM OUT GROUP 2 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 3 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
18	On TD-976/G, set GROUP 3 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 3 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
19	On TD-976/G, set GROUP 4 switch on DGP card 21A6 to ON.	INPUT ALARMS 4, OUTPUT ALARMS 4, and DUMMY SIGNAL indicators remain out.
20	Disconnect cable from PCM IN GROUP 4 and PCM OUT GROUP 3 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 4 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
21	On TD-976/G, set GROUP 4 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 4 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
22	On TD-976/G, set GROUP 5 switch on DGP card 21A6 to ON.	INPUT ALARMS 5, OUTPUT ALARMS 5, and DUMMY SIGNAL indicators remain out.
23	Disconnect cable from PCM IN GROUP 5 and PCM OUT GROUP 4 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 5 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
24	On TD-976/G, set GROUP 5 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 5 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
25	On TD-976/G, set GROUP 6 switch on DGP card 21A6 to ON.	INPUT ALARMS 6, OUTPUT ALARMS 6, and DUMMY SIGNAL indicators remain out.
26	Disconnect cable from PCM IN GROUP 6 and PCM OUT GROUP 5 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 6 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
27	On TD-976/G, set GROUP 6 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 6 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
28	On TD-976/G, set GROUP 7 switch on DGP card 21A6 to ON.	INPUT ALARMS 7, OUTPUT ALARMS 7, and DUMMY SIGNAL indicators remain out.
29	Disconnect cable from PCM IN GROUP 7 and PCM OUT GROUP 6 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 7 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
30	On TD-976/G, set GROUP 7 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 7 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
31	On TD-976/G, set GROUP 8 switch on DGP card 21A6 to ON.	INPUT ALARMS 8, OUTPUT ALARMS 8, and DUMMY SIGNAL indicators remain out.

Table 3-10. *Data Transfer Test—Continued*

Step	Procedure	Normal indication
32	Disconnect cable from PCM IN GROUP 8 and PCM OUT GROUP 7 connectors on rear of TD-976/G.	*a.* INPUT ALARMS 8 and DUMMY SIGNAL indicators light. *b.* Audible ALARM horn sounds.
33	On TD-976/G, set GROUP 8 switch on DGP card 21A6 to OFF.	*a.* INPUT ALARMS 8 and DUMMY SIGNAL indicators go out. *b.* Audible ALARM horn stops sounding.
	GROUP LEVEL WAVEFORM CHECKS	
34	Connect cable assembly 70730080-019 between PCM OUT GROUP 1 connector on rear of TD-976/G and PCM IN connector on TD-976/G breakout box.	
35	Connect second 70730080-019 cable assembly between TMG OUT GROUP 1 connector on rear of TD-976/G and TMG IN connector on TD-976/G breakout box.	
36	On TD-976/G breakout box, connect oscilloscope channel 1 to PCM OUT connector and channel 2 to TMG OUT connector. Trigger oscilloscope with channel 1.	
37	Refer to figure 3-4 and perform the following checks: *a.* Check data waveform (oscilloscope channel 1) for proper characteristics. *b.* Check timing waveform (oscilloscope channel 2) for proper characteristics. *c.* Check for proper phase relationship between timing and data waveform.	Compliance with figure 3-4.
38	Sequentially connect cable assemblies 70730080-019 to PCM OUT and TMG OUT connectors on rear of TD-976/G for GROUPS 2 through 8 and repeat waveform check of step 37 for each group.	Compliance with figure 3-4.
	SG WAVEFORM CHECK	
39	Disconnect P1 and P2 of TD-976/G breakout box from CABLE OUT connector J27 and CABLE IN connector J28, respectively, on rear of TD-976/G. Disconnect two 70730080-019 cables connected between TD-976/G and TD-976/G breakout box. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	
40	On TD-976/G breakout box, set CABLE switch to OFF.	
41	Set CABLE MILES switch on SG D/R card 21A9 to ½ (clockwise position).	
42	Connect cable assemblies CG-2437/TCC and CG-2438/TCC together.	
43	Connect one end of cables assembled in step 42 to CABLE OUT connector J27 on rear of TD-976/G. Connect other end of assembled cables to S/G IN connector on TD-976/G breakout box.	
44	Use cable assembly 70730080-019 and connect SYNC connector on TD-976/G front panel to oscilloscope external trigger input. Set oscilloscope for external triggering mode and for ac vertical coupling.	
45	Using oscilloscope probe, connect oscilloscope vertical input to S/G OUT connector on TD-976/G breakout box.	
46	On TD-976/G, set DIGITAL LOOP BACK switch to ON.	
47	Adjust oscilloscope vertical position to superimpose baseline of SG output signal on zero scale line of oscilloscope screen (SG signal is all logic O's).	Peak-to-peak ripple and noise is less than 0.2 volt.
48	On TD-976/G, set DIGITAL LOOP BACK switch to OFF.	
49	Refer to figure 3-5 and check characteristics of SG waveform displayed on oscilloscope.	Compliance with figure 3-5.
50	On TD-976/G, set POWER SUPPLY switch to OFF.	
51	Turn off test equipment disconnect test setup, and proceed to AVOW test (para 3-12).	

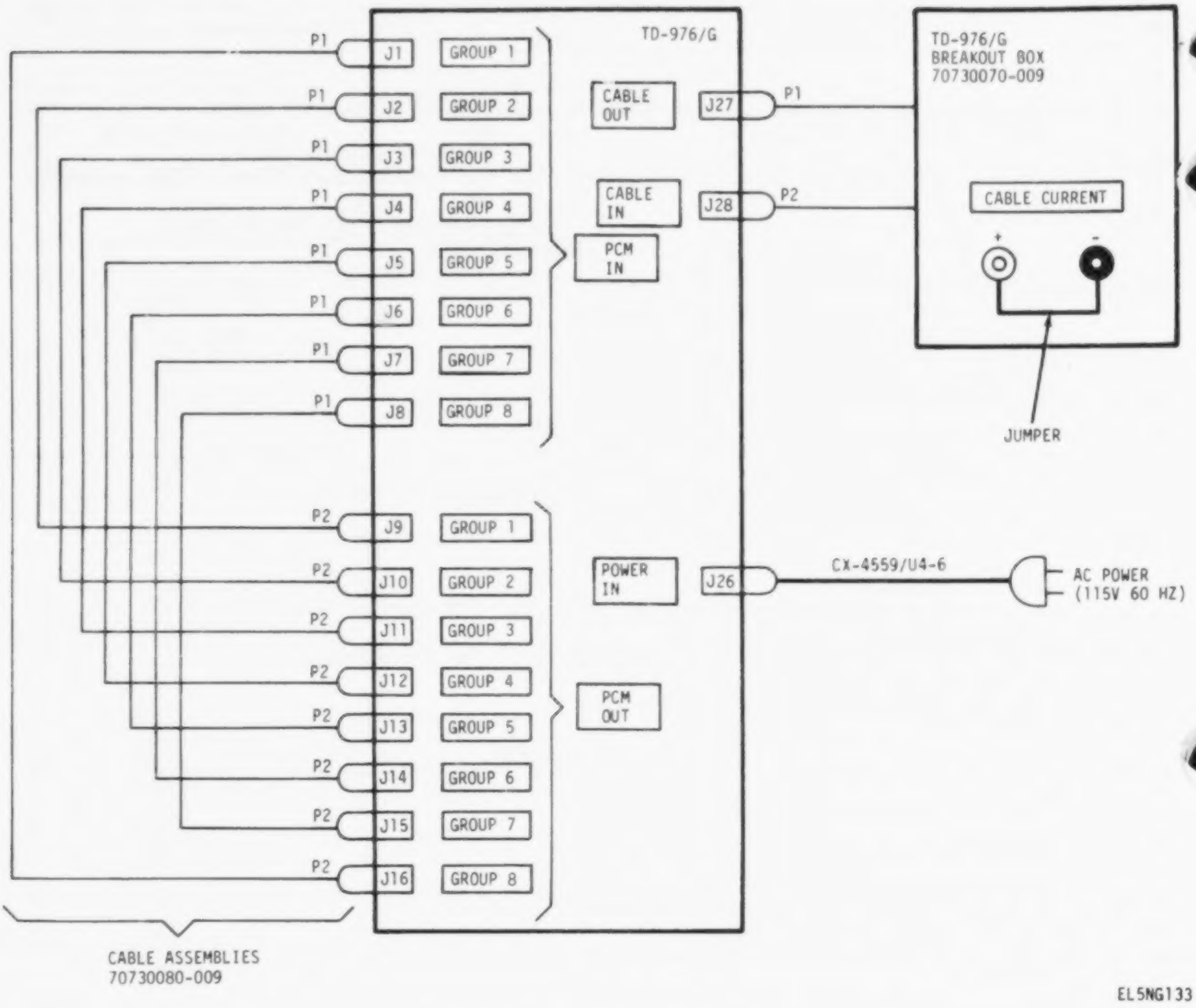

TD-976/G
P1
J1
GROUP 1
P1
J2
GROUP 2
P1
J3
GROUP 3
P1
J4
GROUP 4
P1
J5
GROUP 5
P1
J6
GROUP 6
P1
J7
GROUP 7
P1
J8
GROUP 8
CABLE OUT
J27
P1
CABLE IN
J28
P2
PCM IN
TD-976/G BREAKOUT BOX 70730070-009
CABLE CURRENT
+
-
JUMPER
P2
J9
GROUP 1
P2
J10
GROUP 2
P2
J11
GROUP 3
P2
J12
GROUP 4
P2
J13
GROUP 5
P2
J14
GROUP 6
P2
J15
GROUP 7
P2
J16
GROUP 8
POWER IN
J26
CX-4559/U4-6
AC POWER (115V 60 HZ)
PCM OUT
CABLE ASSEMBLIES 70730080-009
EL5NG133

Figure 3-3. Data transfer test setup diagram.

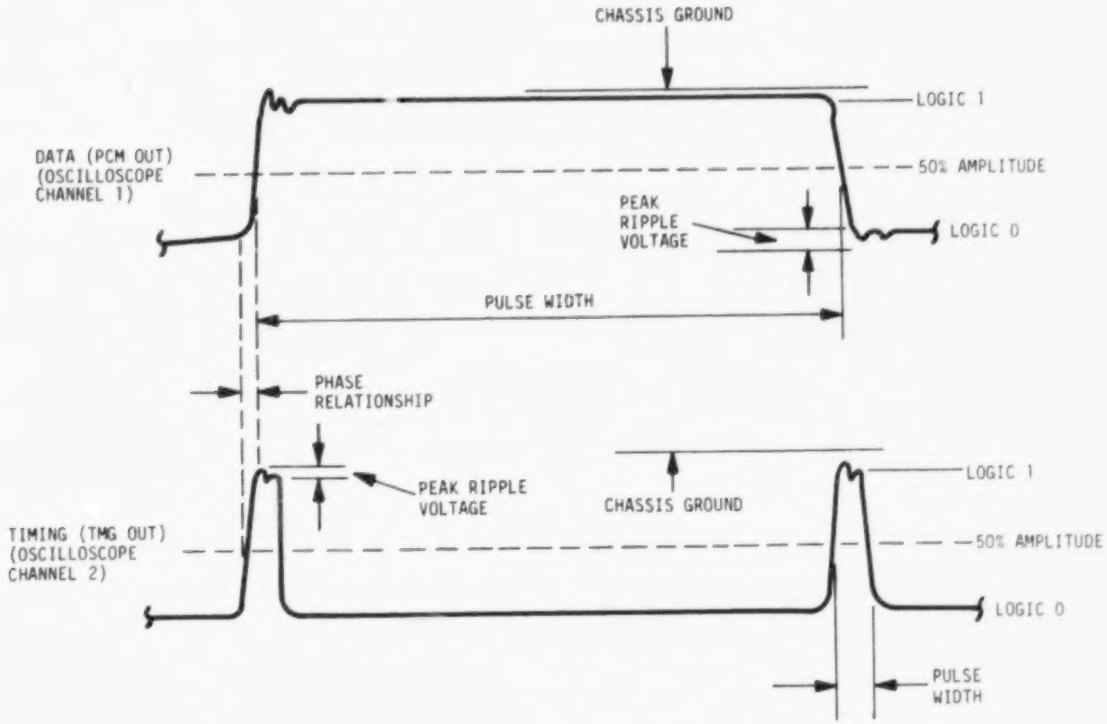
3-12. AVOW Test

a. General. This paragraph contains the procedures for testing the AVOW circuits in the TD-976/G and in the RAU attached to the TD-976/G. A RAU can also be tested separately as described in section VI. Subparagraph *b* below contains a brief functional description of the AVOW test.

b. Functional Test Description. The functional description of the AVOW test is contained in (1) through (4) below.

(1) *AVOW transmit checks.* The AVOW transmit circuits are tested with a 1 kHz test tone applied to the MIC input of the handset breakout box, which is connected to either the TD-976/G front panel or the RAU. The amplified analog signals at the TD-976/G SG output are then measured at a connector on the TD-976/G breakout box. An AVOW transmit check conducted at the TD-976/G front panel is contained in steps 5 through 9 of table 3-12. The same check conducted at the RAU is contained in steps 23 through 25.

(2) *AVOW sidetone checks.* The AVOW sidetone circuits are tested with the SG loop broken and a 1 kHz test tone applied to the MIC input of the handset breakout box, which is connected to either the TD-976/G front panel or the RAU. The analog sidetone signal is then measured at the EAR output of the handset breakout box. A sidetone check conducted at the TD-976/G front panel is contained in steps 10 and 11 of table 3-12. The same check conducted at the RAU is contained in steps 20 through 22.


CHASSIS GROUND
LOGIC 1
DATA (PCM OUT) (OSCILLOSCOPE CHANNEL 1)
50% AMPLITUDE
PEAK RIPPLE VOLTAGE
LOGIC 0
PULSE WIDTH
PHASE RELATIONSHIP
PEAK RIPPLE VOLTAGE
CHASSIS GROUND
LOGIC 1
TIMING (TMG OUT) (OSCILLOSCOPE CHANNEL 2)
50% AMPLITUDE
LOGIC 0
PULSE WIDTH

NOTES:

1. DATA IS IN FORM OF 7-BIT REPEATING ACTIVITY PATTERN (0001101, FIRST BIT IN TIME ON LEFT). ONLY 1 BIT OF DATA SHOWN IN ABOVE WAVEFORM.

2. DATA CHARACTERISTICS:

   PULSE AMPLITUDE (LOGIC 1) - -0.2±0.2V DC
   PULSE AMPLITUDE (LOGIC 0) - -2.2±0.2V DC
   PULSE WIDTH - 1.73±0.2 USEC (50% POINT)
   RISE AND FALL TIMES - 120 NSEC MAX (10 TO 90% POINTS)
   PEAK RIPPLE VOLTAGE - LESS THAN 400 MV (PEAK-TO-PEAK)

3. TIMING CHARACTERISTICS:

   PULSE AMPLITUDE (LOGIC 1) - -0.2±0.2V DC
   PULSE AMPLITUDE (LOGIC 0) - -2.2±0.2V DC
   PULSE WIDTH - 100±20 NSEC (50% POINT)
   RISE AND FALL TIMES - 120 NSEC MAX (10 TO 90% POINTS)
   PEAK RIPPLE VOLTAGE - LESS THAN 400 MV (PEAK-TO-PEAK)

4. PHASE RELATIONSHIP:

   POSITIVE-GOING EDGE OF TIMING SIGNAL LEADS DATA TRANSITION BY 10 TO 70 NSEC AS MEASURED AT 50% POINTS.

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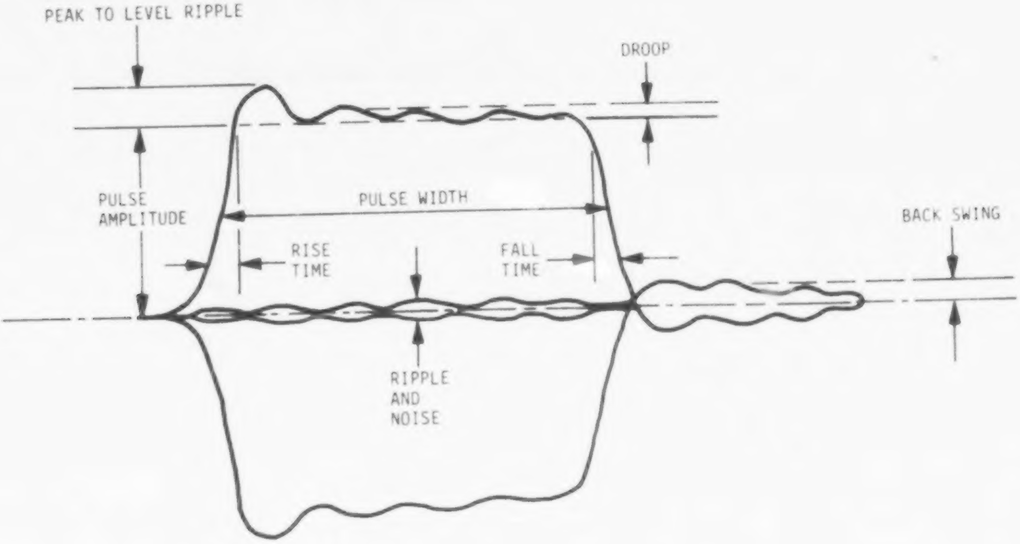
Figure 3-4. PCM data and timing waveforms.

(3) *AVOW receive checks.* The AVOW receive circuits are tested with a 1 kHz test tone applied through the TD-976/G breakout box to the TD-976/G SG input. The received analog signals are then measured at the EAR output of the handset breakout box, which is connected to either the TD-976/G front panel or the RAU. A receive check conducted at the TD-976/G front panel is contained in steps 12 through 15 of table 3-12. The same check conducted at the RAU is contained in steps 16 through 19.

(4) *Ring checks.* The AVOW ring circuits are tested by calling yourself. A ring is initiated and processed through the transmit circuits, looped back to the TD-976/G SG input by the TD-976/G breakout box,



DESCRIPTION	VALUE
PULSE WIDTH	100±10 NSEC (50% POINTS)
PULSE AMPLITUDE	0.9±0.1 VOLT
DROOP	0.2 VOLT MAX
RISE TIME	25 NSEC MAX (10 TO 90% POINTS)
FALL TIME	25 NSEC MAX (10 TO 90% POINTS)
BACK SWING	0.2 VOLT MAX
RIPPLE AND NOISE	LESS THAN 200 MV PEAK-TO-PEAK
PEAK TO LEVEL RIPPLE	0.3 VOLT MAX

NOTES:

1. MEASURE ALL CHARACTERISTICS, EXCEPT RIPPLE AND NOISE VOLTAGE, FOR BOTH POSITIVE AND NEGATIVE HALVES OF WAVEFORM.
2. OSCILLOSCOPE VERTICAL INPUT MUST BE CONNECTED TO TD-976/G BREAKOUT BOX USING OSCILLOSCOPE PROBE. USING COAXIAL CABLE FOR THIS INTERCONNECTION WILL INDUCE IMPROPER SIGNAL LOADING.

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Figure 3-5. SG output data characteristics.

and detected by the receive circuits. A ring check conducted at the TD-976/G front panel is contained in steps 26 through 29 of table 3-12. The same check conducted at the RAU is contained in steps 30 and 31.

c. Test Equipment Required. Table 3-11 lists the test equipment required to perform the AVOW test.

d. Test Procedures. Perform the procedures in table 3-12 to accomplish the AVOW test. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-20.

Table 3-11. Test Equipment Required for AVOW Test

Test equipment	Qty	NSN or part No.
Audio level meter TA-885/U.	1	6625-00-255-1083
Cable assembly CX-4559/U4-6.	1	5995-00-985-7772
Cable assembly (Martin Marietta).	1	70730080-019
Digital multimeter (DMM).	1	6625-01-010-9255
Handset breakout box (Martin Marietta).	1	70730060-009
Power supply PP-3940A.	1	6130-00-460-2148
RAU feedthru box (Martin Marietta).	1	70730000-009
Signal generator SG-970/U.	1	6625-00-145-1193
TD-976/G breakout box (Martin Marietta).	1	70730070-009

Table 3-12. AVOW Test

Step	Procedure	Normal indication
	INITIAL SETUP	
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to ON. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF. VOICE O.W. SELECT to CABLE. VOICE O.W. TALK/LISTEN-OFF-RING to TALK/LISTEN.	
2	On RAU, set switches as follows: LAMP to ON. TTY RCV-OFF-READY to OFF. TTY SEND-OFF-RING to OFF. VO ORDW CABLE to OFF. VO ORDW SYSTEM to OFF.	
3	On TD-976/G breakout box, set switches as follows: MODE SELECT to LOOP. CABLE to ON.	
4	Connect test setup as shown in figure 3-6. Leave power supply PP-3940A turned off and set power supply voltage control for minimum (0-volt) output.	
	NOTE An external DMM is used when adjusting output levels of the signal generator. Do not use meter on signal generator to set output levels.	
	AVOW TRANSMIT CHECK (TD-976/G)	
5	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	POWER AC and POWER DC indicators light (if indicators do not light, repeat paragraph 3-9).
6	Turn on audio level meter and DMM. Set audio level meter controls as follows: INPUT to TMS BRDG. FUNCTION to 600 BAL.	
7	Turn on signal generator and adjust for 1 kHz sinewave output (dial accuracy). Adjust signal generator output level to 224 + 2 mv rms as indicated on DMM.	
8	Turn on power supply PP-3940A and adjust for 24 v dc output (dial accuracy).	
9	Disconnect DMM from handset breakout box. Connect DMM to CABLE IN connector on TD-976/G breakout box. Observe DMM indication.	2.75 ± 0.275 v rms.
	AVOW SIDETONE CHECK (TD-976/G)	
10	On TD-976/G breakout box, set CABLE switch to OFF.	
11	Observe audio level meter indication.	− 24 dBm ± 4 dB (54 ± 23 mv rms).
	AVOW RECEIVE CHECK (TD-976/G)	
12	On TD-976/G breakout box, set CABLE switch to ON and disconnect P1 from CABLE OUT connector J27 on rear of TD-976/G.	
13	Disconnect signal generator from handset breakout box and connect signal generator to CABLE IN connector on TD-976/G breakout box (DMM still connected to CABLE IN connector on TD-976/G breakout box).	
14	Adjust signal generator for 1 kHz sinewave output (dial accuracy). Adjust signal generator output level to 2.75 ± 0.1 v rms as indicated on DMM.	
15	Observe audio level meter indication.	− 18 dBm ± 2 dB (97 ± 20 mv rms).
	AVOW RECEIVE CHECK (RAU)	
16	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to OFF.	
17	Disconnect handset breakout box from TD-976/G and reconnect to HANDSET connector on RAU (audio level meter	

Table 3-12. AVOW Test—Continued

Step	Procedure	Normal indication
	still connected to EAR output of handset breakout box).	
18	On RAU, set VO ORDW CABLE switch to T/L.	
19	Observe audio level meter indication.	−18 dBm ± 2 dB (97 ± 20 mv rms).
	AVOW SIDETONE CHECK (RAU)	
20	Disconnect signal generator from CABLE IN connector on TD-976/G breakout box and reconnect to MIC input on handset breakout box. Disconnect DMM from CABLE IN connector on TD-976/G breakout box and reconnect DMM to MIC jacks on handset breakout box.	
21	Adjust signal generator for 1 kHz sinewave output (dial accuracy). Adjust signal generator output level to 224 ± 2 mv rms as indicated on DMM.	
22	Observe audio level meter indication.	− 24 dBm ± 4 dB (54 ± 23 mv rms).
	AVOW TRANSMIT CHECK (RAU)	
23	On TD-976/G breakout box, reconnect P1 to CABLE OUT connector J27 on rear of TD-976/G.	
24	Connect DMM to CABLE IN connector on TD-976/G breakout box.	
25	Observe DMM indication.	2.75 ± 0.275 v rms.
	RING CHECK (TD-976/G)	
26	On RAU, set VO ORDW CABLE switch to OFF.	
27	Disconnect signal generator from handset breakout box.	
28	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and then back to OFF.	*a.* On TD-976/G, VOICE O.W. CABLE CALL indicator lights and audible ALARM horn sounds. *b.* On RAU, VO ORDW CABLE CALL indicator lights.
29	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to TALK/LISTEN and then back to OFF.	*a.* On TD-976/G, VOICE O.W. CABLE CALL indicator goes out and audible ALARM horn is silenced. *b.* On RAU, VO ORDW CABLE CALL indicator goes out.
	RING CHECK (RAU)	
30	On RAU, set VO ORDW CABLE switch to RING and then back to OFF.	Same as step 28.
31	On RAU, set VO ORDW CABLE switch to T/L and then back to OFF.	Same as step 29.
32	On TD-976/G, set POWER SUPPLY switch to OFF.	
33	Turn off test equipment, disconnect test setup, and proceed to DVOW test (para 3-13).	

3-13. DVOW Test

a. General. This paragraph contains the procedures for testing the DVOW circuits in the TD-976/G and in the RAU attached to the TD-976/G. A RAU can also be tested separately as described in section VI. Subparagraph *b* below contains a brief functional description of the DVOW test.

b. Functional Test Description. The functional description of the DVOW test is contained in (1) through (6) below.

(1) *DVOW call check.* In this test, a ring is initiated, digitally encoded by the DVOW circuits, and inserted into the SG. The SG is then looped back to the demultiplexer input where the DVOW data are demultiplexed and decoded back into an analog signal. The DVOW ring detector detects the analog ring signal and causes the appropriate indicators to light. A DVOW call check is conducted from both the TD-976/G front panel and from the RAU.

(2) *DVOW 4-wire transmit and receive gain check.* In this test, a 1 kHz test tone is applied to the 4-wire DVOW input on the RAU (DGTL VO XMT receptacle). The test tone is digitally encoded and inserted into the SG and is then looped back to the demultiplexer section input. The DVOW data are demultiplexed out of the SG and decoded back into an analog signal which is measured at the 4-wire DVOW output on the RAU (DGTL VO RCV receptacle).

(3) *DVOW noise check.* In this test, the test tone is removed from the DVOW 4-wire RAU input and the noise is measured at the DVOW 4-wire RAU output.

(4) *DVOW receive (less sidetone) checks.* In this test, a test tone is applied to the 4-wire DVOW input on the RAU (DGTL VO XMT receptacle). The test tone is digitally encoded and inserted into the SG and then looped back to the demultiplexer section input. The DVOW data are demultiplexed out of the SG and decoded back into an analog signal which is measured, by

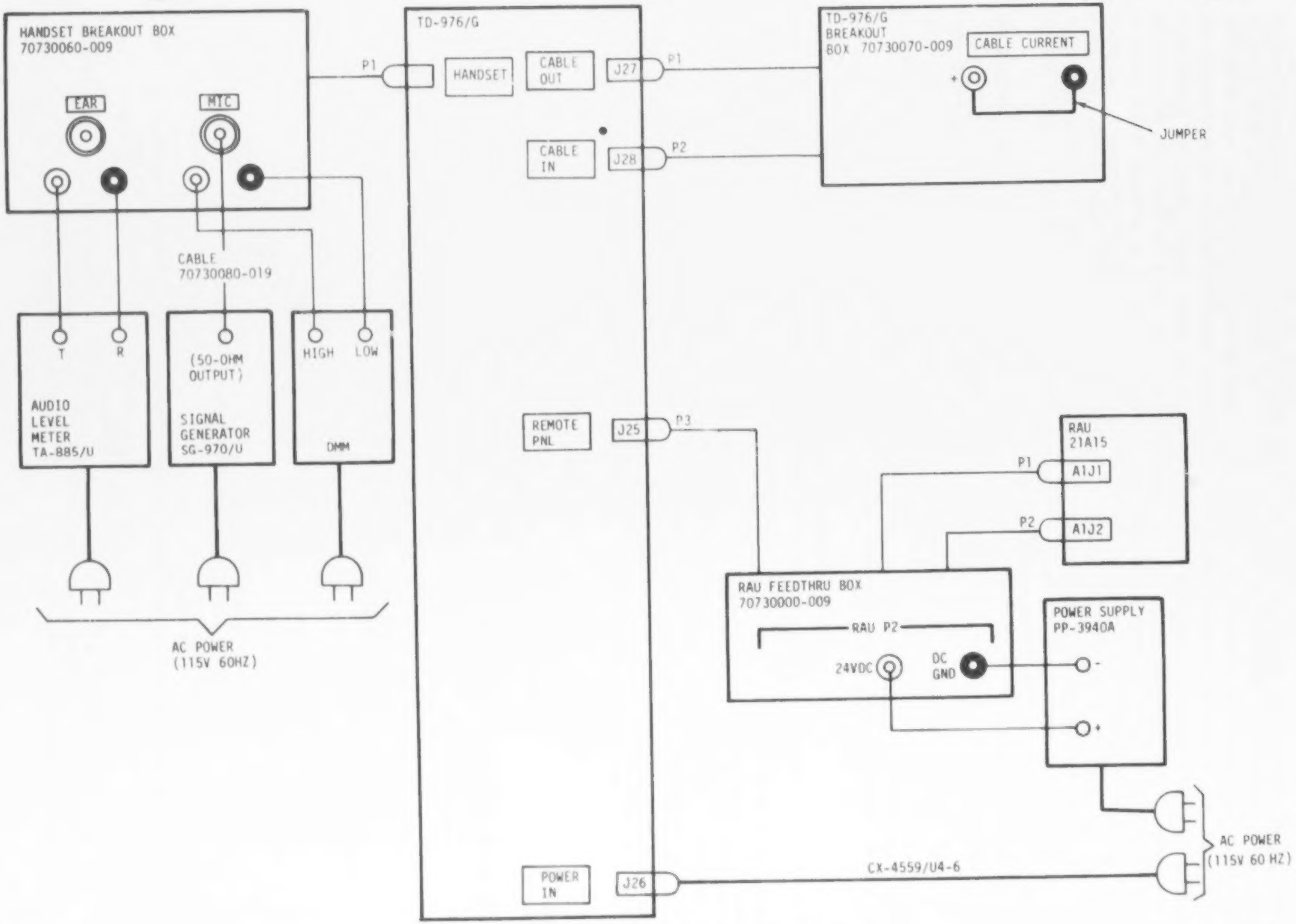
HANDSET BREAKOUT BOX
70730060-009
EAR
MIC
P1
TD-976/G
HANDSET
CABLE OUT
CABLE IN
J27
J28
P1
P2
TD-976/G
BREAKOUT
BOX 70730070-009
CABLE CURRENT
+
JUMPER
CABLE
70730080-019
T
R
AUDIO
LEVEL
METER
TA-885/U
(50-OHM
OUTPUT)
SIGNAL
GENERATOR
SG-970/U
HIGH
LOW
DMM
AC POWER
(115V 60HZ)
REMOTE PNL
J25
P3
RAU
21A15
P1
A1J1
P2
A1J2
RAU FEEDTHRU BOX
70730000-009
RAU P2
24VDC
DC
GND
POWER SUPPLY
PP-3940A
-
+
POWER IN
J26
CX-4559/U4-6
AC POWER
(115V 60 HZ)

Figure 3-6. AVOW test setup diagram.

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use of the handset breakout box, at the ear output of the front panel and RAU HANDSET connectors. The DVOW receive (less sidetone) check conducted at the TD-976/G front panel is contained in steps 18 through 22 of table 3-14. The same check conducted at the RAU is contained in steps 23 through 26.

(5) *DVOW sidetone check.* In this test, a test tone is applied, by use of the handset breakout box, to the microphone input of the front panel or RAU HANDSET connector. The resulting sidetone is measured, by use of the handset breakout box, at the ear output of the front panel or RAU HANDSET connector. The DIGITAL LOOP BACK switch on the TD-976/G is set to OFF so that no SG is applied to the demultiplexer section input. The DVOW sidetone check conducted at the TD-976/G front panel is contained in steps 27 through 33 of table 3-14. The same check conducted at the RAU is contained in steps 42 through 44.

(6) *DVOW transmit gain checks.* In this test, a test tone is applied, by use of the handset breakout box, to the microphone input of the front panel or RAU HANDSET connector. The test tone is digitally encoded and inserted into the SG and then looped back to the demultiplexer section input. The DVOW data are demultiplexed out of the SG and decoded back into an analog signal which is measured at the output of DVOW card 21A11. The DVOW transmit gain check conducted at the TD-976/G front panel is contained in steps 34 through 37 of table 3-14. The same check conducted at the RAU is contained in steps 38 through 41.

c. *Test Equipment Required.* Table 3-13 lists the test equipment required to perform the DVOW test.

d. *Test Procedures.* Perform the procedures in table 3-14 to accomplish the DVOW test. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-21.

Table 3-13. Test Equipment Required for DVOW Test

Test equipment	Qty	NSN or part No.
Audio level meter TA-885/U.	1	6625-00-255-1083
Cable assembly CX-4559/U4-6.	1	5995-00-985-7772
Cable assembly (Martin Marietta).	1	70730085-009
Cable assembly (Martin Marietta).	1	70730085-019
Handset breakout box (Martin Marietta).	1	70730060-009
Power supply PP-3940A.	1	6130-00-460-2148
RAU feedthru box (Martin Marietta).	1	70730000-009
Signal generator SG-970/U.	1	6625-00-145-1193

Table 3-14. DVOW Test

Step	Procedure	Normal indication
	INITIAL SETUP	
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to ON. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF. VOICE O.W. SELECT to SYSTEM. VOICE O.W. TALK/LISTEN-OFF-RING to OFF.	
2	On RAU, set switches as follows: LAMP to ON. TTY RCV-OFF-READY to OFF. TTY SEND-OFF-RING to OFF. VO ORDW CABLE to OFF. VO ORDW SYSTEM to OFF.	
3	Connect test setup as shown in figure 3-7. Leave power supply PP-3940A turned off and set power supply voltage control for minimum (0 volt) output. **NOTE** An external DMM is used when adjusting output levels of the signal generator. Do not use meter on signal generator to set output levels.	
	DVOW CALL CHECK	
4	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	*a.* POWER AC and POWER DC indicators light (if indicators do not light, repeat paragraph 3-9). *b.* FRAME ALARM indicator is out (if indicator is lit, repeat paragraph 3-11).

Table 3-14. DVOW Test—Continued

Step	Procedure	Normal indication
5	Turn on power supply PP-3940A and adjust for 24 v dc output (dial accuracy).	
6	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and then back to OFF.	*a.* On TD-976/G, VOICE O.W. SYSTEM CALL indicator lights and audible ALARM horn sounds. *b.* On RAU, VO ORDW SYSTEM CALL indicator lights.
7	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to TALK/LISTEN and then back to OFF.	*a.* On TD-976/G, VOICE O.W. SYSTEM CALL indicator goes out and audible ALARM horn is silenced. *b.* On RAU, VO ORDW SYSTEM CALL indicator goes out.
8	On RAU, set VO ORDW SYSTEM switch to RING and then back to OFF.	Same as step 6.
9	On RAU, set VO ORDW SYSTEM switch to T/L and then back to OFF.	Same as step 7.
DVOW 4-WIRE TRANSMIT AND RECEIVE GAIN CHECK		
10	Connect P1 of cable 70730085-009 to DGTL VO XMT receptacle on RAU. Use a BNC-to-banana adapter and connect P2 and P3 of this cable to ground and output terminals, respectively, of signal generator. Use 600-ohm output connector on signal generator. Connect DMM across signal generator output.	
11	Connect P1 of cable 70730085-019 to DGTL VO RCV receptacle on RAU. Connect P2 and P3 of this cable to R (ground) and T (input) terminals, respectively, of audio level meter.	
12	Turn on audio level meter and set controls as follows: INPUT to TMS TERM. FUNCTION to 600 BAL.	
13	Turn on signal generator and adjust for 1 kHz sinewave output (dial accuracy). Adjust signal generator output level to 488 ± 4 mv rms as indicated on DMM.	
14	Observe audio level meter indication.	– 4 dBm ± 1 dB (488 ± 53 mv rms into 600 ohms).
DVOW NOISE CHECK		
15	Record audio level meter indication of step 14. Set audio level meter controls as follows: NOISE WGT to F1A. FUNCTION to 600 BAL. INPUT to NOISE TERM.	
16	Disconnect P1 of cable 70730085-009 from DGTL VO XMT receptacle on RAU.	
17	Observe audio level meter indication.	Meter reads at least 55 dB below value recorded in step 15.
DVOW RECEIVE (LESS SIDETONE) CHECK (TD-976/G)		
18	Reconnect P1 of cable 70730085-009 to DGTL VO XMT receptacle on RAU. Check to ensure that signal generator output level is still 488 mv rms; adjust if necessary.	
19	Disconnect cable 70730085-019 from RAU and audio level meter.	
20	Use test leads and connect audio level meter terminals to handset breakout box (meter R (ground) to black EAR test point and meter T (input) to red EAR test point). Set audio level meter controls as follows: INPUT to TMS BRDG. FUNCTION to 600 BAL.	
21	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to TALK/LISTEN.	
22	Observe audio level meter indication.	– 21 dBm ± 2 dB (69 ± 14 mv rms)
23	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to OFF.	
24	Disconnect handset breakout box from TD-976/G and reconnect to HANDSET connector on RAU (audio level meter still connected to EAR output of breakout box).	
25	On RAU, set VO ORDW SYSTEM switch to T/L.	
26	Observe audio level meter indication.	– 21 dBm ± 2 dB (69 ± 14 mv rms)

Table 3-14. DVOW Test—Continued

Step	Procedure	Normal indication
	DVOW SIDETONE CHECK (TD-976/G)	
27	On RAU, set VO ORDW SYSTEM switch to OFF.	
28	Disconnect handset breakout box from RAU and reconnect to HANDSET connector on TD-976/G (audio level meter still connected to EAR output of breakout box).	
29	Disconnect cable 70730085-009 from RAU and signal generator.	
30	On TD-976/G, set DIGITAL LOOP BACK switch to OFF.	
31	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to TALK/LISTEN.	
32	Use test leads and connect signal generator to handset breakout box (generator ground to black MIC test point and generator output to red MIC test point). Use 50-ohm output connector on signal generator. Adjust signal generator output level to 224 ± 2 mv rms as indicated on DMM.	
33	Observe audio level meter indication.	− 24 dBm ± 4 dB (49 ± 18 mv rms)
	DVOW TRANSMIT GAIN CHECK (TD-976/G)	
34	On TD-976/G, set DIGITAL LOOP BACK switch to ON.	
35	Disconnect audio level meter leads from EAR test points on handset breakout box.	
36	Connect audio level meter ground lead to TP1 (ground) on DVOW card 21A11. Connect meter input lead to TP3 on DVOW card 21A11.	
37	Observe audio level meter indication.	− 11.1 dBm ± 2 dB (215 ± 44 mv rms)
	DVOW TRANSMIT GAIN CHECK (RAU)	
38	On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to OFF.	
39	Disconnect handset breakout box from TD-976/G and reconnect to HANDSET connector on RAU (signal generator still connected to MIC input of breakout box).	
40	On RAU, set VO ORDW SYSTEM switch to T/L. Check to ensure that signal generator output level is still 224 ± 2 mv rms, adjust if necessary.	
41	Observe audio level meter indication.	− 11.1 dBm ± 2 dB (215 ± 44 mv rms)
	DVOW SIDETONE CHECK (RAU)	
42	On TD-976/G, set DIGITAL LOOP BACK switch to OFF.	
43	Disconnect audio level meter from DVOW card 21A11 and reconnect to handset breakout box (meter ground lead to black EAR test point and meter input lead to red EAR test point).	
44	Observe audio level meter indication.	− 24 dBm ± 4 dB (49 ± 18 mv rms)
45	On TD-976/G, set POWER SUPPLY switch to OFF.	
46	Turn off test equipment, disconnect test setup, and proceed to cable fault detection test (para 3-14).	

3-14. Cable Fault Detection Test

a. General. This paragraph contains the procedures for testing the TD-976/G cable system fault detection circuits. Subparagraph *b* below contains a brief functional description of the cable fault detection test.

b. Functional Test Description. During the cable fault detection test, the TD-976/G breakout box is used to introduce loading of the TD-976/G constant current cable power supply. The breakout box also introduces simulated TD-982/G pulse form restorers for purposes of testing the TD-976/G cable fault detection and display circuits.

c. Test Equipment Required. Table 3-15 lists the test equipment required to perform the cable fault detection test.

d. Test Procedures. Perform the procedures in table 3-16 to test the TD-976/G cable fault detection circuits. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-22.

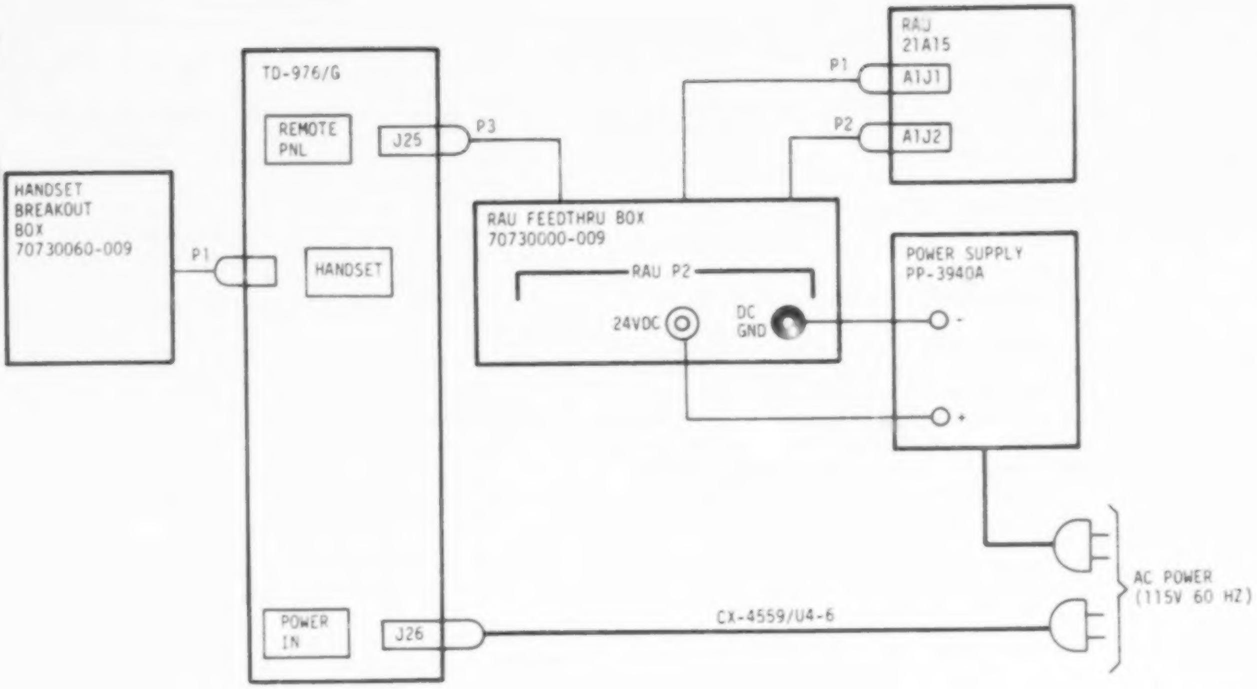

TD-976/G
REMOTE PNL
J25
P3
HANDSET
POWER IN
J26
HANDSET BREAKOUT BOX 70730060-009
P1
RAU 21A15
P1
A1J1
P2
A1J2
RAU FEEDTHRU BOX 70730000-009
RAU P2
24VDC
DC GND
POWER SUPPLY PP-3940A
-
+
CX-4559/U4-6
AC POWER (115V 60 HZ)
EL5NG137

Figure 3-7. DVOW test setup diagram.

Table 3-15. Test Equipment Required for Cable Fault Detection Test

Test Equipment	Qty	NSN or part No.
Cable assembly CX-4559/U4-6	1	5995-00-985-7772
TD-976/G breakout box (Martin Marietta)	1	70730070-009

Table 3-16. Cable Fault Detection Test

Step	Procedure	Normal indication
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to OFF. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF. CABLE MILES switch on edge of SG D/R card 21A9. to ½ (clockwise position).	
2	On TD-976/G breakout box, set switches as follows: MODE SELECT to TEST. CABLE to ON. FAULT SELECT to 1.	
3	Connect test setup as shown in figure 3-1.	
4	Connect a test lead between one of the GND test points on front of TD-976/G card file and POWER IN – test point on TD-976/G breakout box.	

Table 3-16. Cable Fault Detection Test—Continued

<table>
<tr><th>Step</th><th>Procedure</th><th>Normal indication</th></tr>
<tr><td>5</td><td>Connect a second test lead between +5V test point on front of TD-976/G card file and POWER IN + test point on TD-976/G breakout box.</td><td></td></tr>
<tr><td>6</td><td>On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.</td><td>a. POWER AC and POWER DC indicators on TD-976/G light (if indicators do not light, repeat paragraph 3-9).
b. STATUS +5V POWER and STATUS DATA indicators on TD-976/G breakout box light.</td></tr>
<tr><td>7</td><td>On TD-976/G, set POWER CABLE switch to ON.</td><td>a. POWER IN and POWER OUT indicators on TD-976/G light (if indicators do not light, repeat paragraph 3-9).
b. STATUS CABLE POWER indicator on TD-976/G breakout box lights.</td></tr>
<tr><td>8</td><td>On TD-976/G, set CABLE TEST switch to ON.</td><td>STATUS DATA indicator on TD-976/G breakout box blinks on and off.</td></tr>
<tr><td>9</td><td>Allow CABLE FAULT indicator display on TD-976/G front panel to stabilize. Then rotate FAULT SELECT switch on TD-976/G breakout box to each position and note indication on CABLE FAULT indicators on TD-976/G front panel. An "x" in the normal indication column indicates which indicator(s) should be lit. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.</td><td>
<table>
<tr><th>FAULT SELECT switch position</th><th>CABLE FAULT indication 16 8 4 2 1</th></tr>
<tr><td>1</td><td>- - - - x</td></tr>
<tr><td>2</td><td>- - - x -</td></tr>
<tr><td>3</td><td>- - - x x</td></tr>
<tr><td>4</td><td>- - x - -</td></tr>
<tr><td>5</td><td>- - x - x</td></tr>
<tr><td>6</td><td>- - x x -</td></tr>
<tr><td>7</td><td>- - x x x</td></tr>
<tr><td>8</td><td>- x - - -</td></tr>
<tr><td>9</td><td>- x - - x</td></tr>
<tr><td>10</td><td>- x - x -</td></tr>
<tr><td>11</td><td>- x - x x</td></tr>
<tr><td>12</td><td>- x x - -</td></tr>
<tr><td>13</td><td>- x x - x</td></tr>
<tr><td>14</td><td>- x x x -</td></tr>
<tr><td>15</td><td>- x x x x</td></tr>
<tr><td>16</td><td>x - - - -</td></tr>
<tr><td>17</td><td>x - - - x</td></tr>
<tr><td>18</td><td>x - - x -</td></tr>
<tr><td>19</td><td>x - - x x</td></tr>
</table>
</td></tr>
<tr><td>10</td><td>ON TD-976/G, set POWER CABLE and POWER SUPPLY switches to OFF.</td><td></td></tr>
<tr><td>11</td><td>Disconnect test setup and proceed to DDOW test (para 3-15).</td><td></td></tr>
</table>

3-15. DDOW Test

a. General. This paragraph contains the procedures for testing the DDOW circuits in the TD-976/G and in the RAU attached to the TD-976/G. Subparagraph *b* below contains a brief functional description of the DDOW test.

b. Functional Test Description. The DDOW test checks the ability of the TD-976/G and its RAU to initiate and receive DDOW transmissions at both the 75- and 1200-baud rates. Ring generation and detection circuits are tested, as well as the ability to properly process teletype (TTY) signals from an external generator.

c. Test Equipment Required. Table 3-17 lists the test equipment required to perform the DDOW test.

d. Test Procedures. Perform the procedures in table 3-18 to accomplish the DDOW test. When a normal indication is not obtained, refer to the troubleshooting procedures in paragraph 3-23.

Table 3-17. Test Equipment Required for DDOW Test

Test equipment	Qty	NSN or part No.
Cable assembly CX-4559/U4-6.	1	5995-00-985-7772
Cable assembly (Martin Marietta).	1	70730085-009
Cable assembly (Martin Marietta).	1	70730085-019
Oscilloscope OS-261/U.	1	6625-00-127-0079
Pattern generator SG-1054/G.	1	6625-00-137-7738
Power supply PP-3135/U.	1	6625-00-635-7991
Power supply PP-3940A.	1	6130-00-460-2148
RAU feedthru box (Martin Marietta).	1	70730000-009
Resistor (6800-ohm ± 5%, 5-watt).	2	None

Table 3-18. DDOW Test

Step	Procedure	Normal indication
	INITIAL SETUP	
1	On TD-976/G, set switches as follows: DIGITAL LOOP BACK to ON. CABLE TEST to OFF. POWER CABLE to OFF. POWER SUPPLY to OFF.	
2	On RAU, set switches as follows: LAMP to ON. TTY RCV-OFF-READY to OFF. TTY SEND-OFF-RING to OFF. VO ORDW CABLE to OFF. VO ORDW SYSTEM to OFF.	
3	Remove DDOW encoder card 21A3 from TD-976/G and install card jumper switch between J2 and J3. Reinstall card.	
4	On RAU, remove six screws and washers securing RAU cover. Remove cover and set cover aside.	
5	On RAU circuit card, install jumper switches P1 through P4 to interconnect sockets marked A and B.	

WARNING

Potentials in excess of 130 v dc are applied to the RAU and interconnecting cables and test leads during the DDOW test. Exercise when making tests and measurements.

CAUTIONS

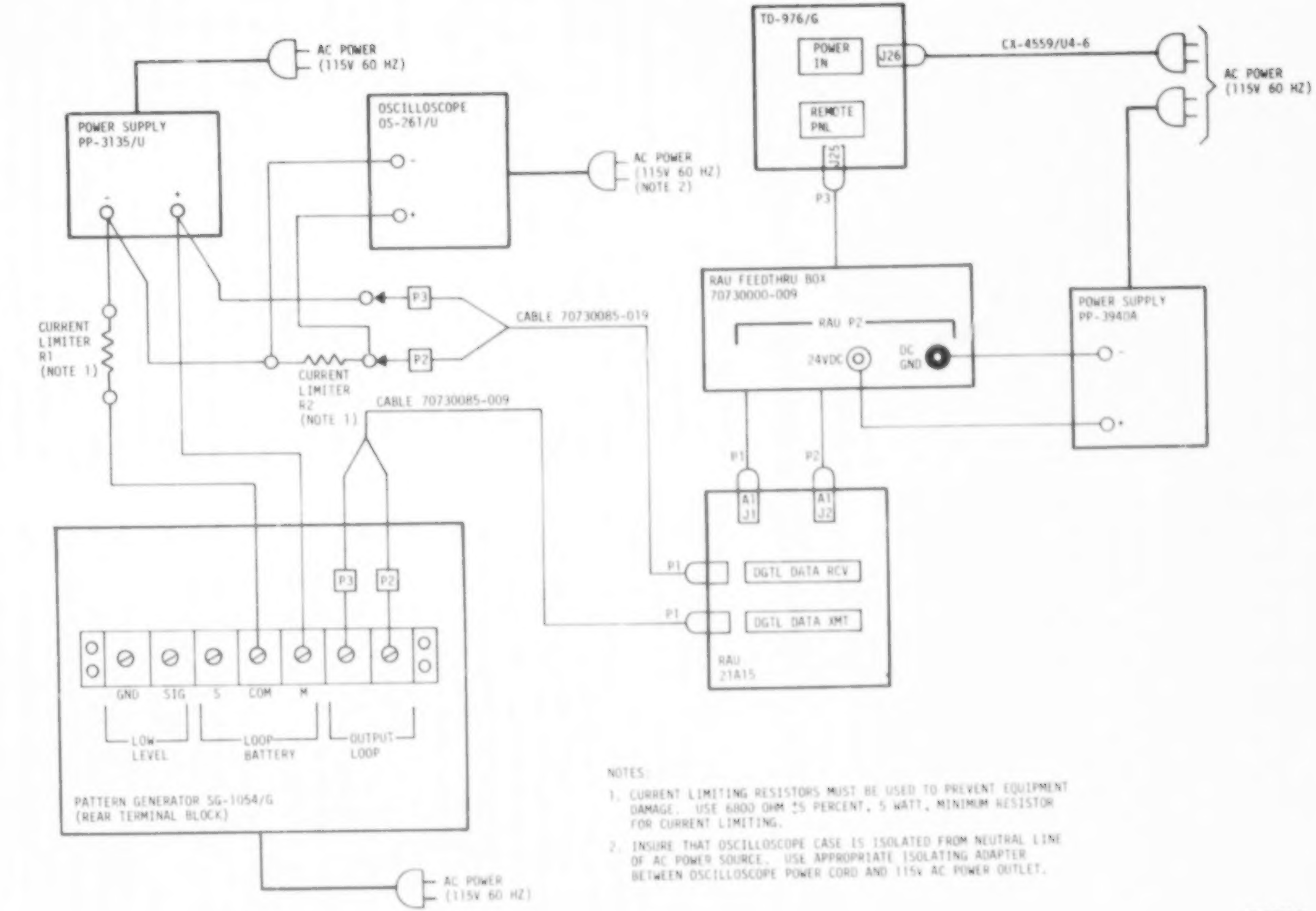
Do not turn on TD-976/G or any test equipment untill directed to do so in following procedures.

When connecting oscilloscope to ac power source, use appropriate adapter to isolate oscilloscope case from power source neutral line.

6	Connect test setup as shown in figure 3-8. Leave power supplies turned off and set power supply voltage controls for minimum (0-volt) outputs.	
7	Turn on power supply PP-3940A and adjust for 24 v dc output (dial accuracy).	
	RING/READY CALL CHECK	
8	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	POWER AC and POWER DC indicators light (if indicators do not light, repeat paragraph 3-9).
9	On RAU, set TTY SEND-OFF-RING switch to RING and then back to OFF.	*a.* On RAU, TTY CALL indicator lights. *b.* On TD-976/G, audible ALARM horn sounds.
10	On RAU, set TTY SEND-OFF-RING switch to SEND and then back to OFF.	*a.* On RAU, TTY CALL indicator goes out. *b.* On TD-976/G, audible ALARM horn is silenced.
11	On RAU, set TTY RCV-OFF-READY switch to READY and then back to OFF.	Same as step 9.
12	On RAU, set TTY RCV-OFF-READY to RCV, and TTY SEND-OFF-RING switch to SEND.	Same as step 10.
	75-BAUD CHECK	
13	On pattern generator, set controls as follows: Set up SELECTED CHARACTERS 1 pushbuttons for letter Y (depress BITS 1, 3, and 5 pushbuttons to program letter Y). Depress CHARACTER SEQUENCE LENGTH pushbutton 1. PATTERN to SELECTED CHARACTERS CODE LEVEL 5. DISTORTION PERCENT to 0. DISTORTION TYPE to OFF. BIT RATE to A and 75. MODE (left switch) to FREE RUN. MODE (right switch) to START/STOP UNIT STOP MARK 1.5. OUTPUTS HI-LEVEL SELECT to NEUT. CR/LF to OUT (switch located on generator rear panel).	
14	Turn on power supply PP-3135/U and adjust for +130 v dc output (dial accuracy).	

Table 3-18. DDOW Test—Continued

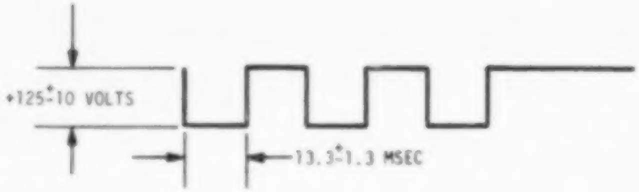
Step	Procedure	Normal indication
15	Turn on oscilloscope and pattern generator. Set oscilloscope for internal negative-going trigger mode.	
16	Observe oscilloscope.	Oscilloscope waveform as shown in A of figure 3-9.
	1200-BAUD CHECK	
17	Adjust power supply PP-3135/U for minimum output and then turn power supply off.	
18	Turn power supply PP-3940A off.	
19	On TD-976/G, set POWER SUPPLY switch to OFF.	
20	Disconnect oscilloscope and cable 70730085-019 from current limiter R2 (fig. 3-8).	
21	Disconnect leads from LOOP BATTERY COM and M terminals at rear of pattern generator (fig. 3-8). Disconnect leads and current limiting resistors from power supply PP-3135/U. Power supply PP-3135/U will not be used throughout remainder of test.	
22	Disconnect P2 and P3 of cable 70730085-009 from OUTPUT LOOP terminals at rear of pattern generator (fig. 3-8).	
23	Connect P2 and P3 of cable 70730085-009 to LOW LEVEL output terminals at front of pattern generator as follows: P2 to GND terminal. P3 to SIG terminal.	
24	Connect P2 of cable 70730085-019 to oscilloscope vertical input and P3 to oscilloscope return.	
25	Remove DDOW encoder card 21A3 from TD-976/G and install card jumper switch between J1 and J2. Reinstall card.	
26	On RAU circuit card, install jumper switches P1 through P4 to interconnect sockets marked A and C.	
27	Turn on power supply PP-3940A and check that output voltage is still +24 v dc (dial accuracy). If necessary, readjust power supply output.	
28	On TD-976/G, set POWER SUPPLY switch to ON. If audible ALARM horn sounds, momentarily press ALARM RESET switch to silence horn.	POWER AC and POWER DC indicators light (if indicators do not light, repeat paragraph 3-9).
29	On pattern generator, reposition controls as follows: Set up CHARACTERS 1 pushbuttons for letter U (refer to B of figure 2-16 and depress BITS 1, 3, 5, and 7 pushbuttons to program letter U). PATTERN to SELECTED CHARACTERS CODE LEVEL 8 BIT RATE to A and 1200 MODE (right switch) to START/STOP UNIT STOP MARK 2.0	
30	Turn pattern generator off, and verify that it is strapped to produce a positive low-level mark polarity and even parity as follows: Position low-level mark: strap on printed circuit card A3 is between 2 and 5. Even parity: strap on printed circuit card A8 is between 1 and 4. (Refer to T.O. 33A1-8-771-1 for detailed strapping instructions).	
31	Turn pattern generator on.	
32	Observe oscilloscope.	Oscilloscope waveforms as shown in B of figure 3-9.
33	On TD-976/G, set POWER SUPPLY switch to OFF.	
34	Turn off all test equipment and disconnect test setup.	
35	Install RAU cover removed in step 4 above.	
36	Test complete. This complets TD-976/G performance tests.	


AC POWER
(115V 60 HZ)
POWER SUPPLY
PP-3135/U
-
+
OSCILLOSCOPE
OS-261/U
-
+
AC POWER
(115V 60 HZ)
(NOTE 2)
CURRENT
LIMITER
R1
(NOTE 1)
P3
P2
CABLE 70730085-019
CURRENT
LIMITER
R2
(NOTE 1)
CABLE 70730085-009
P3
P2
GND
SIG
S
COM
M
LOW
LEVEL
LOOP
BATTERY
OUTPUT
LOOP
PATTERN GENERATOR SG-1054/G
(REAR TERMINAL BLOCK)
AC POWER
(115V 60 HZ)
TD-976/G
POWER
IN
J26
REMOTE
PNL
J25
P3
CX-4559/U4-6
AC POWER
(115V 60 HZ)
RAU FEEDTHRU BOX
70730000-009
RAU P2
24VDC
DC
GND
POWER SUPPLY
PP-3940A
-
+
P1
P2
A1
J1
A1
J2
P1
DGTL DATA RCV
P1
DGTL DATA XMT
RAU
21A15
EL5NG138

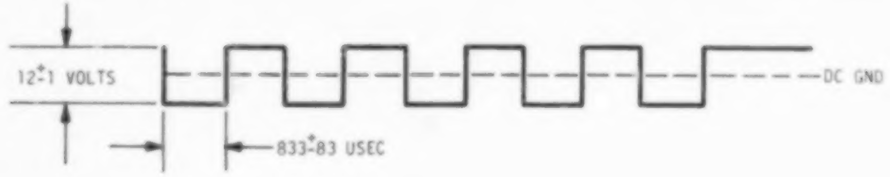
NOTES:

1. CURRENT LIMITING RESISTORS MUST BE USED TO PREVENT EQUIPMENT DAMAGE. USE 6800 OHM ±5 PERCENT, 5 WATT, MINIMUM RESISTOR FOR CURRENT LIMITING.
2. INSURE THAT OSCILLOSCOPE CASE IS ISOLATED FROM NEUTRAL LINE OF AC POWER SOURCE. USE APPROPRIATE ISOLATING ADAPTER BETWEEN OSCILLOSCOPE POWER CORD AND 115V AC POWER OUTLET.

Figure 3-8. DDOW test setup diagram.



A. 5-LEVEL CODE WAVEFORM FOR LETTER Y



B. 8-LEVEL CODE WAVEFORM FOR LETTER U

Figure 3-9. DDOW waveforms.

Section IV. TD-976/G TROUBLESHOOTING PROCEDURES

3-16. Introduction

a. General. This section contains the troubleshooting procedures for isolating a malfunction to the power supply, RAU, a plug-in card, a component or wiring problem in the front panel, or a component or wiring problem in the card file. There are seven troubleshooting procedures (paragraph 3-17 through 3-23) in this section. Each of the seven troubleshooting procedures is associated with one of the seven functional performance test procedures in section III. The troubleshooting procedure that is used in this section is determined, and identified, in the test procedure in which a faulty condition is detected.

b. Test Equipment and Tools Required for Troubleshooting. The tools and test equipment used in each of the test procedures in section III are also used in the associated troubleshooting procedure in this section. The only item not listed in table 3-3 that is used in the troubleshooting procedures is the extender card described in paragraph 3-3.

c. Troubleshooting Requirements.

(1) The TD-976/G will be connected in the same test configuration as directed in the associated test procedure at the time that the abnormal indication was obtained.

(2) The switches on the test equipment and the TD-976/G under test will be set in the same positions they were set at the time the abnormal indication was obtained.

(3) In some of the troubleshooting steps, it will be necessary to remove the front panel from the case to gain access to components and wiring mounted on the rear of the front panel. Front panel removal procedures are in paragraph 3-32.

(4) In some of the troubleshooting steps, it will be necessary to remove the card file from the case to gain access to components and wiring mounted in the card file. Card file removal procedures are in paragraph 3-37.

d. Troubleshooting Table Usage. Each of the troubleshooting tables in paragraphs 3-17 through 3-23 contains three columns. The contents and usage of the information in the columns are described in (1) through (3) below.

(1) *No. column.* Each abnormal indication and the appropriate troubleshooting actions are assigned an identification number. The identification number is listed under the "No." column to identify the starting point of each abnormal indication in the table.

(2) *Abnormal indication column.* This column lists each of the abnormal indications that could be obtained in the associated test procedures. As an aid in locating the abnormal indication associated with a given test condition, each abnormal indication in the "Abnormal indication" column contains a step number in parentheses. This step number in parentheses is the actual step number in the associated test procedures table in which the abnormal indication was detected. For example, assume that the user detects an abnormal indication when performing step 6 in a given test procedure. The "Abnormal indication" column in the associated troubleshooting table is scanned until an ab-

normal indication description is located that contains "(step 6)." It is possible that a given troubleshooting table could have more than one abnormal indication for a given test step. In this situation, there will be more than one abnormal indication in the troubleshooting table that contains the same step number in parentheses. At this time, the user selects the appropriate abnormal indication that was detected in the testing.

(3) *Action column.* This column contains the troubleshooting action that should be performed to isolate and correct the fault. The troubleshooting actions listed under the "Action" column are described in *e* below.

e. Troubleshooting Actions. The various troubleshooting actions are described in (1) through (4) below.

(1) *Switch settings.* In some of the actions, certain switch settings are changed to establish a specific condition to perform a troubleshooting function. When the troubleshooting procedure is completed, ensure that the equipment is returned to the original operating configuration it was in before the troubleshooting procedure was started.

(2) *Replace.* This action involves replacement of the listed items (power supply, plug-in cards, and/or RAU). When more than one item is listed to be replaced, replace the items, one at a time, in the order listed. Each time the replacement item does not eliminate the abnormal condition, install the original item back in the TD-976/G.

(3) *Check.* This action involves checking a component or circuit suspected to be the probable fault causing the abnormal indication. A number of the check actions are for components mounted on the front panel or the card file. Gaining physical access to these components generally requires some disassembly of the TD-976/G. However, in many cases, electrical access to these components can be obtained at pins of the plug-in circuit card to which they interface. Research the applicable schematic diagrams and wire run lists to determine interface pins. Extend the appropriate plug-in circuit card on the extender card and make the check.

(4) *Continuity checks and signal tracing.* If the abnormal indication still exists after all the listed troubleshooting actions have been performed, the problem has been isolated to a wiring or connector problem. Use the wire run in section XI and perform continuity checks of the wiring.

3-17. Power Supply Output Test Troubleshooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-9. In table 3-19, locate the abnormal indication under the "Abnormal indication" column and then perform the appropriate troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-19. Power Supply Output Test Troubleshooting Chart

No.	Abnormal indication	Action
1	POWER AC indictor does not light (step 4).	Check F1, F2, DS6, and S9 on front panel 21A14 (fig. 2-29).
2	POWER DC indicator does not light (step 4).	*a.* Cycle POWER SUPPLY switch to OFF and then back to ON. *b.* Perform step 5 of table 3-6 to check for presence of power supply dc outputs. If outputs are present and within tolerances, proceed to *c* below. If one or more outputs are missing or out of tolerance, replace power supply 21A12. *c.* Check for less than +1 v dc at anode of CR22 on front panel circuit card 21A14A1 (fig. 3-20). If voltage is greater than +1 v dc, replace power supply 21A12. If voltage is less than +1 v dc, check DS5 on front panel 21A14 and Q5 and associated parts on front panel circuit card 21A14A1 (fig. 2-29.
3	One or more card file power test point voltages missing or out of tolerance (step 5).	*a.* Replace power supply 21A12. *b.* If replacing power supply does not correct problem, perform following. (1) Set POWER SUPPLY switch to OFF. (2) Disengage cards 21A1 through 21A11 from their connectors. (3) Set POWER SUPPLY switch to ON and recheck card file power test point voltages. If voltages are still not present, troubleshoot TD-976/G wiring. If voltages are present, proceed to (4) below. (4) Reinstall cards 21A1 through 21A11, one at a time, while monitoring votage(s). Replace the card that, when installed, causes the voltage(s) to disappear.

Table 3-19. Power Supply Output Test Troubleshooting Chart—Continued

No.	Abnormal indication	Action
4	Ripple voltage of one or more voltages is greater than specified (step 6).	a. Replace power supply 21A12. b. If only −4.4 v ripple voltage is out of tolerance and replacing power supply did not correct problem, replace DGP cards 21A6, one at a time. Observe ripple voltage after each card replacement to isolate defective DGO card 21A6.
5	POWER CABLE switch is set to ON (step 7) and:	
	a. POWER IN, POWER OUT, and CABLE POWER indicators are out.	(1) Cycle POWER CABLE switch to OFF and then back to ON. (2) Replace power supply 21A12. (3) Check switch S8 on front panel 21A14 (fig. FO-17, sheet 2).
	b. POWER IN indictor is out and POWER OUT indicator is lit.	(1) Check DS3 on front panel 21A14 (fig. FO-17, sheet 1). (2) Check VR1, K1, and associated parts on front panel circuit card 21A14A1 (fig. FO-18, sheet 2).
	c. POWER OUT indicator is out and POWER IN indicator is lit.	(1) Check DS4 on front panel 21A14 (fig. FO-17, sheet 1). (2) Check VR2, K2, and associated parts on front panel circuit card 21A14A1 (fig. FO-18, sheet 2).
6	DMM indication of 4.5 ± 0.25 v dc is out of tolerance (steps 8, 9, and 11).	Replace power supply 21A12.
7	CABLE POWER indicator on TD-976/G breakout box is on when CABLE switch is cycled to OFF and back to ON (step 10).	Replace power supply 21A12.
8	CABLE POWER indicator on TD-976/G breakout box remains off when TD-976/G POWER CABLE switch is cycled to OFF and back to ON (step 11).	Replace power supply 21A12.

3-18. Alarm and Indicator Lamp Test Troubleshooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-10. In table 3-20, locate the abnormal indication under the "Abnormal indication" column and then perform the appropriate troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-20. Alarm and Indicator Lamp Test Troubleshooting Chart

No.	Abnormal indication	Action
1	One or more front panel and/or RAU visual indicators did not light while ALARM TEST switch was pressed (step 6).	a. Compare front panel and RAU indicators. (1) If corresponding front panel and RAU indicators did not light, replace AD card 21A1. Check S4 on front panel 21A14 (fig. FO-17, sheet 1). (2) If a front panel indicator did not light but corresponding RAU indicator did light, check that front panel indicator and associated parts (figs. FO-17 and FO-18). (3) If a RAU indicator did not light but corresponding front panel indicator did light, replace RAU 21A15. b. If one or more front panel CABLE FAULT indicators did not light, replace AVOW card 21A10. Check appropriate front panel CABLE FAULT indicator(s) (fig. FO-18, sheet 2).
2	Front panel audible ALARM horn did not sound while ALARM TEST switch was pressed (step 6).	a. Replace AD card 21A1. b. Check front panel ALARM horn LS1 (fig. FO-17, sheet 1).
3	A RAU indicator remained lit, but corresponding front panel indicator did not when ALARM TEST switch was released (step 7).	Replace RAU 21A15.
4	All front panel and RAU visual indicators did not light when RAU LAMP switch was set to TEST (step 8).	a. On RAU feedthru box, connect DDM + lead to RAU P1 EXAT and − lead to RAU P1 DC GND. b. On RAU, set and hold LAMP switch to TEST while noting DDM indication. (1) If DDM indicated +24 ± 2.4 v dc, replace AD card 21A1. (2) If DDM indicated 0.0 ± 0.5 v dc, replace RAU 21A15.

Table 3-20. Alarm and Indicator Lamp Test Troubleshooting Chart—Continued

No.	Abnormal indication	Action
5	LED's on FS card 21A7 and/or SG D/R card 21A9 did not light when DIGITAL LOOP BACK switch was set to OFF (step 10).	*a.* If both LED's did not light, replace TC (D) card 21A5. *b.* If only LED on SG D/R card 21A9 did not light, replace: (1) SG D/R card 21A9. (2) TC (D) card 21A5. *c.* If only LED on FS card 21A7 did not light, replace: (1) FS card 21A7. (2) TC (D) card 21A5. (3) AD card 21A1.
6	LED on MO/C card 21A4 did not light while jumper was connected (step 11).	Replace below listed cards: MO/C card 21A4. TC (M) card 21A5.
7	LED on TC (M) card 21A5 did not light while jumper was connected (step 12).	Replace TC (M) card 21A5.
8	LED on TC (D) card 21A5 did not light (step 14).	Replace below listed cards: TC (D) card 21A5. AD card 21A1.

3-19. Data Transfer Test Troubleshooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-11. In table 3-21, locate the abnormal indication under the "Abnormal indication" column and then perform the appropriate troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-21. Data Transfer Test Troubleshooting Chart

NOTE

There are two types of multiple-use plug-in circuit cards in the TD-976/G: Two 21A5 TC cards and four 21A6 DGP cards. The 21A5 card located in the fifth card slot from the front left is used in the multiplexer section and is defined as TC (M) card 21A5. The other 21A5 card is used in the multiplexer section and is defined as TC (D) card 21A5. The four 21A6 DGP cards are defined as DGP cards No. 1 through No. 4 (DGP card No. 1 is the leftmost card). DGP card No. 1 processes input/output data for groups 1 and 5, DGP card No. 2 processes input/output data for groups 2 and 6, and so on. Replace the DGP card that corresponds to the group in which the failure occurred.

No.	Abnormal indication	Action
1	One or more front panel indicators are lit (step 4). Note indicators that are lit, and sequentially progress through steps *a* through *g* below. Ensure that indicators for each step have been cleared before proceeding to the next step.	
	a. One or more INPUT ALARMS and/or OUTPUT ALARMS indicators are lit (ignore other indicators that may be lit).	*a.* Replace below listed cards. AD card 21A1. MO/C card 21A4. DGP card 21A6 (1 of 4). GTM card 21A2.
	b. CABLE SIGNAL indicator is lit (ignore other indicators that may be lit).	*b.* Replace below listed cards. SG D/R card 21A9. TC (M) card 21A5. MO/C card 21A4. AD card 21A1.
	c. EQUIP ALARM and LED's on edges of MO/C card 21A4 or TC (M) card 21A5 are lit (ignore other indicators that may be lit).	*c.* Replace below listed cards. TC (M) card 21A5. MO/C card 21A4.
	d. FRAME ALARM indicator lit (ignore other indicators that may be lit).	*d.* Replace below listed cards. SG D/R card 21A9. FS card 21A7. TC (D) card 21A5. TC (M) card 21A5. MO/C card 21A4. AD card 21A1.
	e. EQUIP ALARM and LED's on edges of TC (D) card 21A5 and/or FS card 21A7 are lit (ignore other indicators that may be lit).	*e.* Replace below listed cards. TC (D) card 21A5. FS card 21A7.

Table 3-21. Data Transfer Test Troubleshooting Chart—Continued

No.	Abnormal indication	Action
	f. EQUIP ALARM indicator is lit but no card edge LED's are lit.	*f.* Replace AD card 21A1.
	g. DUMMY SIGNAL indicator is lit.	*g.* Replace AD card 21A1.
2	Oscillator Y2 on MO/C card 21A4 cannot be adjusted to correct value (step 5).	Replace MO/C card 21A4.
3	Oscillator Y1 on MO/C card 21A4 cannot be adjusted to correct value (step 6).	Replace MO/C card 21A4.
4	Audible ALARM horn did not sound. FRAME ALARM, EQUIP ALARM, and LED's on card edges did not light (step 7).	Replace below listed cards. TC (D) card 21A5. FS card 21A7. AD card 21A1. SG D/R card 21A9.
5	Audible ALARM horn did not sound and CABLE SIGNAL indicator did not light (step 8).	Replace below listed cards. SG D/R card 21A9. AD card 21A1.
6	INPUT ALARMS, OUTPUT ALARMS, and/or DUMMY SIGNAL indicators are lit (steps 10, 13, 16, 19, 22, 25, 28, and 31).	*a.* If INPUT ALARMS and/or OUTPUT ALARMS indicators are lit (ignore DUMMY SIGNAL indicator), replace below listed cards. DGP card 21A6 (one of four). GTM card 21A2. MO/C card 21A4. FS card 21A7. *b.* If only DUMMY SIGNAL indicator is lit, replace GTM card 21A2.
7	INPUT ALARMS and/or DUMMY SIGNAL indicators did not light (steps 11, 14, 17, 20, 23, 26, 29, and 32).	Replace below listed cards. DGP card 21A6 (one of four). TC (M) card 21A5. TC (D) card 21A5. GTM card 21A2. AD card 21A1.
8	Group level waveforms incorrect (steps 37 and 38).	Replace DGP card 21A6 (one of four).
9	SG waveforms incorrect (steps 47 and 49).	Replace SG D/R card 21A9.

3-20. AVOW Test Troubleshooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-12. In table 3-22, locate the abnormal indication under the "Abnormal indication" column and then perform the appropriate troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-22. AVOW Test Troubleshooting Chart

No.	Abnormal indication	Action
1	Meter indication is incorrect (step 9).	*a.* If voltage is missing, perform following. (1) Replace AVOW card 21A10. (2) Replace SG D/R card 21A9. (3) Check transformer 21A13T1 (fig. FO-15). (4) Check switches S5 and S7 on front panel 21A14 (fig. FO-17, sheet 1). *b.* If voltage is present but out of tolerance, perform following. (1) Use extender card (para 3-3) to extend AVOW card 21A10. (2) Adjust R18 on AVOW card for proper DDM indication. (3) If adjustments cannot be made, replace AVOW card 21A10.
2	Meter indication is incorrect (step 11).	Replace AVOW card 21A10.
3	Meter indication is incorrect (step 15).	*a.* If meter reading is more than 20 dB below correct value, perform following. (1) Replace AVOW card 21A10. (2) Replace SG D/R card 21A9. (3) Check transformer 21A13T2 (fig. FO-15).

Table 3-22. AVOW Test Troubleshooting Chart—Continued

No.	Abnormal indication	Action
		b. If meter reading is within 20 dB of correct value, perform following. (1) Use extender card (para 3-3) to extend AVOW card 21A10. (2) Adjust R17 on AVOW card for proper audio level meter indication. (3) If adjustment cannot be made, replace AVOW card 21A10.
4	Meter indication is incorrect (step 19).	a. Replace AVOW card 21A10. b. Replace RAU 21A15.
5	Meter indication is incorrect (step 22).	Replace AVOW card 21A10.
6	Meter indication is incorrect (step 25).	Replace AVOW card 21A10.
7	On TD-976/G, VOICE O.W. TALK/LISTEN-OFF-RING switch is set to RING (step 28) and:	
	a. TD-976/G VOICE O.W. CABLE CALL and RAU VO ORDW CABLE CALL indicators do not light and audible ALARM horn does not sound.	(1) Use extender card (para 3-3) to extend AVOW card 21A10. Connect oscilloscope probe to card pin 47 and return to TP 1 of AVOW card. Observe oscilloscope for 1600 ± 50 Hz (625 ± 20 μsec period), 4.0 ± 1 volt peak-to-peak square wave. If waveform is present, proceed to (2) below; otherwise replace MO/C card 21A4. (2) Connect DDM to CABLE IN connector on TD-976/G breakout box. On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and then back to OFF while observing DDM. If DDM indicated 4.0 ± 1 v rms while switch was in RING position, proceed to (3) below; otherwise, perform following. (a) Replace AVOW card 21A10. (b) Check switch S7 on front panel 21A14 (fig. FO-17, sheet 1). (3) Use extender card (para 3-3) to extend AVOW card. Connect DDM + lead to card pin 51 and − lead to TP1 on AVOW card. On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and then back to OFF. If DMM indicates 0± 0.5 v dc, replace AD card 21A1; otherwise, proceed to (4) below. (4) Connect DMM + lead to TP9 and − lead to TP1 on AVOW card. Hold VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and adjust R61 on AVOW card for maximum rms reading on DMM; release switch. Proceed to (5) below. (5) Connect DMM + lead to card pin 51 and − lead to TP1 on AVOW card. On TD-976/G, set VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and then back to OFF. If DMM now indicates 0 ± 0.5 v dc, problem has been corrected; otherwise, replace AVOW card 21A10.
	b. TD-976/G VOICE O.W. CABLE CALL indicator lights and RAU VO ORDW CABLE CALL indicator does not light.	(1) Replace AD card 21A1. (2) Replace RAU 21A15.
	c. RAU VO ORDW CABLE CALL indicator lights and TD-976/G VOICE O.W. CABLE CALL indicator does not light.	(1) Replace AD card 21A1. (2) Check front panel indicator DS1 and associated parts (figs. FO-17 and FO-18).
	d. Audible ALARM horn does not sound.	Replace AD card 21A1.
8	Indicators do not go out and/or audible ALARM horn is not silenced (step 29).	a. Replace AVOW card 21A10. b. Replace AD card 21A1.
9	Indicators do not light and audible ALARM horn does not sound (step 30).	a. Replace RAU 21A15. b. Replace AVOW card 21A10.
10	Indicators do not go out and audible ALARM horn is not silenced (step 31).	a. Replace AVOW card 21A10. b. Replace RAU 21A15.

3-21. DVOW Test Troubleshooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-13. In table 3-23, locate the abnormal indication under the "Abnormal indication" column and then perform the appropriate troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-23. DVOW Test Troubleshooting Chart

No.	Abnormal indication	Action
1	CALL indicators do not light and/or ALARM horn fails to sound (step 6).	*a.* If either CALL indicator lights or ALARM horn sounds, but not both, replace AD card 21A1. *b.* If CALL indicators do not light and ALARM horn fails to sound, perform following. (1) Use extender card (para 3-3) to extend DVOW card 21A11. Connect oscilloscope to card pin 39 and return to card pin 40. On TD-976/G, hold VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and observe oscilloscope for 1600 ± 50 Hz (625 ± 20 μsec period), 1.5 ± 0.5 volt peak-to-peak alternating waveform. Release switch. (2) If waveform in (1) above is incorrect, perform following. (*a*) Replace AVOW card 21A10. (*b*) Replace MO/C card 21A4. (*c*) Check switches S5 and S7 on front panel 21A14 (fig. FO-17, sheet 1). (3) If waveform in (1) above is correct, connect DMM to TP1 (ground) and TP6 (meter input) on DVOW card. On TD-976/G, hold VOICE O.W. TALK/LISTEN-OFF-RING switch to RING and adjust R40 on DVOW card for maximum rms reading on DMM; release switch. Proceed to (4) below. (4) Repeat step 6 of table 3-14. If step still fails, perform following. (*a*) Replace DVOW card 21A11. (*b*) Replace TC (M) card 21A5. (*c*) Replace TC (D) card 21A5. (*d*) Replace MO/C card 21A4.
2	CALL indicators remain lit and ALARM horn continues to sound (step 7).	*a.* Use extender card (para 3-3) to extend DVOW card 21A11. Connect oscilloscope to card pin 39 and return to card pin 40. Observe oscilloscope for absence of 1600 ± 50 Hz (625 ± 20 μsec period), 1.5 ± 0.5 volt peak-to-peak alternating waveform. *b.* If waveform is present, replace AVOW card 21A10 and check switch S7 on front panel 21A14. *c.* If waveform is not present replace DVOW card 21A11.
3	CALL indicators do not light and ALARM horn fails to sound (step 8).	*a.* Connect DMM to following RAU P1 test points on RAU feedthru box. + lead to DVRNG—. − lead to DC GND. *b.* Observe DMM and set RAU VO ORDW SYSTEM switch to RING and then back to OFF. (1) If DMM indicated 0 ± 0.5 v dc while switch was in RING, replace AVOW card 21A10. (2) If DMM did not indicate 0 ± 0.5 v dc while switch was in RING, replace RAU 21A15.
4	CALL indicators remain lit and ALARM horn continues to sound (step 9).	*a.* Connect DMM to following RAU P1 test points on RAU feedthru box. + lead to RDTL— − lead to DC GND *b.* Set RAU VO ORDW SYSTEM switch to T/L. *c.* If DMM indicates 0 ± 0.5 v dc, replace DVOW card 21A11. If DMM indicates + 4.5 ± 1.0 v dc, replace RAU 21A15.
5	Meter indication is incorrect (step 14).	*a.* If meter reading is more than 20 dB below correct value, perform following. (1) Replace DVOW card 21A11. (2) Replace RAU 21A15.

Table 3-23. DVOW Test Troubleshooting Chart—Continued

No.	Abnormal indication	Action
		b. If meter reading is within 20 dB of correct value, use extender card (para 3-3) to extend DVOW card 21A11 and perform following. (1) Connect audio level meter between TP1 (ground) and TP5 (meter input) on DVOW card 21A11. Set audio level meter controls as follows: (*a*) INPUT to TMS BRDG. (*b*) FUNCTION to 600 BAL. (2) Observe meter for indication of −6.5 dBm ± 0.2 dB (366 ± 8 mv rms). If necessary, adjust R6 on DVOW card to obtain proper indication. If adjustment cannot be made, replace DVOW card 21A11. (3) Reconnect audio level meter to cable 70730085-019 that is connected to DGTL VO RCV receptacle on RAU. Connect P2 and P3 of this cable to R (ground) and T (input) terminals, respectively, of audio level meter. Set audio level meter controls as follows: (*a*) INPUT to TMS TERM. (*b*) FUNCTION to 600 BAL. (4) Observe meter for indication of −4 dBm ± 1 dB (488 ± 53 mv rms into 600 ohms). If necessary, adjust R57 on DVOW card to obtain proper indication. If adjustment cannot be made, replace DVOW card 21A11.
6	Meter does nto read 55 dB below recorded value (step 17).	Replace DVOW card 21A11.
7	Meter indication is incorrect (step 22).	*a.* If meter reading is more than 20dB below correct value, perform following. (1) Connect audio level meter between TP1 (ground) and TP3 (meter input) on DVOW card 21A11. Set audio level meter controls as follows: (*a*) INPUT to TMS BRDG. (*b*) FUNCTION to 600 BAL. (2) Observe meter for indication of −11.1 dBm ± 2 dB (215 ± 44 mv rms). If proper indication is obtained, replace AVOW card 21A10. If improper indication is obtained, replace DVOW card 21A11. *b.* If meter reading is within 20 dB of correct value, use extender card (para 3-3) to extend DVOW card 21A11. Adjust R59 on DVOW card for indication of −21 dBm + 2 dB (69 ± 14 mv rms) on audio level meter (audio level meter still connected to EAR test points on handset breakout box). If adjustment cannot be made, replace DVOW card 21A11.
8	Meter indication is incorrect (step 26).	*a.* Replace AVOW card 21A10. *b.* Replace RAU 21A15.
9	Meter indication is incorrect (step 33).	Replace AVOW card 21A10.
10	Meter indication is incorrect (step 37).	*a.* If meter reading is more than 20 dB below correct value, replace DVOW card 21A11. *b.* If meter reading is within 20 dB of correct value, use extender card (para 3-3) to extend DVOW card 21A11. Adjust R3 on DVOW card for indication of −11.1 dBm ± 2 dB (215 ± 44 mv rms) on audio level meter (audio level meter still connected to TP1 and TP3 on DVOW card). If adjustment cannot be made, replace DVOW card 21A11.
11	Meter indication is incorrect (step 41).	Replace AVOW card 21A10.
12	Meter indication is incorrect (step 44).	Replace AVOW card 21A10.

3-22. Cable Fault Detection Test Trouble shooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-14. In table 3-24, locate the abnormal indication under the "Abnormal indication" column and then perform the associated troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-24. Cable Fault Detection Test Troubleshooting Chart

No.	Abnormal indication	Action
1	STATUS +5V POWER indicator on TD-976/G breakout box did not light (step 6).	TD-976/G breakout box is defective (POWER AC and POWER DC indicators on TD-976/G are lit). Refer to TB 11-7025-202-34 (to be published).
2	STATUS DATA indicator on TD-976/G breakout box did not light (step 6).	TD-976/G breakout box is defective (CABLE SIGNAL indicator on TD-976/G is out). Refer to TB 11-7025-202-34 (to be published).
3	STATUS CABLE POWER indicator on TD-976/G breakout box did not light (step 7).	TD-976/G breakout box is defective (POWER IN and POWER OUT indicators on TD-976/G are lit). Refer to TB 11-7025-202-34 (to be published).
4	STATUS DATA indicator on TD-976/G breakout box does not blink (step 8).	*a.* Observe CABLE SIGNAL indicator on TD-976/G. If indicator is blinking on and off, TD-976/G breakout box is defective (refer to TB 11-7025-202-34, to be published). If CABLE SIGNAL is not blinking, proceed to *b* below. *b.* Connect oscilloscope to TP3 and return to TP1 (ground) on DDOW encoder card 21A3. Check for 75 ±7 Hz (13.3 ± 1.3 msec period) clock signal whose amplitude alternates between 0 ± 0.5 and +4 ± 1 volts. *c.* If clock signal is correct at TP3, perform following. (1) Replace SG D/R card 21A9. (2) Check switch S2 on front panel 21A14 (fig. FO-17, sheet 1). *d.* If clock signal is incorrect at TP3, perform the following. (1) Replace DDOW encoder card 21A3. (2) Replace MO/C card 21A4.
5	CABLE FAULT indicators on TD-976/G incorrect for one or more positions of TD-976/G breakout box FAULT SELECT switch (step 9).	*a.* Use extender card (para 3-3) to extend AVOW card 21A10. Connect DMM + lead to card pin 50 and − lead to card pin 49. If DMM indicates −2.53 ± 0.17 v dc, proceed to *b* below; otherwise, replace power supply 21A12. *b.* Perform steps (1) through (5) below. If adjustments cannot be made or if step 9 of table 3-16 still fails after making adjustments, perform the following. Replace AVOD card 21A10. Replace SG D/R card 21A9. Check capacitors C1, C2, and C3 and resistor R1 on card file 21A13 (fig. FO-15). (1) Connect channel 1 of oscilloscope to pin U8-7 and return to TP1 on AVOW card. Connect channel 2 of oscilloscope to pin U8-6 and return to TP1 on AVOW card. (2) On TD-976/G breakout box, set FAULT SELECT switch to position 1. (3) Adjust R86 on AVOW card for following conditions: (*a*) TD-976/G CABLE FAULT indicators 16, 8, 4, and 2 are off and 1 is on. (*b*) Oscilloscope channel 1 displays a logic 1 (+4 ± 1 v dc) with no pulses. (*c*) Oscilloscope channel 2 displays a square wave whose period is approximately 0.6 msec. Center R86 adjustment. (4) On TD-976/G breakout box, set FAULT SELECT switch to position 19. (5) Slowly adjust R80 on AVOW card for following conditions: (*a*) TD-976/G CABLE FAULT indicators 8 and 4 are off, and 16, 2, and 1 are on. (*b*) Oscilloscope channel 1 displays a logic 1 (+4 ± 1 v dc) with no pulses. (*c*) Oscilloscope channel 2 displays a square wave whose period is approximately 0.6 msec. This square wave may not be perfectly stable. Adjust R80 for most stable square wave obtainable.

3-23. DDOW Test Troubleshooting Procedures

This paragraph contains the troubleshooting procedures for locating the faulty component(s) that produced the abnormal indication in the associated test procedures in paragraph 3-15. In table 3-25, locate the abnormal indication under the "Abnormal indication" column and then perform the associated troubleshooting listed under the "Action" column to isolate the malfunction.

Table 3-25. DDOW Test Troubleshooting Chart

No.	Abnormal indication	Action
1	RAU TTY CALL indicator did not light and TD-976/G audible ALARM horn did not sound (step 9).	*a.* Connect DMM to following RAU P1 test points on RAU feedthru box. (1) + lead to DDRG——. (2) − lead to DC GND. *b.* Observe DMM and set TTY SEND-OFF-RING switch to RING and then back to OFF. (1) If DMM indicated 0 ±0.5 v dc while switch was in RING, proceed to c below. (2) If DMM indicated +4.5 ±1 v dc while switch was in RING, replace RAU 21A15. *c.* Connect DMM to following RAU P1 test points on RAU feedthru box. (1) + lead to DDCALS. (2) − lead to DC GND. *d.* Set TTY SEND-OFF-RING switch to RING and then back to OFF. Observe DMM indication. (1) If DMM indicates +2 ±0.5 v dc, replace RAU 21A15. (2) If DMM indicates 0 ±0.5 v dc, perform following. (*a*) Replace DDOW encoder card 21A3. (*b*) Replace DDOW decoder card 21A8. (*c*) Replace TC (M) card 21A5. (*d*) Replace TC (D) card 21A5. (*e*) Replace MO/C card 21A4.
2	RAU TTY CALL indicator did not go out and TD-976/G audible ALARM horn did not stop sounding (step 10).	*a.* Connect DMM to following RAU P1 test points on RAU feedthru box. (1) + lead to DDSD—. (2) − lead to DC GND. *b.* Observe DMM and set TTY SEND-OFF-RING switch to SEND and then back to OFF. (1) If DMM indicated +4.5 ±1 v dc while switch was in SEND, replace RAU 21A15. (2) If DMM indicated 0 ±0.5 v dc while switch was in SEND, replace DDOW decoder card 21A8.
3	RAU TTY CALL indicator did not light and TD-976/G audible ALARM horn did not sound (step 11).	*a.* Connect DMM to following RAU P1 test points on RAU feedthru box. (1) + lead to DDRY—. (2) − lead to DC GND. *b.* Observe DMM and set TTY RCV-OFF-READY switch to READY and then back to OFF. (1) If DMM indicated 0 ±0.5 v dc while switch was in READY, replace DDOW encoder card 21A3. (2) If DMM indicated +4.5 ±1 v dc while switch was in READY, replace RAU 21A15.
4	RAU TTY CALL indicator did not go out and TD-976/G audible ALARM horn did not stop sounding (step 12).	Same as No. 2 above.
5	Waveform is incorrect (step 16).	*a.* If waveform is present with proper timing characteristics but amplitude is incorrect and/or waveform is distorted, replace RAU 21A15. *b.* If no waveform is displayed or timing characteristics of waveform are incorrect, perform following. (1) Replace DDOW encoder card 21A3. (2) Replace DDOW decoder card 21A8. (3) Replace RAU 21A15.
6	Waveform is incorrect (step 32).	*a.* If waveform is present with proper timing characteristics but amplitude is incorrect and/or waveform is distorted, replace DDOW decoder card 21A8. *b.* If no waveform is displayed or timing characteristics of

Table 3-25. DDOW Test Troubleshooting Chart—Continued

No.	Abnormal indication	Action
		waveform are incorrect, perform following. (1) Replace DDOW encoder card 21A3. (2) Replace DDOW decoder card 21A8. (3) Replace RAU 21A15.

Section V. MAINTENANCE OF MO/C CARD 21A4

3-24. Introduction

Maintenance of the MO/C card consists of a semiannual check of the output frequencies of the two oscillators on the MO/C card. The receiving and performance tests in section II also require these checks to be performed. When an oscillator frequency is out of tolerance, adjust that oscillator as instructed in paragraph 3-25.

3-25. Oscillator Checks and Adjustments

a. General. Perform the procedures in *b* below to check, and if necessary adjust, the output frequencies of the two oscillators. Use digital counter AN/USM-207A to check the oscillator frequencies. Use a nonmetallic alignment tool when adjusting an oscillator.

b. Check and Adjustment Procedure. The following procedures may be performed on a TD-976/G installed in a system configuration or on a TD-976/G connected in a test configuration.

(1) Remove TD-976/G front cover to expose plug-in cards.

(2) Ensure that ac power is applied to TD-976/G and that POWER SUPPLY switch is set to ON.

(3) Connect digital counter to TP4 (oscillator output) and TP1 (ground) on MO/C card 21A4. Observe digital counter for indication of 9,830,400 ± 50 Hz. If indication is correct, proceed to (7) below. If indication is incorrect, proceed to (4) below.

(4) Set POWER SUPPLY switch to OFF and remove MO/C card 21A4 approximately ¼ way out of card file. Remove screw cap from oscillator Y2 (located at top of card). Reseat MO/C card in card file. Set POWER SUPPLY switch to ON.

(5) Using nonmetallic alignment tool, carefully adjust Y2 for indication on digital counter of 9,830,400 ± 50 Hz. Remove tool from Y2 and observe that counter indication is still correct.

(6) Set POWER SUPPLY switch to OFF and remove MO/C card approximately ¼ way out of card file. Install screw cap on oscillator Y2. Reseat MO/C card in card file. Set POWER SUPPLY switch to ON.

(7) Disconnect digital counter and reconnect it to TP5 (oscillator output) and TP1 (ground) on MO/C card 21A4. Observe digital counter for indication of 4,608,000 ± 20 Hz. If indication is correct, proceed to (11) below. If indication is incorrect, proceed to (8) below.

(8) Set POWER SUPPLY switch to OFF and remove MO/C card 21A4 approximately ¼ way out of card file. Remove screw cap from oscillator Y1 (located at bottom of card). Reseat MO/C card in card file. Set POWER SUPPLY switch to ON.

(9) Using nonmetallic alignment tool, carefully adjust Y1 for indication of 4,608,000 ± 20 Hz on digital counter. Remove tool from Y1 and observe that counter indication is still correct.

(10) Set POWER SUPPLY switch to OFF and remove MO/C card approximately ¼ way out of card file. Install screw cap on oscillator Y1. Reseat MO/C card in card file. Set POWER SUPPLY switch to ON.

(11) Disconnect digital counter and install TD-976/G front cover.

Section VI. RAU TEST AND TROUBLESHOOTING PROCEDURES

3-26. Introduction

a. General. This section contains the RAU test and troubleshooting procedures. The test and troubleshooting procedures are combined in table 3-27. The procedures in table 3-27 are used as the receiving test, troubleshooting procedures, and final performance standards as described in *b* below.

b. Test and Troubleshooting Concept. The procedures in table 3-27 are performed as the receiving test on each RAU received from the user. The procedures are also performed as a receiving test on each RAU found to be faulty as part of the overall TD-976/G test and troubleshooting procedures in sections III and IV. As a receiving test, the procedures in table 3-27 are sequentially performed until an abnormal indication is obtained. For each potential abnormal indication, the table also contains the appropriate troubleshooting actions necessary to isolate the faulty component(s) as described in paragraph 3-27. When the RAU has been repaired, the procedures in table 3-27 must be performed as the performance standards.

3-27. Test and Troubleshooting Procedures

a. Test and Troubleshooting Requirements. Perform the procedures in table 3-27 on each RAU to detect the specific malfunction and then use the specific troubleshooting procedures in the same table to isolate the faulty component(s). After the faulty component(s) is located and the repair is accomplished, the procedures in table 3-27 are repeated as the performance standards. As the performance standards, all the procedures in the table must be performed without obtaining any abnormal indications.

b. Test and Troubleshooting Table Usage. Table 3-27 contains three columns. The contents and use of the information in each column is described in (1) through (3) below.

(1) *Step column.* This column lists the step sequence in which the procedures in the "Procedure/normal indication" column must be performed. As a receiving test, the steps are performed in sequence until an abnormal indication is obtained for a given step. At this time, the troubleshooting function is performed as described below. As a performance standards function, all the sequential steps must be performed without obtaining any abnormal indications.

(2) *Procedure/normal indication column.* This column contains the detailed instructions for setting controls on the equipment and making test connections; it also contains other pertinent information necessary to obtain the required test conditions. When applicable, the column also contains the normal indication(s) that should be produced for the given test condition. When the normal condition is not obtained for a given step, then the troubleshooting action is performed as directed in the "If indication is abnormal" column. The normal indication may be a voltage measurement, a waveform displayed on an oscilloscope, or the status (lit or out) of an equipment indicator.

(3) *If indication is abnormal column.* This column contains the appropriate troubleshooting actions used to locate the faulty condition that caused the abnormal indication in a given step. The troubleshooting actions listed in this column consist of parts substitution, continuity checks, and circuit analysis. The RAU wire run list and schematic diagram required to troubleshoot a faulty RAU are in this manual.

c. Test Equipment Required for Test and Troubleshooting. Table 3-26 lists the test equipment required for testing and troubleshooting the RAU.

d. Test and Troubleshooting Procedures. Perform the procedures in table 3-27 to test and troubleshoot a faulty RAU. When the faulty component(s) are located, perform the appropriate repair procedures as described in section VII. Repeat the procedures in table 3-27 on each repaired RAU as the performance standards. The RAU is ready to be returned to stock or to the user when all the procedures in table 3-27 are performed without obtaining any abnormal indications.

Table 3-26. Test Equipment Required for RAU Test and Troubleshooting

Test equipment	Qty	NSN or part No.
Cable assembly (Martin Marietta).	1	70730085-009
Cable assembly (Martin Marietta).	1	70730085-019
Digital multimeter (DMM).	1	6625-01-010-9255
Oscilloscope OS-261/U.	1	6625-00-127-0079
Pattern generator SG-1054/G.	1	6625-00-137-7738
Power supply PP-3135/U.	1	6625-00-635-7991
Power supply PP-3940A.	1	6130-00-460-2148
RAU breakout box (Martin Marietta).	1	70730020-009
Resistor (6800-ohm ± 5%, 5 watt)	2	None

Table 3-27. RAU Test and Troubleshooting

Step	Procedure/normal indication	If indication is abnormal
	INITIAL SETUP	
1	On RAU, set switches as follows: LAMP to OFF. TTY RCV-OFF-READY to OFF. TTY SEND-OFF-RING to OFF. VO ORDW CABLE to OFF. VO ORDW SYSTEM to OFF.	
2	On RAU breakout box, set switches as follows: INDICATOR SELECT to unused position (between FRAME and SYSTEM). INDICATOR to OFF. SWITCH SELECT to OFF.	

Table 3-27. RAU Test and Troubleshooting—Continued

<table>
<tr><th>Step</th><th>Procedure/normal indication</th><th>If indication is abnormal</th></tr>
<tr><td></td><td>CONTINUITY SELECT to OFF.
24 VDC POWER to OFF.</td><td></td></tr>
<tr><td>3</td><td>Connect test setup as shown in figure 3-10. Leave power supply PP-3940A turned off and set power supply voltage control for minimum (0-volt) output.</td><td></td></tr>
<tr><td colspan="3">INDICATOR CHECK</td></tr>
<tr><td>4</td><td>Turn on power supply PP-3940A and adjust for 24 v dc output (dial accuracy).</td><td></td></tr>
<tr><td>5</td><td>On RAU breakout box, set 24 VDC POWER switch to ON. Observe that 24 VDC POWER DC ON indicator lights.</td><td>RAU breakout box is defective; refer problem to appropriate maintenance personnel.</td></tr>
<tr><td>6</td><td>On RAU, set LAMP switch to ON. Verify that all RAU indicators (LED's) are out.</td><td>If any indicator is lit, its associated steering diode is open. Replace steering diode (fig. FO-19). (All steering diodes are forward biased by RAU breakout box.)</td></tr>
<tr><td>7</td><td>On RAU breakout box, set INDICATOR switch to ON.</td><td></td></tr>
<tr><td>8</td><td>On RAU breakout box, sequentially rotate INDICATOR SELECT switch clockwise and perform following at each switch position.
<i>a.</i> Verify that RAU indicator corresponding to switch position lights.
<i>b.</i> On RAU, set LAMP switch to OFF and verify that indicator is now out. Set LAMP switch back to ON and proceed to next position of INDICATOR SELECT switch.</td><td><i>a.</i> If any indicator fails to light, replace that indicator and/or its associated resistor (fig. FO-19).
<i>b.</i> If any indicator fails to go out, its associated steering diode is shorted. Replace steering diode (fig. FO-19).</td></tr>
<tr><td>9</td><td>On RAU, set LAMP switch to OFF.</td><td></td></tr>
<tr><td>10</td><td>On RAU breakout box, set INDICATOR switch to OFF.</td><td></td></tr>
<tr><td colspan="3">SWITCH CHECK</td></tr>
<tr><td>11</td><td>Sequentially rotate SWITCH SELECT switch to below listed positions. At each position, set corresponding RAU switch to position listed and verify that SWITCH STATUS indicator on RAU breakout box lights. Then return that RAU switch back to OFF.
<table>
<tr><th><i>SWITCH SELECT position</i></th><th><i>RAU switch position</i></th></tr>
<tr><td>TTY RDY</td><td>TTY RCV-OFF-READY to READY</td></tr>
<tr><td>TTY RCV</td><td>TTY RCV-OFF-READY to RCV</td></tr>
<tr><td>TTY RING</td><td>TTY SEND-OFF-RING to RING</td></tr>
<tr><td>TTY SEND</td><td>TTY SEND-OFF-RING to SEND</td></tr>
<tr><td>CABLE OW RING</td><td>VO ORDW CABLE TO RING</td></tr>
<tr><td>CABLE OW T/L</td><td>VO ORDW CABLE to T/L</td></tr>
<tr><td>CABLE OW T/L (RMIC)</td><td>VO ORDW CABLE to T/L</td></tr>
<tr><td>SYS OW RING</td><td>VO ORDW SYSTEM to RING</td></tr>
<tr><td>SYS OW T/L</td><td>VO ORDW SYSTEM to T/L</td></tr>
<tr><td>SYS OW T/L (RMIC)</td><td>VO ORDW SYSTEM to T/L</td></tr>
</table></td><td>If SWITCH STATUS indicator fails to light for any SWITCH SELECT position, trouble is the particular RAU switch or its associated wiring. Refer to RAU wire run list (table 3-29) and RAU schematic (fig. FO-19).</td></tr>
<tr><td>12</td><td>On RAU breakout box, set SWITCH SELECT switch to LAMP TEST.</td><td></td></tr>
<tr><td>13</td><td>On RAU, hold LAMP switch to TEST and verify that SWITCH LAMP TEST indicator on RAU breakout box lights. Release RAU LAMP switch.</td><td>If SWITCH LAMP TEST indicator faued to light, trouble is RAU LAMP switch or its associated wiring. Refer to RAU wire run list (table 3-29) and RAU schematic (fig. FO-19).</td></tr>
<tr><td>14</td><td>On RAU breakout box, set SWITCH SELECT switch to OFF.</td><td></td></tr>
<tr><td colspan="3">CONTINUITY AND RESISTANCE CHECK</td></tr>
<tr><td>15</td><td>On RAU breakout box, sequentially rotate CONTINUITY SELECT switch to each of its 12 designated positions. Verify that CONTINUITY STATUS indicator lights for each designated switch position.</td><td>If CONTINUITY STATUS indicator fails to light for any switch position, trouble is RAU wiring. Refer to RAU wire run list (table 3-29) and RAU schematic (fig. FO-19).</td></tr>
<tr><td>16</td><td>On RAU breakout box, set CONTINUITY SELECT switch to OFF.</td><td></td></tr>
<tr><td>17</td><td>On RAU breakout box, disconnect P4 and P5 from DGTL VO XMT and DGTL VO RCV receptacles of RAU.</td><td></td></tr>
<tr><td>18</td><td>On RAU breakout box, connect DMM to DGTL VO RES XMT test points. DMM indicates 620 ± 93 ohms.</td><td>Replace resistor R1 (fig. FO-19).</td></tr>
</table>

Table 3-27. RAU Test and Troubleshooting—Continued

Step	Procedure/normal indication	If indication is abnormal
19	On RAU breakout box, connect DMM to DGTL VO RES RCV test points. DMM indicates 620 ± 124 ohms.	Replace resistor R2 (fig. FO-19).
20	Turn off test equipment, disconnect test setup, and proceed to 75-baud digital data check (step 21).	
	75-BAUD DIGITAL DATA CHECK	
21	On RAU, remove six screws and washers securing RAU cover. Remove cover and set cover aside.	
22	On RAU circuit card, install jumper switches P1 through P4 to interconnect sockets marked A and B.	
23	On RAU, set switches as follows: LAMP to OFF. TTY RCV-OFF-READY to OFF. TTY SEND-OFF-RING to OFF. VO ORDW CABLE to OFF. VO ORDW SYSTEM to OFF.	
24	On RAU breakout box, set switches as follows: INDICATOR SELECT to unused position (between FRAME and SYSTEM) INDICATOR to OFF. SWITCH SELECT to OFF. CONTINUITY SELECT to OFF. DIGITAL DATA to 75. 24 VDC POWER to OFF.	

WARNING

Potentials in excess of 130 v dc are applied to the RAU and interconnecting cables and test leads during the 75-baud digital data check. Exercise caution when making tests and measurements.

CAUTION

Do not turn on any test equipment until directed to do so in following procedures.

When connecting oscilloscope to ac power source, use appropriate adapter to isolate oscilloscope case from power source neutral line.

Step	Procedure/normal indication	If indication is abnormal
25	Connect test setup as shown in figure 3-11. Leave power supplies turned off and set power supply voltage controls for minimum (0-volt) output.	
26	Turn on power supply PP-3940A and adjust for 24 v dc output (dial accuracy).	
27	On RAU breakout box, set 24 VDC POWER switch to ON. Observe that 24 VDC POWER indicator lights.	RAU breakout box is defective; refer problem to appropriate maintenance personnel.
28	On pattern generator, set controls as follows: Set up SELECTED CHARACTERS 1 pushbuttons for letter Y (depress BITS 1, 3, and 5 pushbuttons to program letter Y). Depress CHARACTER SEQUENCE LENGTH pushbutton 1. PATTERN to SELECTED CHARACTERS CODE LEVEL 5. DISTORTION PERCENT to 0. DISTORTION TYPE to OFF. BIT RATE to A and 75. MODE (left switch) to FREE RUN. MODE (right switch) to START/STOP UNIT STOP MARK 1.5. OUTPUTS HI-LEVEL SELECT to NEUT. CR/LF to OUT (switch located on generator rear panel).	
29	Turn on power supply PP-3135/U and adjust for + 130 v dc output (dial accuracy).	
30	Turn on oscilloscope and pattern generator. Set oscilloscope for internal negative-going trigger mode.	
31	Observe oscilloscope for waveform as shown in A of figure 3-9.	*a.* On RAU breakout box, verify that DIGITAL DATA 75 BAUD indicator is blinking. *b.* If indicator is not blinking, check Q4, R31, and associated parts (fig. FO-19). *c.* If indicator is blinking, check Q1, Q2, Q3, Q5, and associated parts (fig. FO-19).

Table 3-27. *RAU Test and Troubleshooting—Continued*

Step	Procedure/normal indication	If indication is abnormal
32	Adjust power supply PP-3135/U for minimum output and then turn power supply off.	
33	Turn power supply PP-3940A off.	
34	Turn off all test equipment, disconnect test setup, and proceed to 1200-baud loop test (step 35).	
	1200-BAUD LOOP TEST	
35	On RAU circuit card, install jumper switches P1 through P4 to interconnect sockets marked A and C.	
36	On RAU, set switches as follows: LAMP to OFF. TTY RCV-OFF-READY to OFF. TTY SEND-OFF-RING to OFF. VO ORDW CABLE to OFF. VO ORDW SYSTEM to OFF.	
37	On RAU breakout box, set switches as follows: INDICATOR SELECT to unused position (between FRAME and SYSTEM) INDICATOR to OFF. SWITCH SELECT to OFF. CONTINUITY SELECT to OFF. DIGITAL DATA to 1200. 24 VDC POWER to OFF.	
38	Connect test setup as shown in figure 3-12. Leave power supply PP-3940A turned off and set power supply voltage control for minimum (0-volt) output).	
39	Turn on DMM and power supply PP-3940A. Adjust power supply for 5v dc output (dial accuracy).	
40	Verify that DIGITAL DATA 1200 BAUD indicator on RAU breakout box lights and DMM indicates +5 ± 0.5 v dc.	*a.* If voltage is missing, troubleshoot RAU wiring. Refer to RAU wire run list (table 3-29) and RAU schematic (fig. FO-19). *b.* If voltage is correct but DIGITAL DATA 1200 BAUD indicator does not light, RAU breakout box is defective. Refer problem to appropriate maintenance personnel.
41	Turn off all test equipment and disconnect test setup.	
42	Install RAU cover removed in step 21.	
43	End of test. RAU test and troubleshooting procedure is complete.	

Section VII. MAINTENANCE OF RAU 21A15

3-28. Introduction

This section contains the procedures for repairing a faulty RAU. The repair procedures consist of replacing faulty components mounted on the RAU front panel or faulty components mounted on the circuit card.

3-29. Repair Procedures

a. General. The tools required to perform the repair procedures are listed in *b* below. The repair procedures for replacing a component mounted on the front panel are in *c* below and the repair procedures for replacing a component mounted on the circuit card are in *d* below. When replacing components or wiring, use appropriate heat-shrink insulation sleeving as was installed on wiring or component being replaced.

b. Tools Required for RAU Repair. Tool kit TK-105/G contains the tools necessary to disassemble and assemble the RAU. Bench top repair center PRC-150A contains the tools and equipment necessary to repair the circuit card as directed in *d* below.

c. Panel-Mounted Components. Perform the following procedures to replace a component mounted on the RAU front panel. Locations of panel-mounted components are shown in figure 3-13.

(1) Remove six cover mounting screws and then remove cover from RAU.

(2) Use standard replacement procedures to replace components on RAU front panel. Replacement of indicator DS1, DS2, or DS3 is unique in that associated mounting clip and retaining ring (fig. 3-14) are replaced each time the LED is replaced. Perform the following steps to replace a faulty LED.

(a) Cut and trim away insulation sleeving to expose area where wires are soldered to LED.

(b) Cut or unsolder wires to LED.

(c) Cut and remove retaining ring.

(d) Remove LED and then remove clip.

(e) Install replacement clip and then install replacement LED into clip from rear side of panel.

(f) Install replacement retaining ring.

(g) Install short lengths of insulating sleeving M23053/5-104-9 over wires to be resoldered to replacement LED. Length of insulation sleeving must be such that it will extend past solder joint after sleeving is positioned over solder joint and against base of LED.

(h) Strip, trim, and form wires and LED leads into J hooks. Solder wires to leads of replacement LED and then slide insulation sleeving over solder joint and against base of LED. Insulation sleeving must extend past solder joint and at least 3/8 inch past edge of retaining ring. Use portable source of forced hot air to shrink sleeving.

(i) Use MIL-A-46146, Type I adhesive sealant and fill in around LED leads in retaining ring.

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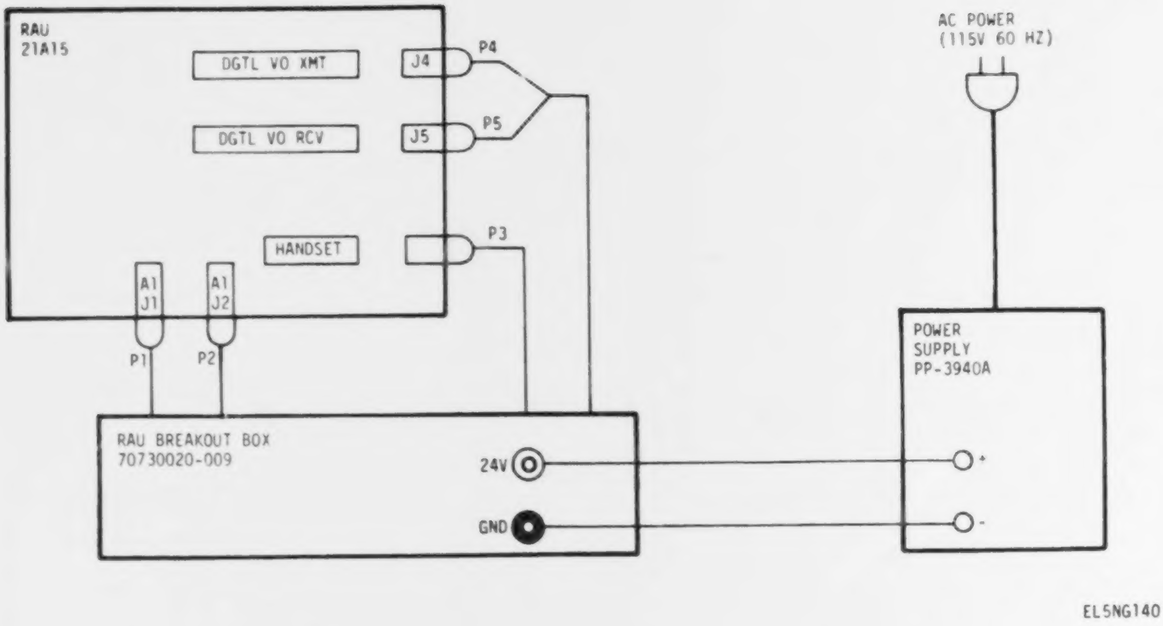


Figure 3-10. RAU indicator, switch, and continuity test setup.

Sealant is to extend along both LED leads, full circle, and for at least 1/4 inch past edge of retaining ring.

(3) Place cover on RAU and attach cover to RAU, using cover mounting screws removed in (1) above.

d. Circuit Card Components. Perform the following procedures to replace a component mounted on the circuit card. Locations of components on the circuit card are shown in figure 3-15.

(1) If installed, remove cover from RAU by removing six cover mounting screws.

(2) Access to components on the circuit card is available with the circuit card installed. To gain access to components on attached diode printed wiring board, remove four card mounting screws (fig. 3-13) holding circuit card to two mounting posts. Then lift circuit card from RAU.

(3) Replace faulty component as directed in the printed circuit board repair procedures in section X. Ensure that replacement component is oriented same as removed component.

(4) If necessary, attach circuit board to RAU, using screws removed in (2) above.

(5) Attach cover to RAU, using screws removed in (1) above.

Section VIII. MAINTENANCE OF FRONT COVER, FRONT PANEL, AND CASE

3-30. Introduction

This section contains the procedures for repairing the front cover, front panel, and case. The procedures in this section are listed below.

a. Front cover repair procedures are in paragraph 3-31.

b. Front panel removal and installation procedures are in paragraph 3-32.

c. Front panel repair procedures are in paragraph 3-33.

d. Case gasket replacement procedures are in paragraph 3-34.

e. Case locking insert replacement procedures are in paragraph 3-35.

f. Case handle replacement procedures are listed below.

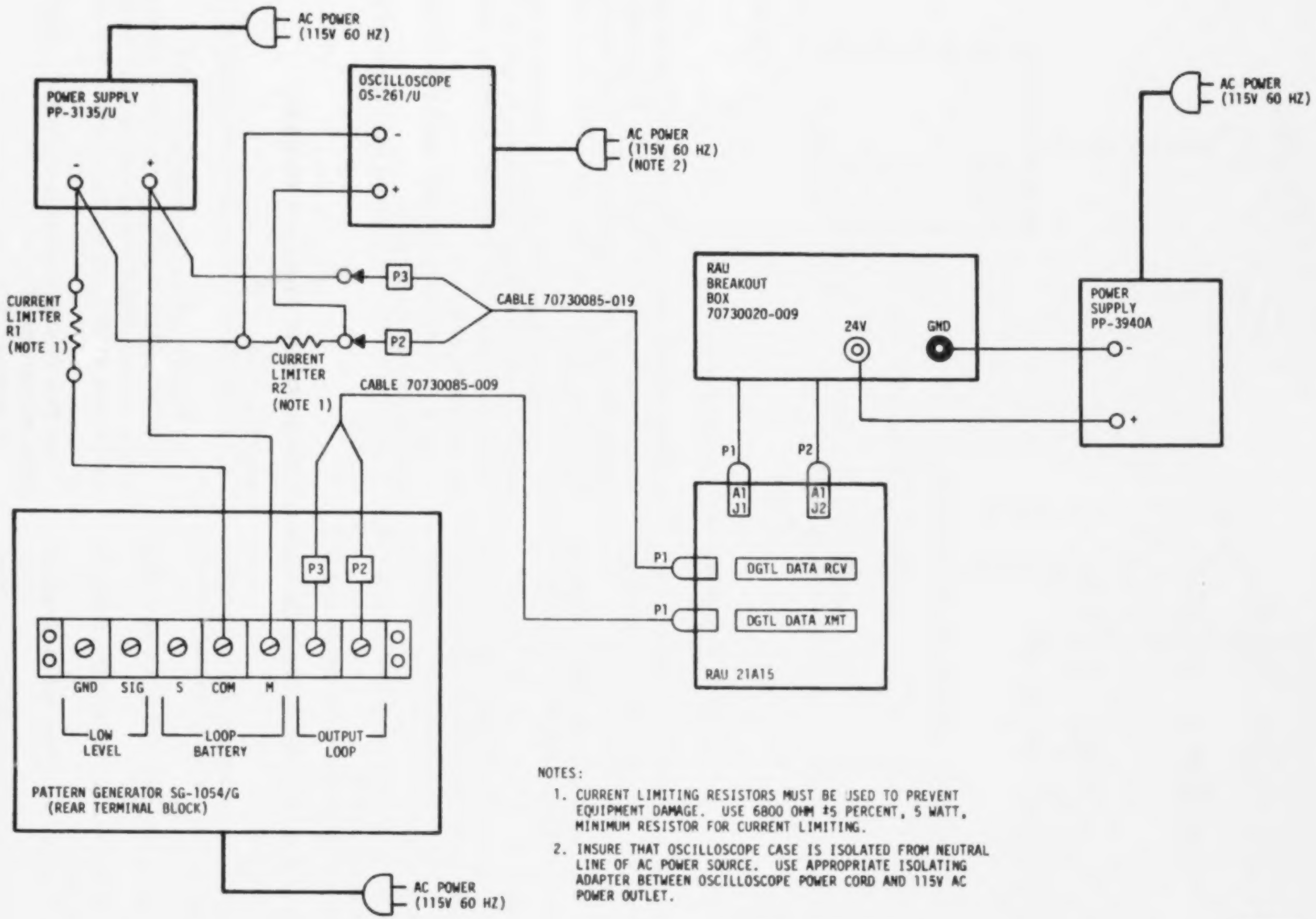
(1) Remove card file from case (para 3-37*a*).

(2) Centerpunch middle of rivet heads securing handle to case. When centerpunching rivet heads, place a solid metal object against the other end of rivet.

(3) Drill through each rivet, using a No. 9 drill 5133-00-189-9254.

(4) Remove handle.

(5) Install new handle SM-A-942099 with five rivets MS20426DD6-9.


AC POWER (115V 60 HZ)
POWER SUPPLY PP-3135/U
-
+
OSCILLOSCOPE OS-261/U
-
+
AC POWER (115V 60 HZ) (NOTE 2)
AC POWER (115V 60 HZ)
CURRENT LIMITER R1 (NOTE 1)
P3
P2
CABLE 70730085-019
CURRENT LIMITER R2 (NOTE 1)
CABLE 70730085-009
RAU BREAKOUT BOX 70730020-009
24V
GND
POWER SUPPLY PP-3940A
-
+
P1
P2
A1 J1
A1 J2
P1
P1
DGTL DATA RCV
DGTL DATA XMT
RAU 21A15
P3
P2
GND
SIG
S
COM
M
LOW LEVEL
LOOP BATTERY
OUTPUT LOOP
PATTERN GENERATOR SG-1054/G (REAR TERMINAL BLOCK)
AC POWER (115V 60 HZ)
EL5NG141

NOTES:

1. CURRENT LIMITING RESISTORS MUST BE USED TO PREVENT EQUIPMENT DAMAGE. USE 6800 OHM ±5 PERCENT, 5 WATT, MINIMUM RESISTOR FOR CURRENT LIMITING.
2. INSURE THAT OSCILLOSCOPE CASE IS ISOLATED FROM NEUTRAL LINE OF AC POWER SOURCE. USE APPROPRIATE ISOLATING ADAPTER BETWEEN OSCILLOSCOPE POWER CORD AND 115V AC POWER OUTLET.

Figure 3-11. 75-baud digital data check test setup.

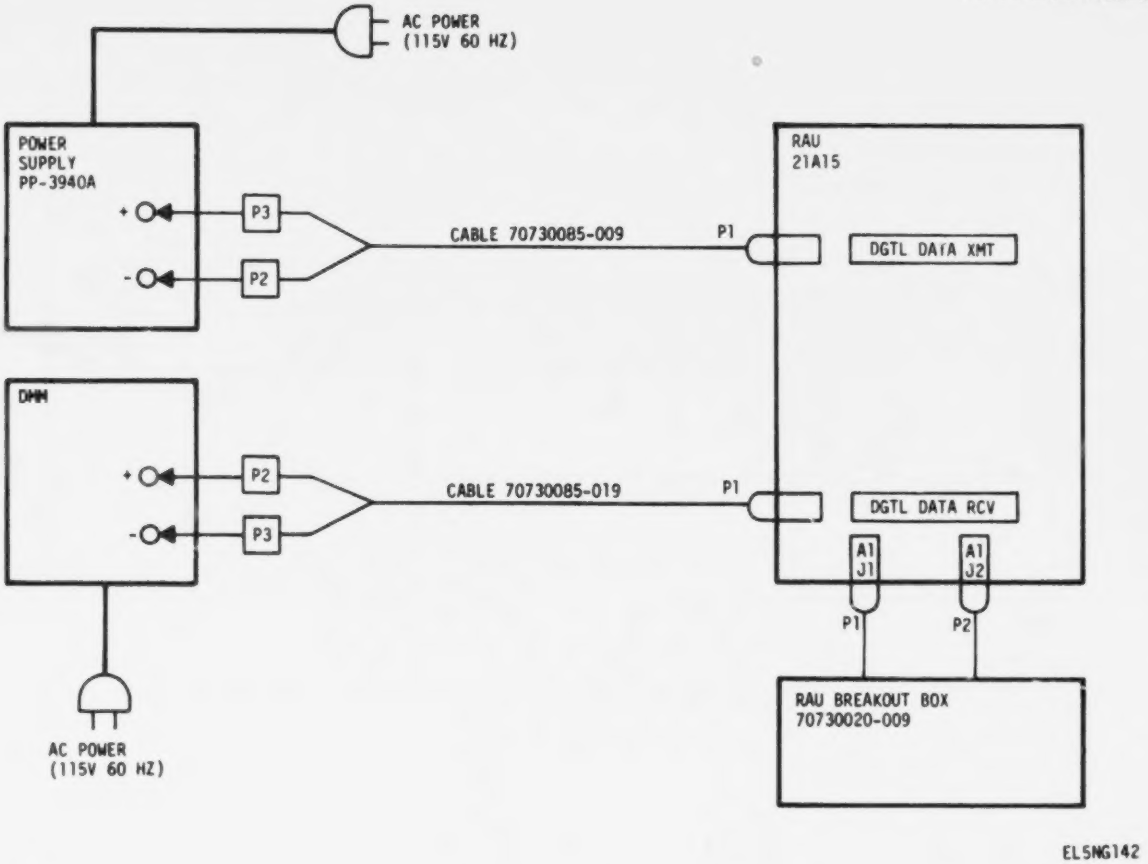


Figure 3-12. 1200-baud loop test setup.

(6) Place a solid metal object against rivet head. Use smooth end of ball peen hammer to upset other end of rivet. Repeat for other four rivets.

(7) Paint required areas of case exterior, including replaced handle, as follows. Use general instructions in TB 43-0118.

(a) Apply primer per TT-P-1757 to case exterior and primer per TT-P-636 to handle. Do not apply primer to rubber grip of handle.

(b) Apply forest green, lusterless paint per MIL-E-52835 over primer.

(8) Install card file in case (para 3-37*b*).

3-31. Front Cover Repair

a. General. Repair of the front cover consists of replacing a faulty retaining pad, shielding gasket, jack cover, or door assembly. The tools required to repair the front cover are given in *b* below. The procedures for replacing a retaining pad are in *c* below. The procedures for replacing the jack cover on the CABLE MILES access opening on the front cover are in *d* below. The replacement procedures for the shielding gasket are in *e* below. The procedures for replacement of the door assembly are in *f* below.

b. Tools Required for Front Cover Repair. Electrical equipment tool kits TK-100/G and TK-105/G contain the tools required to remove and install components on the front cover.

c. Retaining Pad Replacement Procedures. There are three retaining pads on the rear of the front cover as shown in figure 3-16. The part numbers for the three preformed retaining pads are listed on figure 3-16. Perform the following procedures to replace any one of the three pads.

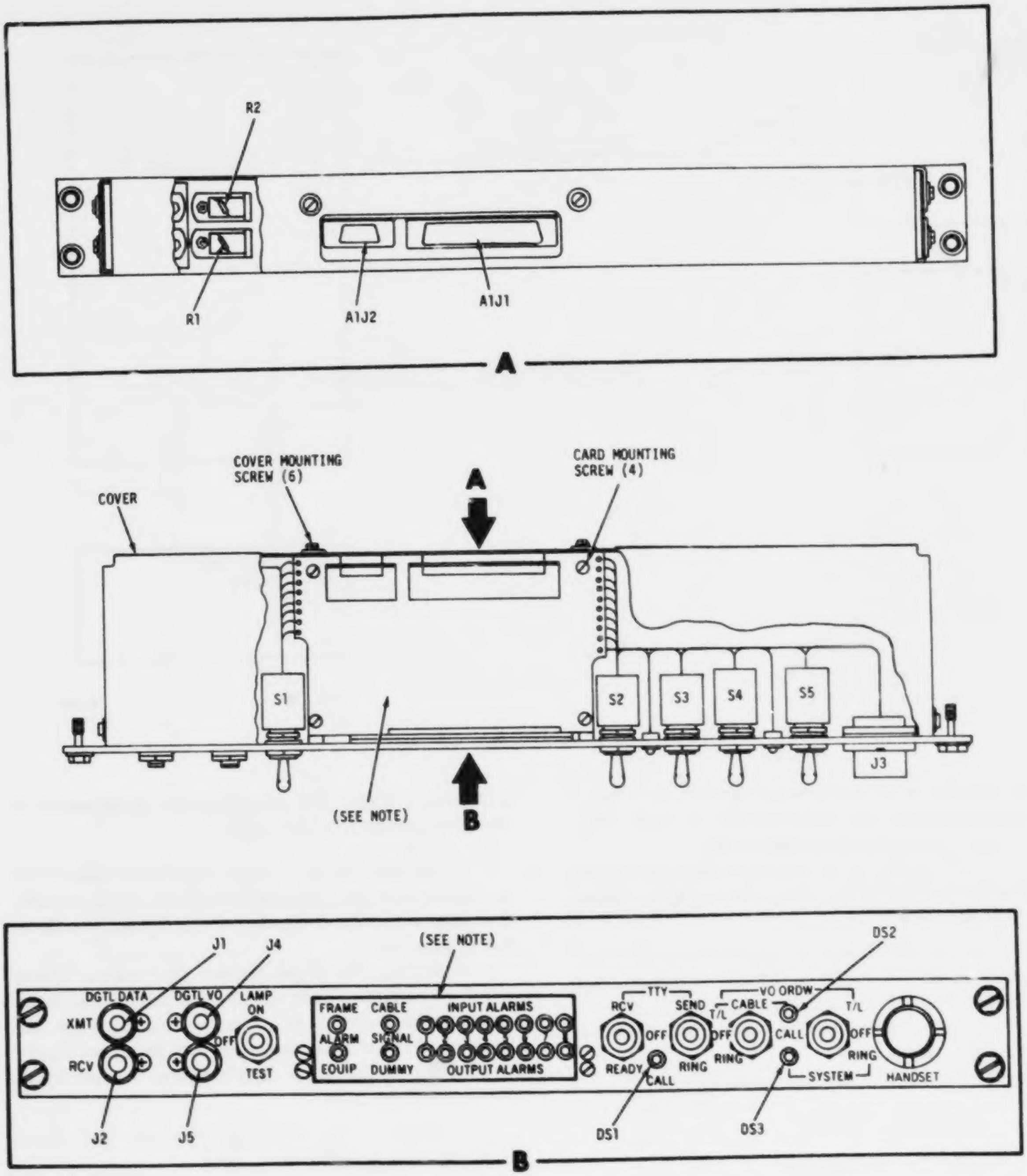
(1) Remove pad from front cover and clean bonding surfaces on cover.

(2) Apply MIL-A-46146, Type I, primer to bonding surface on cover.

(3) After primer is dry, apply a thin coat of MIL-A-46146, Type II, adhesive to surface of replacement pad that mates with cover.

(4) Carefully install pad on cover and remove any excess adhesive from cover immediately.

(5) Allow adhesive to cure before installing cover on case.


R2
R1
A1J2
A1J1
A
COVER
COVER MOUNTING SCREW (6)
A
CARD MOUNTING SCREW (4)
S1
S2
S3
S4
S5
J3
(SEE NOTE)
B
J1
J4
(SEE NOTE)
DS2
DGTL DATA
XMT
RCV
DGTL VO
OFF
LAMP ON
TEST
FRAME
ALARM
EQUIP
CABLE
SIGNAL
DUMMY
INPUT ALARMS
OUTPUT ALARMS
TTY
RCV
OFF
READY
CALL
SEND
RING
VO ORDW
CABLE
T/L
OFF
RING
CALL
T/L
OFF
RING
SYSTEM
HANDSET
J2
J5
DS1
DS3
B

NOTE:
SEE RAU CIRCUIT CARD COMPONENT LOCATION DIAGRAM FOR IDENTIFICATION OF COMPONENTS.

EL5NG108

Figure 3-13. RAU 21A15, component location diagram.

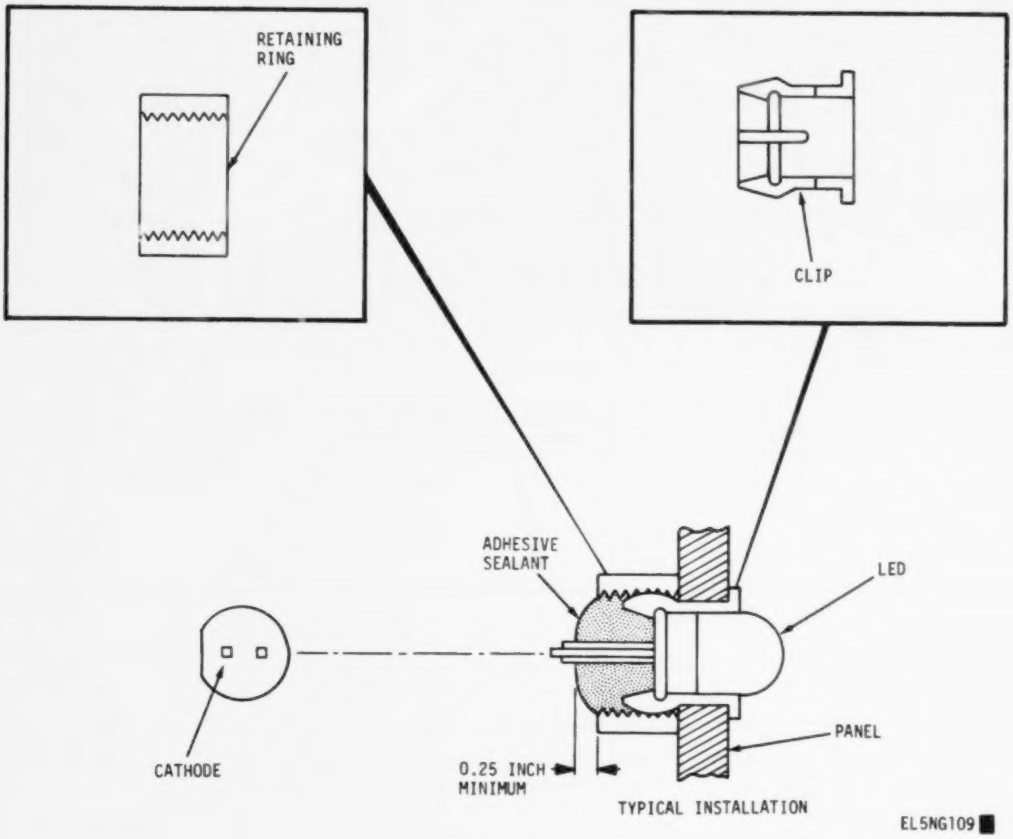

RETAINING RING
CLIP
ADHESIVE SEALANT
LED
CATHODE
PANEL
0.25 INCH MINIMUM
TYPICAL INSTALLATION
EL5NG109

Figure 3-14. RAU 21A15, DS1, DS2, and DS3 installation diagram.

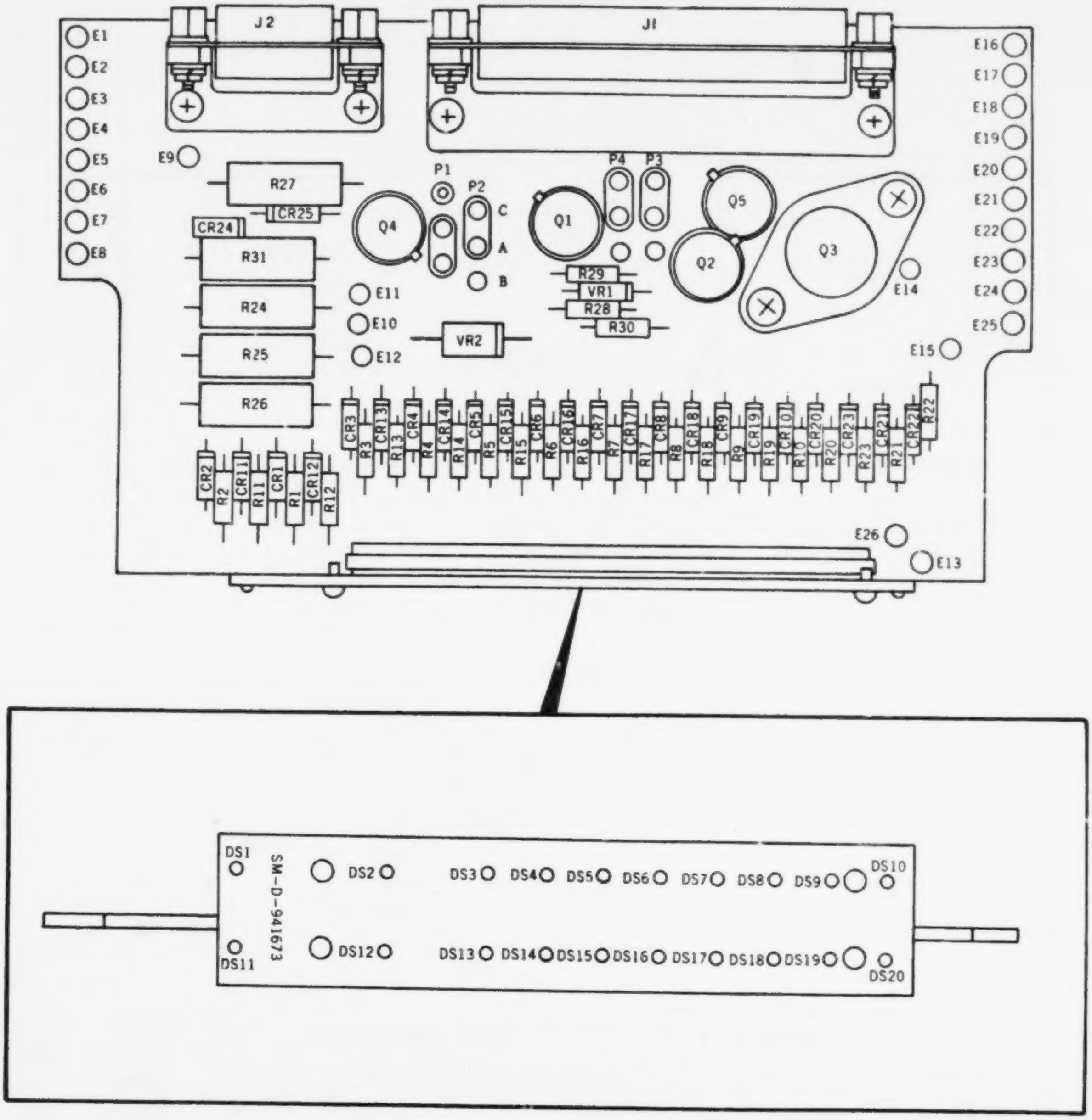
d. Jack (CABLE MILES) Cover Replacement Procedures. There are no special tools or procedures required to remove or install the jack cover. Install replacement jack cover to front cover, using panel bushing and packing with retainer (sealing washer).

e. Gasket Replacement Procedures. Perform the following procedures to replace the shielding gasket mounted behind the door on the front panel as shown in figure 3-17. The gasket is solid silicone rubber containing silvered particles that conform to MIL-R-5847, Class III, Grade 40 or ZZ-R-765, color gray. The gasket is cut and shaped as directed in the following steps.

(1) Remove faulty gasket material from channel in front cover. Clean bonding surface (bottom of channel) in cover.

(2) Ensure that side surfaces of channel are clean.

(3) Cut gasket material to fit in channel. Ensure that ends of gasket mate diagonally as shown in figure 3-17.


J2
J1
E1
E2
E3
E4
E5
E6
E7
E8
E9
E16
E17
E18
E19
E20
E21
E22
E23
E24
E25
R27
CR25
CR24
R31
R24
R25
R26
P1
P2
C
A
B
Q4
Q1
P4
P3
Q5
Q2
Q3
R29
VR1
R28
R30
E11
E10
E12
VR2
E14
E15
CR2
R2
CR11
R11
CR1
R1
CR12
R12
CR3
R3
CR13
R13
CR4
R4
CR14
R14
CR5
R5
CR15
R15
CR6
R6
CR16
R16
CR7
R7
CR17
R17
CR8
R8
CR18
R18
CR9
R9
CR19
R19
CR10
R10
CR20
R20
CR23
R23
CR21
R21
CR22
R22
E26
E13
DS1
SM-D-941673
DS2
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
DS11
DS12
DS13
DS14
DS15
DS16
DS17
DS18
DS19
DS20

EL5NG110

Figure 3-15. RAU circuit card 21A15A1, component location diagram.

CAUTION

Do not coat side surfaces of channel with adhesive or primer that could eliminate or restrict EMI filtering capability.

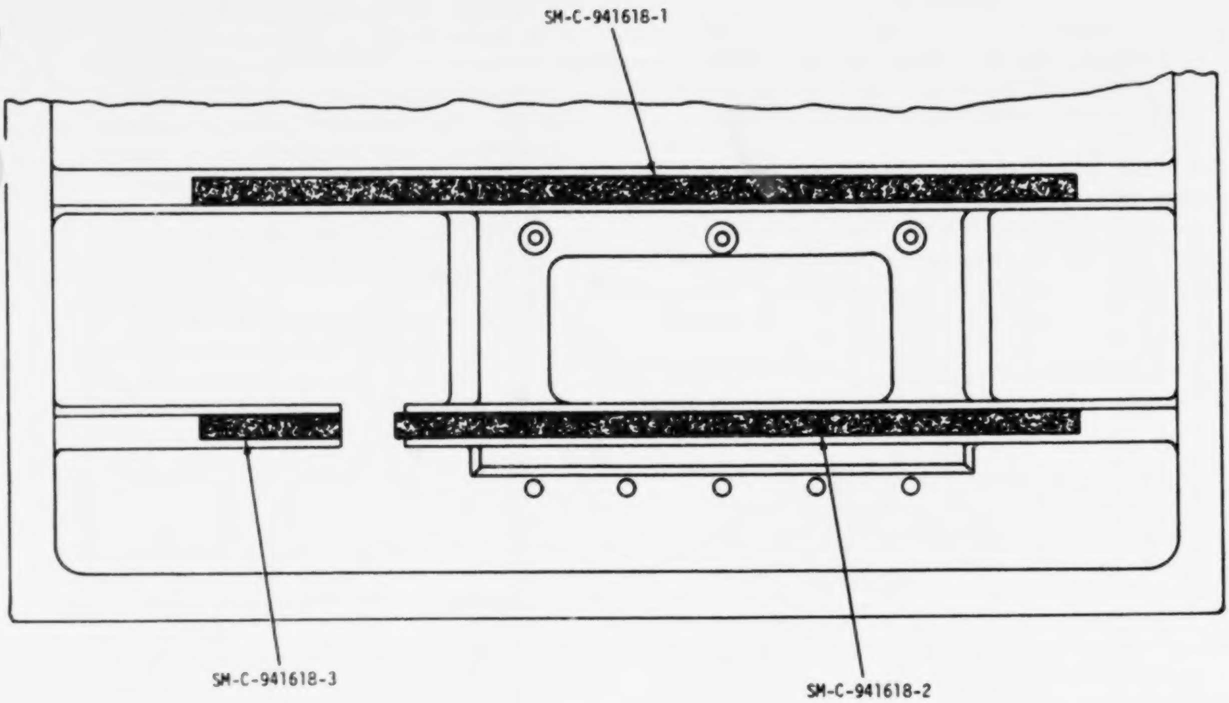
(4) Apply MIL-A-46146, Type I, primer to bottom surface of channel.

(5) After primer is dry, apply a thin coat of MIL-A-46146, Type II, adhesive to bottom of channel. Coat diagonal ends of gasket with adhesive.

(6) Carefully install gasket in channel. Ensure that adhesive does not coat side surfaces of channel.

f. Door Assembly Replacement Procedures. Perform the following procedures to replace the door assembly on the front cover.

(1) Centerpunch middle of rivet heads securing door hinge to front cover. When centerpunching rivet



DIMENSIONS: (REFERENCE ONLY)

PART NO.	LENGTH (IN INCHES)	THICKNESS (IN INCHES)
SM-C-941618-1	12.38	0.38 X 0.38
SM-C-941618-2	9.62	0.38 X 0.38
SM-C-941618-3	2.00	0.38 X 0.38

EL5NG112

Figure 3-16. Front cover, retaining pad installation diagram.

heads, place a solid metal object against other end of rivet.

(2) Drill through each rivet, using a No. 30 drill 5133-00-189-9275.

(3) Remove door assembly.

(4) Install new door assembly SM-D-941617 with five rivets MS20426AD4-5. Apply primer per TT-P-1757 to mating surfaces of rivets.

(5) Place a solid metal object against rivet head. Use smooth end of ball peen hammer to upset other end of rivet. Repeat for other four rivets.

(6) Paint required areas of door assembly and front cover as follows. Use general instructions in TB 43-0118.

(*a*) Apply primer per TT-P-1757.

(*b*) Apply gray, semigloss enamel per MIL-E-15090, class 2, color per FED-STD-595, number 26307.

3-32. Front Panel Removal and Installation Procedures

WARNINGS

- High voltage that can cause death or serious injury is present in the TD-976/G.

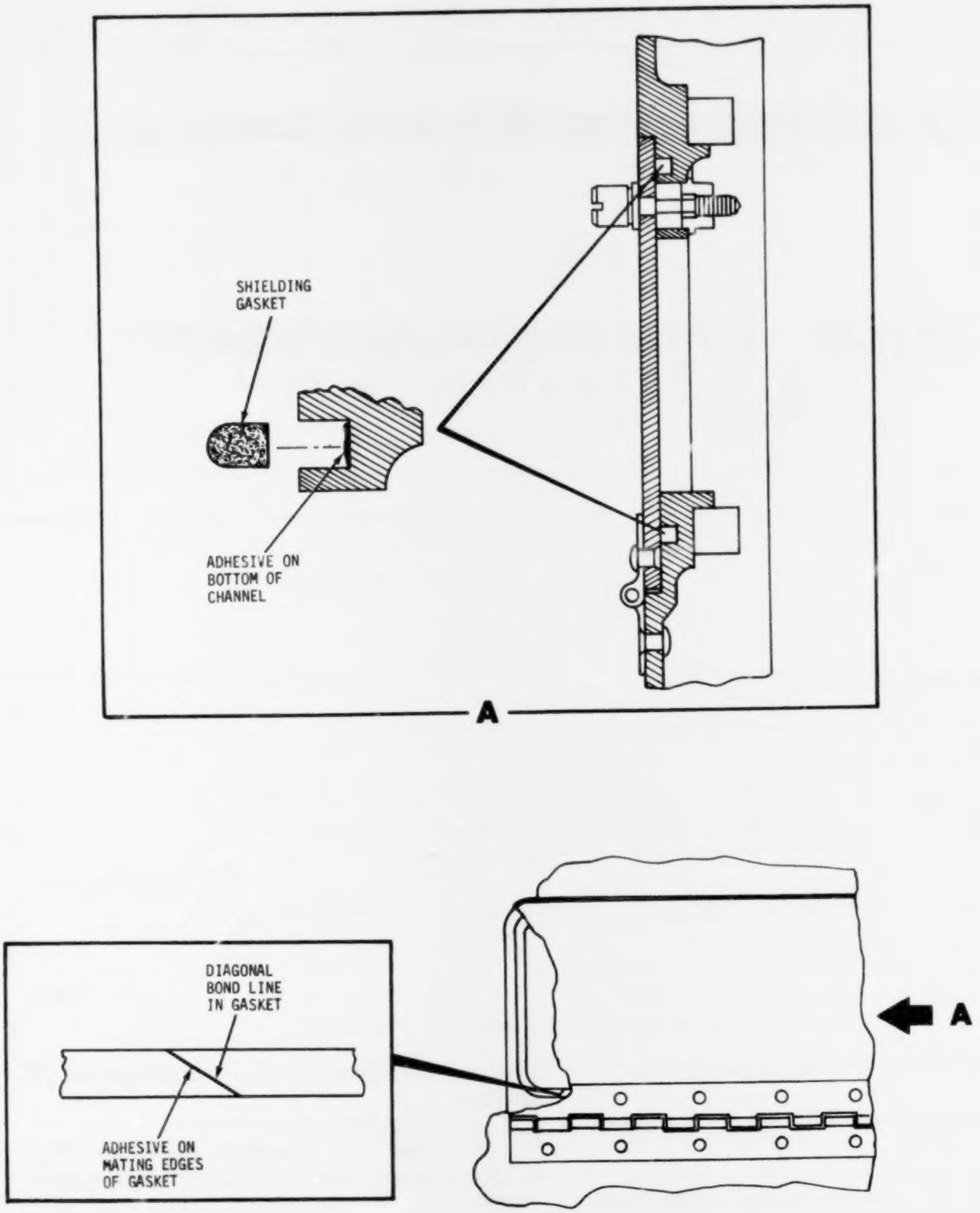

SHIELDING
GASKET
ADHESIVE ON
BOTTOM OF
CHANNEL
A
DIAGONAL
BOND LINE
IN GASKET
ADHESIVE ON
MATING EDGES
OF GASKET
A
EL5NG113

Figure 3-17. Front cover, gasket installation diagram.

- The 115-volt ac primary power is always applied to TB1 in the card file and to switch S9 on the front panel when the power cable is connected between the ac power source and the TD-976/G.
- Cable drive power of 400 volts dc with a constant current of 45 milliamperes may be present in the equipment when the POWER IN and/or POWER OUT indicator is lit. The high voltage can be generated within the unit or the cable power may be applied from another TD-976/G that is connected to the unit being serviced.
- Wait at least 10 seconds after cable power is removed from the TD-976/G before working on equipment to ensure that high-voltage capacitors in the unit are discharged.

a. Removal Procedures. Perform the following procedures to remove the front panel from the case. Limited access to components on the rear of the front panel can be obtained without disconnecting the front panel connectors that are connected to the case and the card file. To gain access to the rear of the front panel without disconnecting the connectors, perform (1) and (11) below.

(1) Set POWER SUPPLY and POWER CABLE switches to OFF. Ensure that POWER IN and POWER OUT indicators are out.

(2) Disconnect power cable from POWER IN connector J26 on rear of TD-976/G.

NOTE

When one of gaskets mounted on case is damaged, replace gasket (para 3-34).

(3) Remove front cover, if installed, by loosening 16 captive screws. Inspect front cover gasket (fig. 3-18, item 18) on case for damage.

(4) Remove top cover, if installed, by loosening 12 captive screws. Inspect top cover gasket (fig. 3-18, item 20) or case for damage.

(5) Remove RAU, if installed, by loosening four captive screws.

(6) Loosen 12 captive screws on power supply and then remove power supply from case. Inspect power supply gasket (fig. 3-18, item 21) on case for damage.

(7) Remove two sets of screws, washers, and nuts (fig. 3-18, items 4 through 7) securing connector 21A14J3 to case.

(8) Remove three plug-in cards from each end of card file to allow access to front panel connectors 21A14P1 and 21A14P2 that are connected to card file.

(9) Remove screws, washers, and nuts (fig. 3-18, items 9 through 12) securing clamps (fig. 3-18, item 8) to bracket and case. Leave clamps around wiring harness.

(10) Loosen captive screws on front panel connectors 21A14P1 and 21A14P2 (fig. 3-18, items 13 and 14) and then disconnect 21A14P1 and 21A14P2 from card file connectors.

CAUTION

When performing (11) below, ensure that front panel connectors 21A14P1, 21A14P2, and 21A14J3 are clear of card file to prevent possible damage to connectors and associated wiring.

(11) Loosen 14 captive screws on front panel and then carefully lift front panel from case. If front panel connectors have not been disconnected, front panel can be removed only to the extent allowed by the service loop in the front panel harness. Inspect front panel gasket (fig. 3-18, item 19) for damage.

b. Installation Procedures. Perform the following procedures to install a front panel in the case. It is assumed that the top cover, RAU, power supply, and front cover are not installed on the case.

CAUTION

When performing (1) below, ensure that front panel connectors 21A14J3, 21A14P1, and 21A14P2 are clear of card file to prevent possible damage to connectors and associated wiring.

(1) Carefully position front panel and three connectors (fig. 3-18, items 1, 3, 13, 14) in case. Secure front panel to case, using front panel captive screws.

(2) Secure connector 21A14J3 to case, using two sets of screws, washers, and nuts (fig. 3-8, items 4 through 7).

(3) Using two captive screws on each connector, secure connectors 21A14P1 and 21A14P2 (fig. 3-18, items 13 and 14) to card file connectors.

(4) Secure two clamps (fig. 3-18, item 8) with screws, washers, and nuts (fig. 3-18, items 9 through 12).

(5) Carefully slide power supply into case, engaging guide pins in mating connector. Using hands, firmly press power supply so as to engage its connector with mating connector. Secure power supply to case, using power supply captive screws.

(6) Install plug-in cards removed from card file in *a*(8) above.

NOTE

Do not perform (7) through (9) below if additional TD-976/G testing is to be performed.

(7) Install RAU in top of case, using captive screws on RAU.

(8) Install top cover on case, using captive screws in cover.

(9) Install front cover on case, using captive screws in cover.

3-33. Front Panel Repair

a. General. This paragraph contains the repair procedures for the front panel. Repair of the front panel

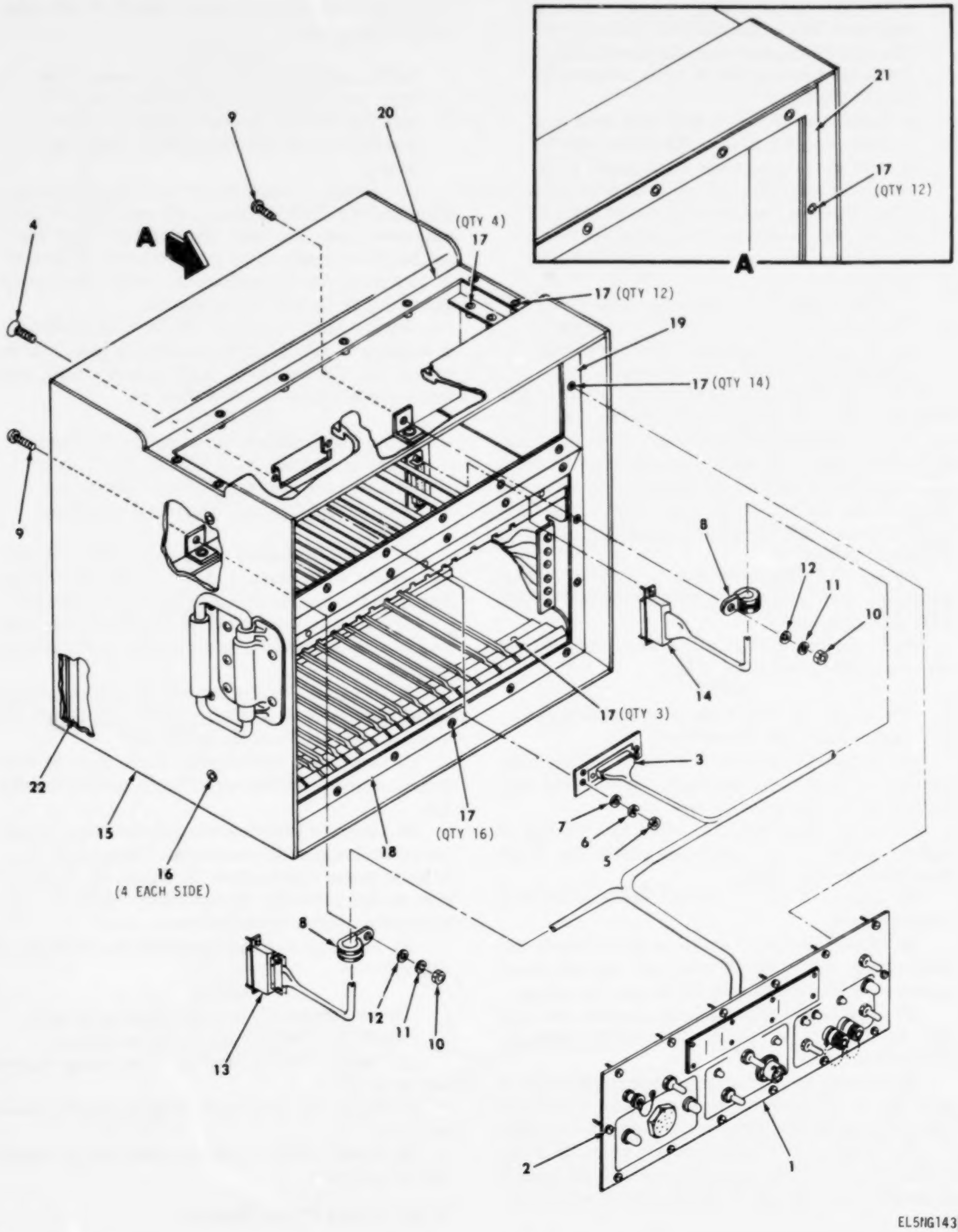

21
17
(QTY 12)
A
9
20
(QTY 4)
17
A
4
17 (QTY 12)
19
17 (QTY 14)
9
8
12
11
10
14
17 (QTY 3)
3
22
15
17
(QTY 16)
7
6
5
18
16
(4 EACH SIDE)
8
12
11
10
13
2
1
EL5NG143

Figure 3-18. Front panel 21A14, removal and installation diagram.

1 Front panel 21A14
2 Captive screw (14)
3 Connector 21A14J3
4 Screw (2)
5 Nut (2)
6 Lockwasher (2)
7 Flat washer (2)
8 Clamp (2)
9 Screw (2)
10 Nut (2)
11 Lockwasher (2)
12 Flat washer (2)
13 Connector 21A14P1
14 Connector 21A14P2
15 Case
16 Locking insert (8)
17 Locking insert (61)
18 Front cover gasket
19 Front panel gasket
20 Top cover gasket
21 Power supply gasket
22 Card file gasket

Legend for fig. 3-18:

---

consists of replacing faulty contacts in front panel connectors 21A14J3, 21A14P1, or 21A14P2, wire replacement, and replacement of faulty electrical components on the front panel. The procedures include the replacement of electrical components on printed circuit card 21A14A1, mounted on the rear of the front panel. The procedures for replacement of faulty contacts in connectors 21A14J3, 21A14P1, and 21A14P2 are in *c* and *d* below. Subparagraph *e* below contains the procedures for replacing faulty wires and electrical components on the front panel. When replacing components or wiring, use appropriate heat-shrink insulation sleeving as was installed on wiring or component being replaced.

b. Tools Required for Front Panel Repair. Connector repair tool kit 7073009C-009, electrical equipment tool kit TK-105/G, and bench top repair center PRC-150A contain the tools required for the repair procedures in *c* through *e* below. The insertion, extraction, and crimp tools used for connector repair are contained in the connector repair tool kit. Specific connector repair tools are listed as part of the repair procedures for each connector.

c. Connector 21A14P2 and 21A14J3 Repair Procedures. Each connector contains 17 nonrepairable contacts and 7 replaceable contacts. The tool listed below is required to extract the faulty replaceable contacts. No special tools are required to install the replacement contacts in the connector.

Tool	*Part No.*
Extraction tool	ITT Cannon CET-C6B

(1) If contacts being replaced are in connector 21A14P2, it is necessary to remove the connector cover. Remove 21A14P2 connector cover as shown in figure 3-19. Back captive screws into clips so that slips can be removed.

(2) Unsolder and remove wire from faulty contact(s).

(3) On face of connector, insert tip of extraction tool in cavity of contact to be removed. Insert tip of tool until it bottoms and closes around retaining ring on contact.

(4) Hold tool in position to keep retaining ring closed and then push plunger on tool to push contact out of connector.

NOTE

Replacement contacts A1 and A2 are part number SM-B-942074-2 and contacts A3 through A7 are part number SM-B-942074-1.

(5) On rear (wire side) of connector, insert proper contact in cavity. Push contact into connector until retaining ring opens and holds contact securely in place.

(6) Clean stripped end of wire or restrip wire by removing between $\frac{1}{8}$ and $\frac{5}{32}$ inch of insulation from wire. Inspect stripped wire for broken or frayed ends that could prevent a good solder connection.

(7) Solder wire end in solder cup on end of replacement contact.

(8) Check wire for proper solder joint. Inspect contacts in connector to ensure that solder spills have not formed undesirable solder bridges.

(9) If applicable, install connector cover.

d. Connector 21A14P1 Repair Procedures. The contacts in connector 21A14P1 are replaceable. The repair procedures require the tools listed below to extract and insert a contact.

Tool	*Part No.*
Crimp tool	M22520/2-01
Crimp turret (used with crimp tool)	M22520/2-08
Removal tool	ATC 2076

(1) Remove connector cover as shown in figure 3-19. Back captive screws into clips so that clips can be removed.

(2) Remove alignment pin from removal tool by slightly spreading tool. Then position end of tool over wire of contact to be removed.

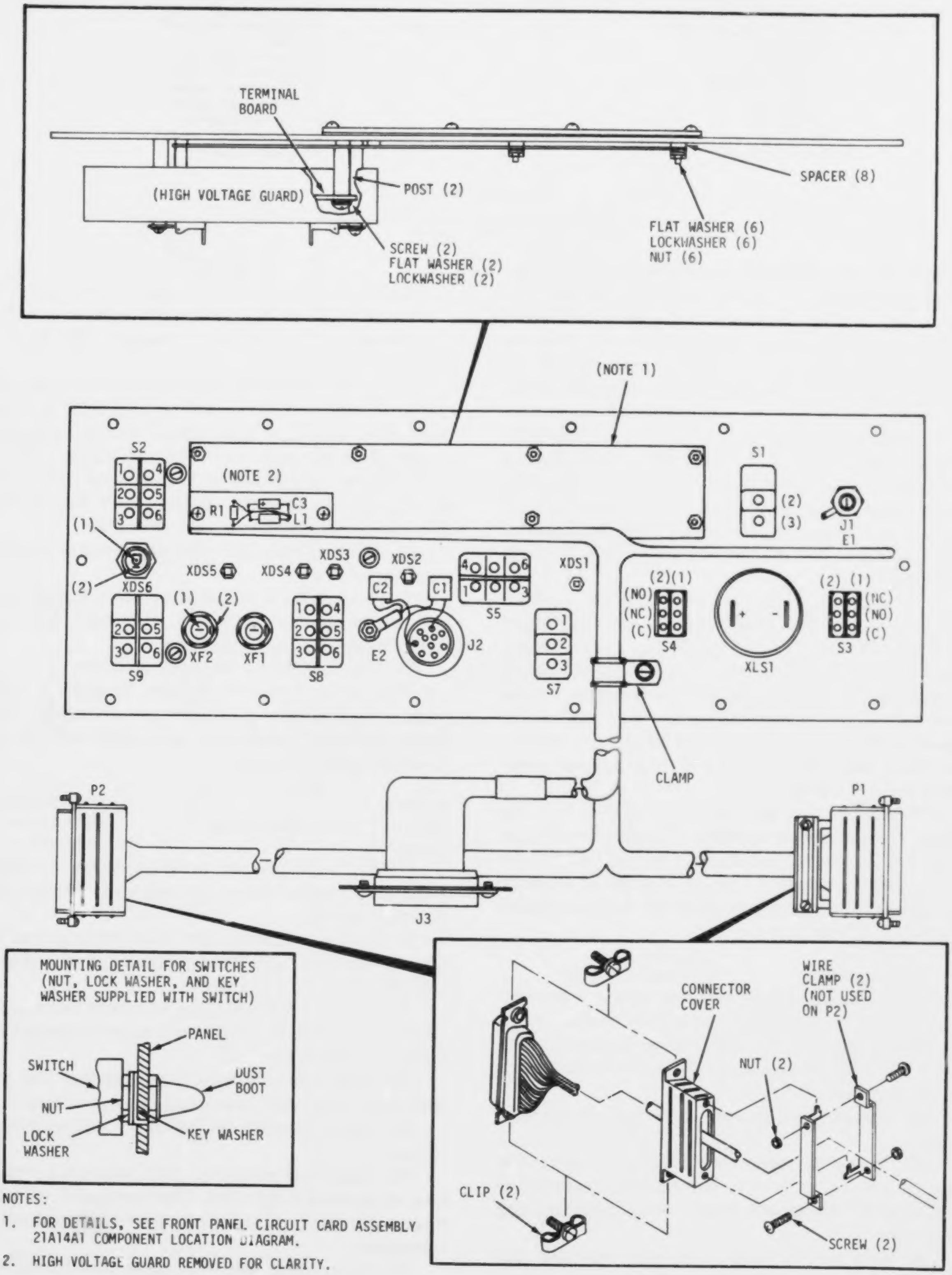
(3) Slide tool forward along wire until tool touches contact. Push firmly on tool until tines on contact are released in connector.

(4) Press and hold wire firmly against tool and then remove tool, wire, and contact from connector.

(5) Using diagonal cutting pliers, cut wire from contact.

(6) Using wire strippers, strip between $\frac{1}{8}$ and $\frac{5}{32}$ inch of insulation for wire. Check stripped wire for broken or frayed ends that may prevent a good crimp connection.

(7) Using crimp tool with crimp turret installed, crimp replacement contact M24308/10-1 to stripped


TERMINAL BOARD
(HIGH VOLTAGE GUARD)
POST (2)
SPACER (8)
SCREW (2)
FLAT WASHER (2)
LOCKWASHER (2)
FLAT WASHER (6)
LOCKWASHER (6)
NUT (6)
(NOTE 1)
(NOTE 2)
S2
R1
C3
L1
S1
(2)
(3)
J1
E1
(1)
(2)
XDS6
XDS5
XDS4
XDS3
XDS2
XDS1
C2
C1
S5
(2)(1)
(NO)
(NC)
(C)
S4
XLS1
(2) (1)
(NC)
(NO)
(C)
S3
S9
XF2
XF1
S8
E2
J2
S7
CLAMP
P2
P1
J3
MOUNTING DETAIL FOR SWITCHES (NUT, LOCK WASHER, AND KEY WASHER SUPPLIED WITH SWITCH)
PANEL
SWITCH
DUST BOOT
NUT
LOCK WASHER
KEY WASHER
CONNECTOR COVER
WIRE CLAMP (2) (NOT USED ON P2)
NUT (2)
CLIP (2)
SCREW (2)
EL5NG114

NOTES:

1. FOR DETAILS, SEE FRONT PANEL CIRCUIT CARD ASSEMBLY 21A14A1 COMPONENT LOCATION DIAGRAM.
2. HIGH VOLTAGE GUARD REMOVED FOR CLARITY.

Figure 3-19. Front panel 21A14, component location diagram.

wire. Ensure that contact is securely and correctly crimped to wire.

(8) Insert contact into connector and press down on wire and contact until contact snaps into connector. Pull lightly on wire to ensure that contact is securely positioned in connector.

e. Front Panel Component Replacement Procedures. There are no special procedures for replacing the front panel components shown in figure 3-19. When repairing a wire or replacing one of the components listed below, perform the appropriate action listed for the item.

(1) *Ferrite bead installation at J2-A or J2-C.* When replacing a wire at either terminal, ensure that ferrite bead SM-A-942085-1 is installed on wire as close to the terminal as possible. Use heat-shrink insulation sleeving M23053/5-106-9 to hold bead in place.

(2) *S1, S2, S5, S8, or S9 replacement.* When installing a replacement switch, discard one hexagon nut supplied with item. Replace discarded nut with dust boot SM-A-942064, which contains a nut for attaching switch to panel.

(3) *S7 replacement.* When installing a replacement switch, discard one hexagon nut supplied with item. Replace discarded nut with dust boot M5423/02-01, which contains a nut for attaching switch to panel.

(4) *DS1 through DS5 wire replacement.* When replacing wires connected to indicators DS1 through DS5, apply epoxy adhesive MIL-A-46864 at intersection of replacement wires and terminal board.

(5) *LS1 replacement.* When installing a replacement horn, remove nose ring supplied with item. Apply adhesive MIL-A-46146, Type I, to mating surfaces of horn and panel. Attach horn to panel using alarm cap SM-C-941706. Discard screws supplied with horn and solder wires directly to terminals.

(6) *J1 replacement.* When installing a replacement connector, discard lockwasher supplied with item and replace it with terminal lockwasher SM-B-603975.

(7) *DS1 through DS6 replacement.* When installing one of these indicators, apply adhesive MIL-A-46146, Type I, to mating surfaces of indicator and panel.

(7.1) *P2 connector cover replacement.* When replacing cover for connector P2, remove and discard 2 wire clamps and associated hardware.

(8) *Component replacement on circuit card 21A14A1.* Remove circuit card 21A14A1 as directed in (*a*) through (*g*) below to obtain access to components. Replace component(s) as directed in printed circuit and repair procedures of section X. The locations of components on card are shown in figure 3-20. Reinstall circuit card 21A14A1 after component replacement procedures are completed.

(*a*) If installed, remove high voltage guard (fig. 3-19).

(*b*) Remove two sets of screws, lockwashers, and flat washers securing terminal board (fig. 3-19). Position terminal board off to side.

(*c*) Remove two posts (fig. 3-19).

(*d*) Remove six sets of nuts, lockwashers, and flat washers securing circuit card 21A14A1 (fig. 3-19).

(*e*) Remove hardware securing clamp (fig. 3-19).

(*f*) Lift up on wiring harness to allow for removal of circuit card 21A14A1.

(*g*) Position circuit card 21A4A1 so access can be gained to both card sides.

3-34. Case Gasket Replacement Procedures

a. General. There are five electronic shielding gaskets mounted on the case that can be replaced. The gaskets are preformed and made of silicone rubber strips embedded with braided monel wire. The replacement procedures in *b* below are applicable for replacing any one of these five gaskets. There are no special tools involved in the replacement procedures. The locations of the gaskets are shown in figure 3-18 (items 18 through 22) and the part numbers for the gaskets are listed below.

(1) Front cover electronic shielding gasket SM-B-942104 (front cover gasket) is mounted under the front cover on the case.

(2) Front panel electronic shielding gasket SM-B-942100 (front panel gasket) is mounted under the front panel on the case.

(3) Top cover electronic shielding gasket SM-B-942102 (top cover gasket) is mounted under the top cover on the case.

(4) Power supply electronic shielding gasket SM-B-942103 (power supply gasket) is mounted under the power supply on the case.

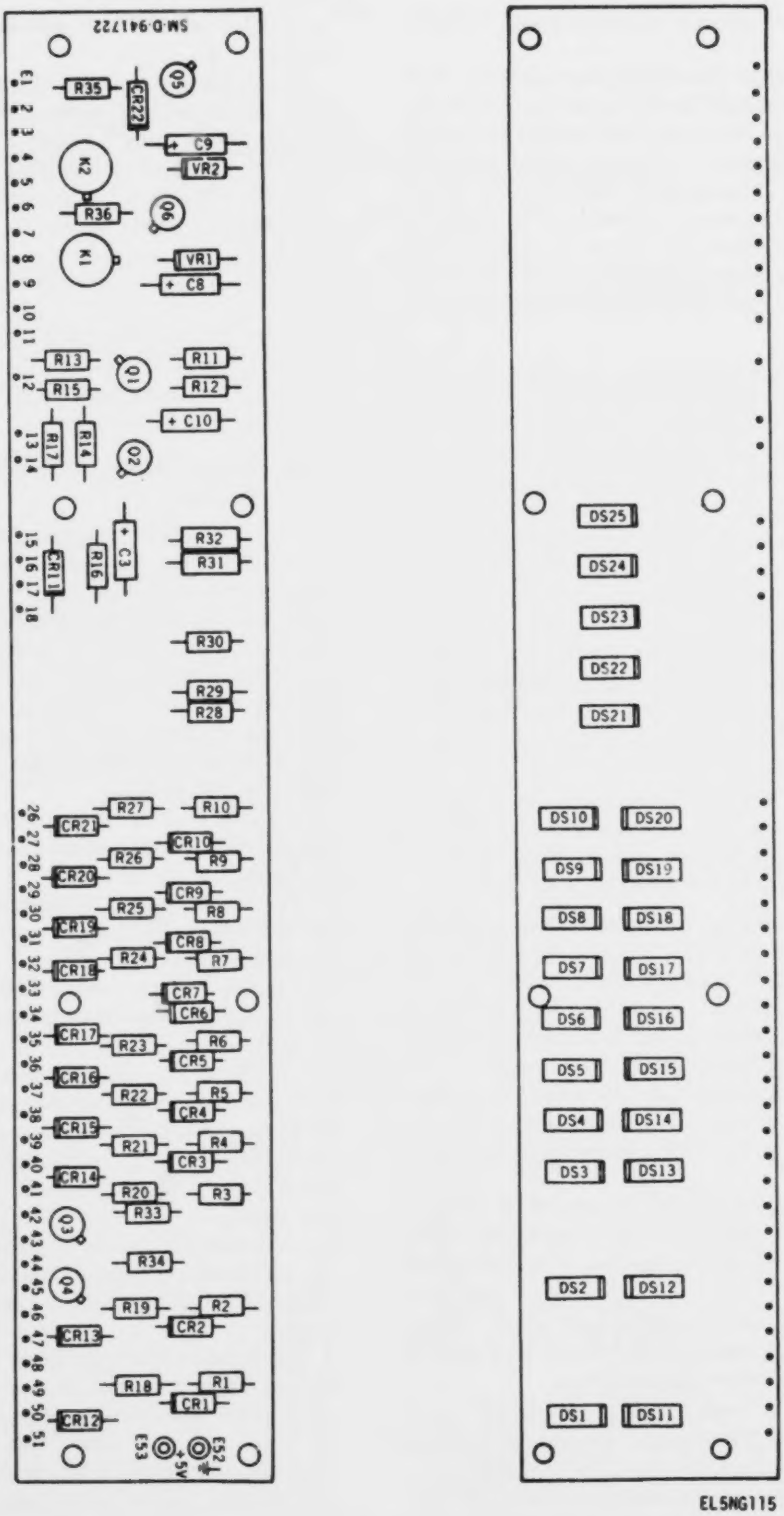
(5) Rear panel electronic shielding gasket SM-B-942101 (card file gasket) is mounted on the rear interior of the case. The connector panel on the rear of the card file faces the gasket.

b. Gasket Replacement Procedures. Perform the following procedures to replace the five gaskets listed in *a* above.

(1) Remove faulty gasket from case. Clean bonding and conductive surface area on case. Refer to figure 3-21 for identification of surface areas.

CAUTION

> When preparing and applying primer and adhesive, follow manufacturer's instructions to ensure proper bonding of gasket material to case.
>
> Do not coat conductive surfaces of gasket or case with primer or adhesive that could


SM-D-941722
E1
2
3
4
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17
18
26
27
28
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42
43
44
45
46
47
48
49
50
51
R35
CR22
Q5
C9
VR2
K2
R36
Q6
K1
VR1
C8
R13
Q1
R11
R15
R12
C10
R17
R14
Q2
R32
R31
CR11
R16
C3
R30
R29
R28
R27
R10
CR21
CR10
R26
R9
CR20
CR9
R25
R8
CR19
CR8
R24
R7
CR18
CR7
CR6
CR17
R23
R6
CR5
CR16
R22
R5
CR4
CR15
R21
R4
CR3
CR14
R20
R3
R33
Q3
R34
Q4
R19
R2
CR2
CR13
R18
R1
CR1
CR12
E53
+5V
E52
DS25
DS24
DS23
DS22
DS21
DS10
DS20
DS9
DS19
DS8
DS18
DS7
DS17
DS6
DS16
DS5
DS15
DS4
DS14
DS3
DS13
DS2
DS12
DS1
DS11
EL5NG115

Figure 3-20. Front panel circuit card 21A14A1, component location diagram.

eliminate or restrict EMI filtering capability.

(2) Apply MIL-A-46146, Type II, primer to bonding surface area on case. Wipe off any primer spills on conductive surface area.

(3) Inspect and ensure that conductive surfaces on gasket and on case are clean and will mate properly when gasket is bonded to case.

(4) After primer is dry, apply coat of MIL-A-46146, Type II, adhesive to bonding area on gasket.

(5) Carefully install gasket on case and remove any excess adhesive from gasket or case immediately.

3-35. Case Locking Insert Replacement Procedures

a. General. There are 8 MS21209F4-15 and 61 MS21209C0815 replaceable locking inserts mounted in the case. The locking inserts are shown as items 16 and 17, respectively, in figure 3-18. The tools required to replace the locking inserts are given in *b* below. The procedures for replacing either type of locking insert are listed in *c* below.

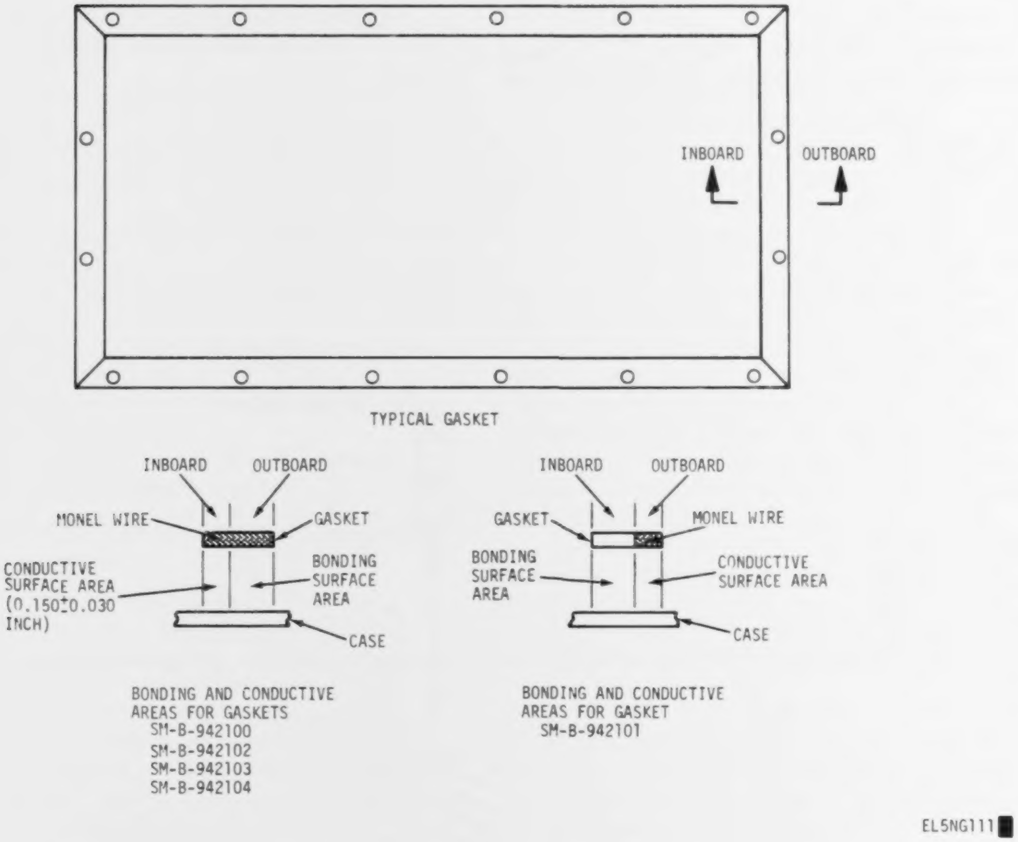

INBOARD
OUTBOARD
TYPICAL GASKET
INBOARD
OUTBOARD
MONEL WIRE
GASKET
CONDUCTIVE SURFACE AREA (0.150±0.030 INCH)
BONDING SURFACE AREA
CASE
BONDING AND CONDUCTIVE AREAS FOR GASKETS SM-B-942100 SM-B-942102 SM-B-942103 SM-B-942104
INBOARD
OUTBOARD
GASKET
MONEL WIRE
BONDING SURFACE AREA
CONDUCTIVE SURFACE AREA
CASE
BONDING AND CONDUCTIVE AREAS FOR GASKET SM-B-942101
EL5NG111

Figure 3-21. Typical shielding gasket installation diagram.

b. Tools Required. The tools required to remove and install the locking inserts in the case are listed below:

(1) Locking insert MS21209C0815 (insert is 0.246 inch long with 0.164-32 UNC internal thread size; 8-32).

Tool	*Part No.*
Extraction tool	Heli-Coil 1227-06
Insertion tool	Heli-Coil 7551-2
Tang breakoff tool	Heli-Coil 3695-2

(2) Locking insert MS21209F4-15 (insert is 0.375 inch long with 0.25-28 UNF internal thread size; 1/4-28).

Tool	*Part No.*
Extraction tool	Heli-Coil 1227-6
Insertion tool	Heli-Coil 7552-4
Tang breakoff tool	Heli-Coil 3695-4

c. Replacement Procedures. Perform the following procedures to remove and install a locking insert in the case. A typical locking insert and the tools used in the following procedures are shown in figure 3-22.

(1) Place blade of extraction tool in locking insert so that one side of blade is approximately one quarter turn from end of insert. Strike head of tool with hammer so that blade digs into top coil of insert. Bear down on tool and maintain downward pressure while rotating tool counterclockwise until insert is removed.

(2) Place end of insertion tool on tang of replacement locking insert and rotate handle of tool clockwise until insert is positioned to desired depth. Remove insertion tool.

(3) Position tang breakoff tool tip on tang of locking insert. Apply pressure on tool until tang snaps off. Remove tang from insert.

(4) Inspect locking insert for damage that would cause binding or inhibit screw from being installed in insert.

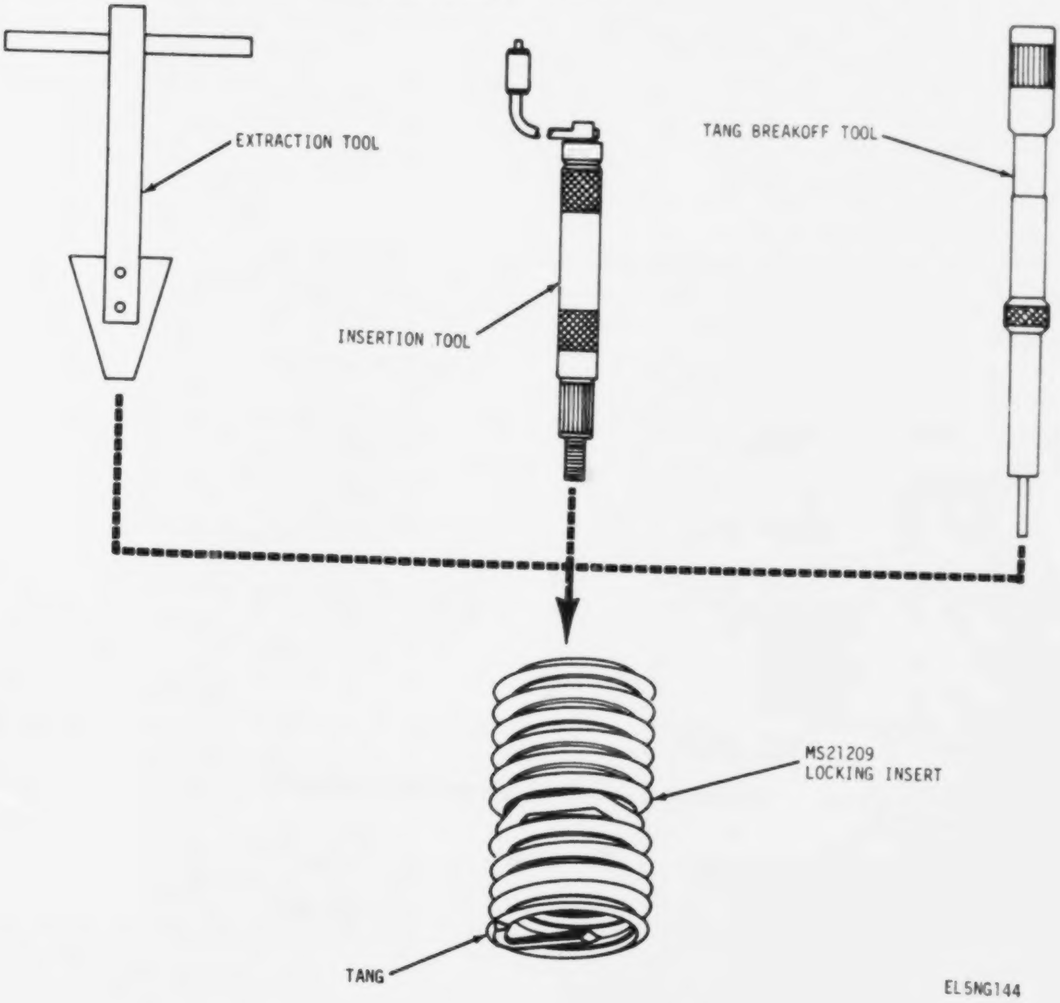


Figure 3-22. Typical locking insert and extraction/insertion tool.

Section IX. MAINTENANCE OF CARD FILE 21A13

3-36. Introduction

a. General. This section contains the procedures for repairing the card file. The plug-in circuit cards are not part of the card file. When the card file is removed from the case and all the plug-in circuit cards are removed from the card file, all the repairable items are accessible.

b. Card File Removal Instructions. The card guides can be replaced without removing the card file from the case. The replacement or repair of other components on the card file require that the card file be removed from the case as directed in paragraph 3-37. Paragraph 3-37 contains the procedures for removing and installing the card file in a case.

c. Maintenance Procedures. The items that can be repaired or replaced on the card file are listed in (1) through (7) below.

(1) Card guide replacement procedures are in paragraph 3-38.

(2) Replacement procedures for the discrete components mounted on the card file frame are in paragraph 3-39.

(3) Connector J30 repair procedures are in paragraph 3-40.

(4) Backplane wire replacement procedures are in paragraph 3-41.

(5) Backplane connector pin replacement procedures are in paragraph 3-42.

(6) Backplane interface connector repair procedures are in paragraph 3-43.

(7) Repair or replacement of components on the connector panel are in paragraph 3-44.

3-37. Card File Removal and Installation Procedures

WARNINGS

- High voltage that can cause death or serious injury is present in the TD-976/G.
- The 115-volt ac primary power is always applied to TB1 in the card file and to switch S9 on the front panel when the power cable is connected between the ac power source and the TD-976/G. Always disconnect the power cable when working in the TD-976/G.
- Cable drive power of 400 volts dc with a constant current of 45 milliamperes may be present in the equipment when the POWER IN and/or POWER OUT indicator is lit. The high voltage can be generated within the unit or the cable power may be applied from another TD-976/G that is connected to the unit being serviced.
- Wait at least 10 seconds after cable power is removed from the TD-976/G before working on equipment to ensure that high-voltage capacitors in the unit are discharged.

a. Removal Procedures. Perform the following procedures to remove the card file from the case. No special tools are required in the removal and installation procedures. Electrical equipment tool kit TK-105/G contains the common tools required in the procedures.

(1) Set POWER SUPPLY and POWER CABLE switches to OFF. Ensure that POWER IN and POWER OUT indicators are out.

(2) Disconnect any cables attached to TD-976/G.

(3) Remove front cover, if installed, by loosening 16 captive screws.

(4) Remove top cover, if installed, by loosening 12 captive screws.

(5) Remove RAU, if installed, by loosening four captive screws.

(6) Loosen 12 captive screws on power supply and then remove power supply from case.

(7) Remove two sets of screws, washers, and nuts securing two clamps to brackets and case (fig. 3-23). Leave clamps around wiring harness.

(8) Remove plug-in cards from card file.

(9) Loosen captive screws on front panel connectors 21A14P1 and 21A14P2 (fig. 3-18, items 13 and 14) and then disconnect 21A14P1 and 21A14P2 from card file connectors. Position front panel wiring harness and connectors up and out of card file area. Clamps are still around wiring harness.

(10) In front of card file, remove seven sets of screws and washers securing card file to case (fig. 3-23). Four sets are in top of card file and three sets are in bottom of card file.

(11) Remove two sets of screws and washers securing two brackets to card file (fig. 3-23). Remove two brackets and set aside.

(12) On rear of case, remove 14 sets of screws and washers securing card file to case (fig. 3-23).

CAUTION

When performing (13) below, insure that front panel connectors 21A14P1 and 21A14P2 are clear of card file to prevent possible damage to connectors and wiring.

(13) Carefully slide card file out of front of case.

(14) Inspect card file gasket (fig. 3-18, item 22) on case for damage. If necessary, replace card file gasket (para 3-34).

b. Installation Procedures. Perform the following procedures to install a card file in the case. It is assumed that the front cover, top cover, power supply, and RAU are not installed on or in the case at this time. It is also assumed that the plug-in cards are not installed in the card file.

CAUTION

When performing (1) below, ensure that front panel connectors 21A14P1 and 21A14P2 are clear of the card file to prevent possible damage to connectors and wiring.

(1) Carefully slide card file in case until rear of card file mates with rear of case.

(2) Attach rear of card file to case, using 14 sets of screws and washers removed in *a*(12) above (fig. 3-23).

(3) Attach two brackets to card file, using screws and washers removed in *a*(11) above (fig. 3-23).

(4) Attach front of card file to case, using seven sets of screws and washers removed in *a*(10) above (fig. 3-23).

(5) Using two captive screws on each connector, secure connectors 21A14P1 (left) and 21A14P2 (right) to card file connectors.

(6) Attach two clamps to brackets and case, using screws, washers, and nuts removed in *a*(7) above (fig. 3-23). Clamps are still around wiring harness.

(7) Install plug-in cards removed in *a*(8) above into card file.

(8) Carefully slide power supply into case, engaging guide pins in mating connector. Using hands, firmly press power supply so as to engage its connector with mating connector. Secure power supply to case, using power supply captive screws.

NOTE

Do not perform (9) through (11) below if additional TD-976/G testing is to be performed.

(9) Install RAU in top of case, using captive screws on RAU.

(10) Install top cover on case, using captive screws in cover.

(11) Install front cover on case, using captive screws in cover.

c. Connector Panel Removal and Installation. The connector panel may be removed to the extent allowed by service loop in wiring. This allows access to rear of connector panel, rear of backplane, and other discrete components.

(1) Remove 12 screws (fig. 3-25, sheet 1) securing connector panel to card file frame.

(2) Carefully remove and lay connector panel down. Avoid placing stress on wiring harnesses.

(3) After repairs have been completed, reinstall connector panel, using 12 screws removed in (1) above.

3-38. Card Guide Replacement Procedures

The card guides in the card file are snap-in items. Tools are not required to replace a damaged card guide. Perform the following procedures to replace a damaged upper or lower card guide. The card file does not have to be removed from the case to perform the following procedures. However, the front cover must be removed.

a. Set POWER SUPPLY and POWER CABLE switches to OFF. Ensure that POWER IN and POWER OUT indicators are out.

b. If installed, remove plug-in card from card guide to be replaced. Except for end card guides, remove at least two plug-in cards on each side of the card guide to be replaced to provide adequate working space.

c. Apply pressure under front part of card guide (fig. 3-24) until end of card guide snaps out of front slot in card file. Lift card guide upward and remove rear of card guide from rear slot in card file.

d. Install rear end of replacement card guide in rear slot in card file.

e. Carefully bend front end of card guide downward and insert front end of card guide in front slot in card file. Press down on card guide until it snaps into place in card file.

f. Install plug-in card in card guide. Check that plug-in card does not bind when it is pressed into card file connector.

g. Replace other plug-in cards removed in *b* above.

3-39. Discrete Component Replacement Procedures

a. General. The discrete components are identified as transformers T1 and T2 on the backplane, capacitors C1, C2, and C3, resistors R1 and R2 on the card file frame, and six power test points on front of card file. The location of these components is shown in figure 3-25.

b. Tools Required. Electrical equipment tool kit TK-105/G and bench top repair center PRC-150A contain the tools required for the repair procedures in *c* below.

c. Procedures. Perform the following procedures to replace one or more of the discrete components in the card file. The card file does not have to be removed to replace a power test point.

(1) Remove card file from case (para 3-37*a*).

(2) Remove connector panel (para 3-37*c*).

(3) There are no special or unique procedures required in the replacement of the discrete components. When replacing capacitor C1, ensure that lead common to capacitor case is connected to terminal to which R2 is connected. Use standard procedures when unsoldering and soldering wires or components. Tag unsoldered wires to ensure that proper connections are made to replacement items.

(4) Install connector panel (para 3-37*c*).

(5) Install card file in case (para 3-37*b*).

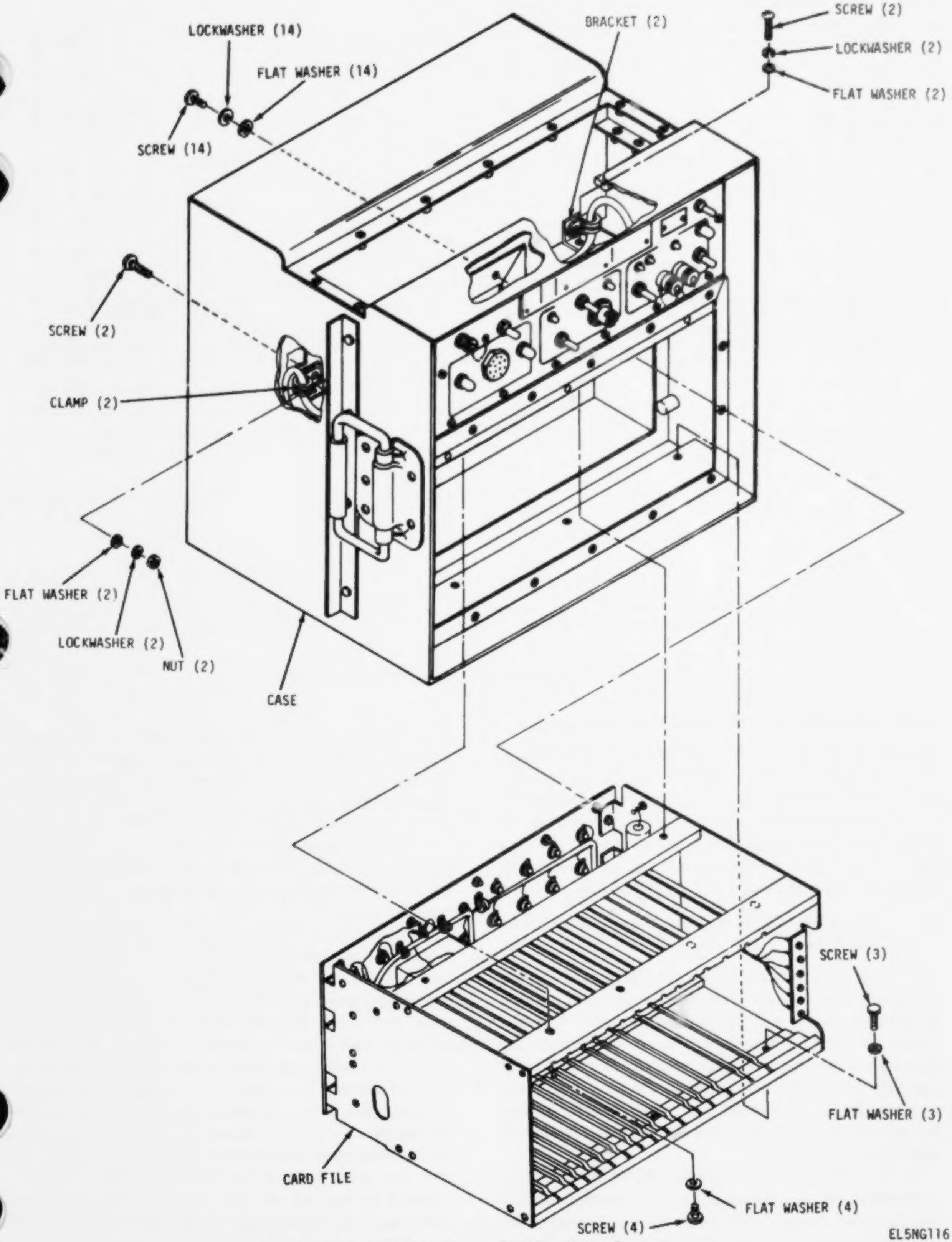

SCREW (2)
LOCKWASHER (2)
FLAT WASHER (2)
BRACKET (2)
LOCKWASHER (14)
FLAT WASHER (14)
SCREW (14)
SCREW (2)
CLAMP (2)
FLAT WASHER (2)
LOCKWASHER (2)
NUT (2)
CASE
SCREW (3)
FLAT WASHER (3)
CARD FILE
FLAT WASHER (4)
SCREW (4)
EL5NG116

Figure 3-23. Card file 21A13, removal and installation diagram.

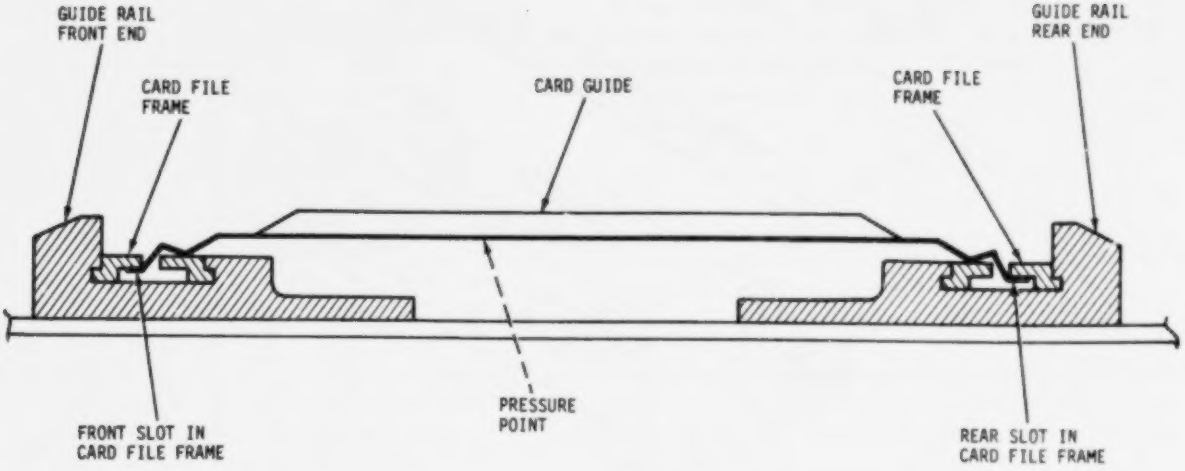


Figure 3-24. Card guide, removal and installation diagram.

3-40. Connector J30 Repair Procedures

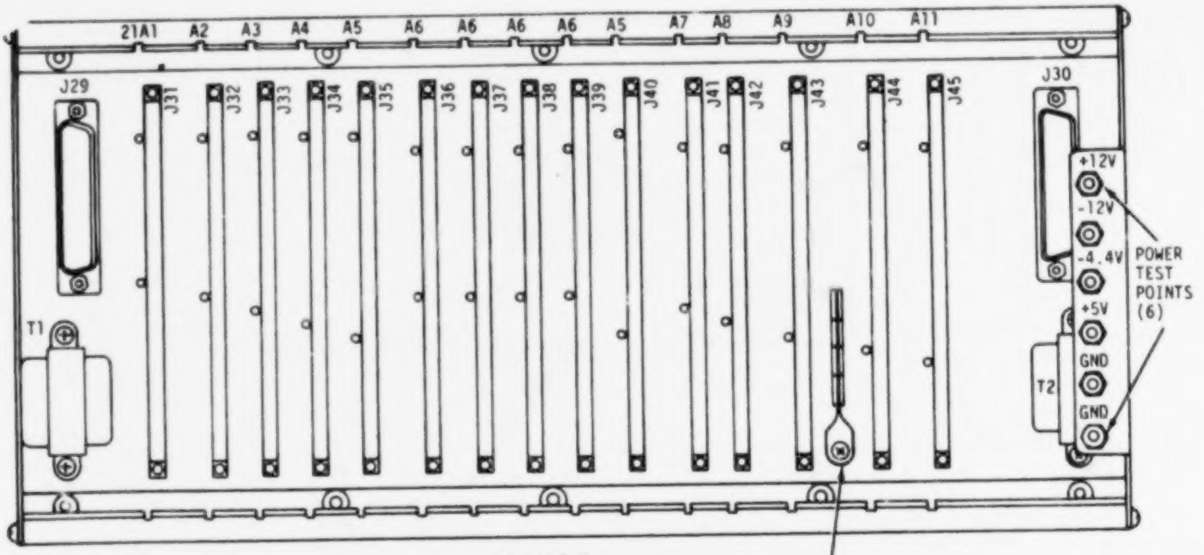
Connector J30 contains 17 nonrepairable contacts and 7 replaceable contacts. The seven replaceable contacts in connector J30 are identical to the replaceable contacts in connectors P2 and J3 on the front panel. To replace one of the contacts in connector J30, perform the contact replacement procedures as directed in paragraph 3-33c for 21A14P2 and 21A14J3.

3-41. Backplane Wire Replacement Procedures

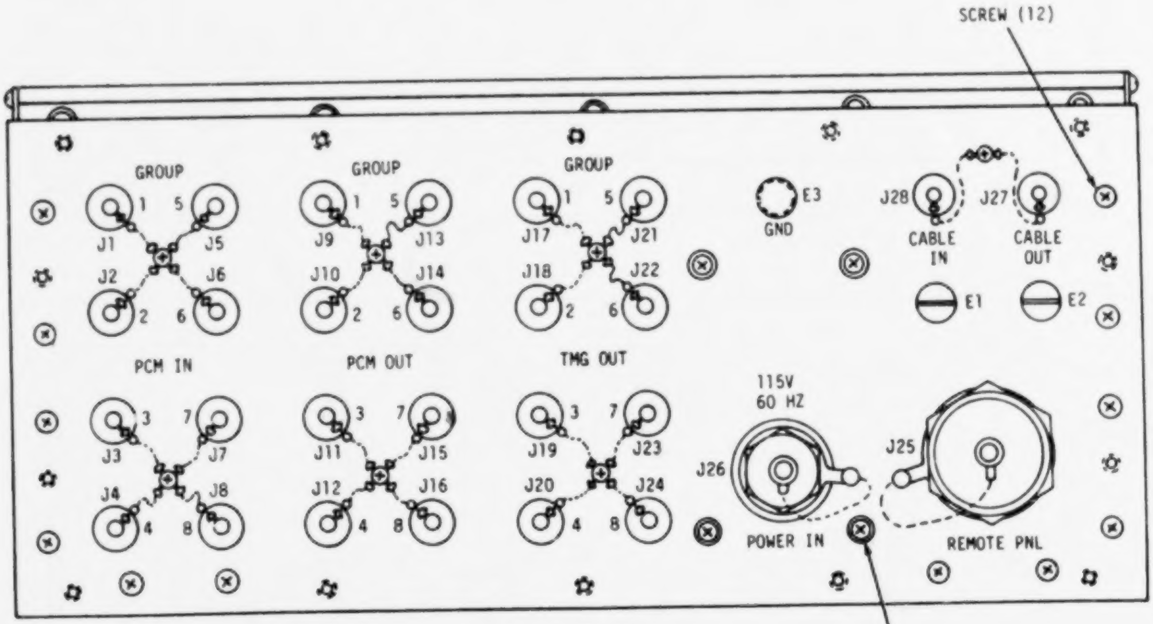
a. General. The wires attached to connector J30 are soldered to the contacts. There are no special requirements to unsolder and solder a replacement wire to a contact in J30. The wire terminations for the interconnecting wires between connectors J29 and J31 through J45 are wire-wrapped to the pins in the connectors. The requirements and procedures for replacing one or more of these wires are described in the following subparagraphs.

b. Wire-Wrap Requirements. When a wire-wrap connection on a connector pin is loosened or unwrapped for maintenance purposes, a new wire-wrap connection must be made. The portion of the wire that was wrapped around the connector pin must be cut off and the end of the remaining wire restripped before the wire is wrapped around the connector pin. When the remaining piece of wire is not long enough to make a wire-wrap on the appropriate connector pin, then the wire must be completely removed and a new wire installed as instructed in *e* below. The tools required for removing and installing a wire-wrap connection are listed in *d* below.

c. Use of level 3 Wire-Wraps. Connector pins have either one or two levels of wire-wraps. As shown in figure 3-26, the connections or a connector pin are designated as level 1 and level 2 wire-wraps. A level 1 wire-wrap is not disturbed when a level 2 wire-wrap is replaced. But a level 1 wire-wrap cannot be replaced unless the level 2 wire-wrap is removed. To prevent rework of a level 2 wire-wrap when a level 1 wire-wrap is replaced, the level 1 wire-wrap may be cut off and reconnected as a level 3 wire-wrap when practical.The level 3 wire-wrap is permitted when the connector pin does not mate with an interface connector. It is permissible for one end of a wire to be a level 1, level 2, or level 3 and the opposite end of the wire to be connected as a different level. When a level 1 wire is too short to


21A1
A2
A3
A4
A5
A6
A6
A6
A6
A5
A7
A8
A9
A10
A11
J29
J31
J32
J33
J34
J35
J36
J37
J38
J39
J40
J41
J42
J43
J44
J45
J30
T1
T2
+12V
-12V
-4.4V
+5V
GND
GND
POWER
TEST
POINTS
(6)
E9

BACKPLANE
(FRONT VIEW)


SCREW (12)
GROUP
1
5
J1
J5
J2
J6
2
6
PCM IN
3
7
J3
J7
J4
J8
4
8
GROUP
1
5
J9
J13
J10
J14
2
6
PCM OUT
3
7
J11
J15
J12
J16
4
8
GROUP
1
5
J17
J21
J18
J22
2
6
TMG OUT
3
7
J19
J23
J20
J24
4
8
E3
GND
J28
J27
CABLE
IN
CABLE
OUT
E1
E2
115V
60 HZ
J26
J25
POWER IN
REMOTE PNL
SCREW (4)
LOCKWASHER (4)
FLAT WASHER (4)

CONNECTOR PANEL
(FRONT VIEW)

EL5NG118

Figure 3-25. Card file 21A13, component location diagram (sheet 1 of 3).

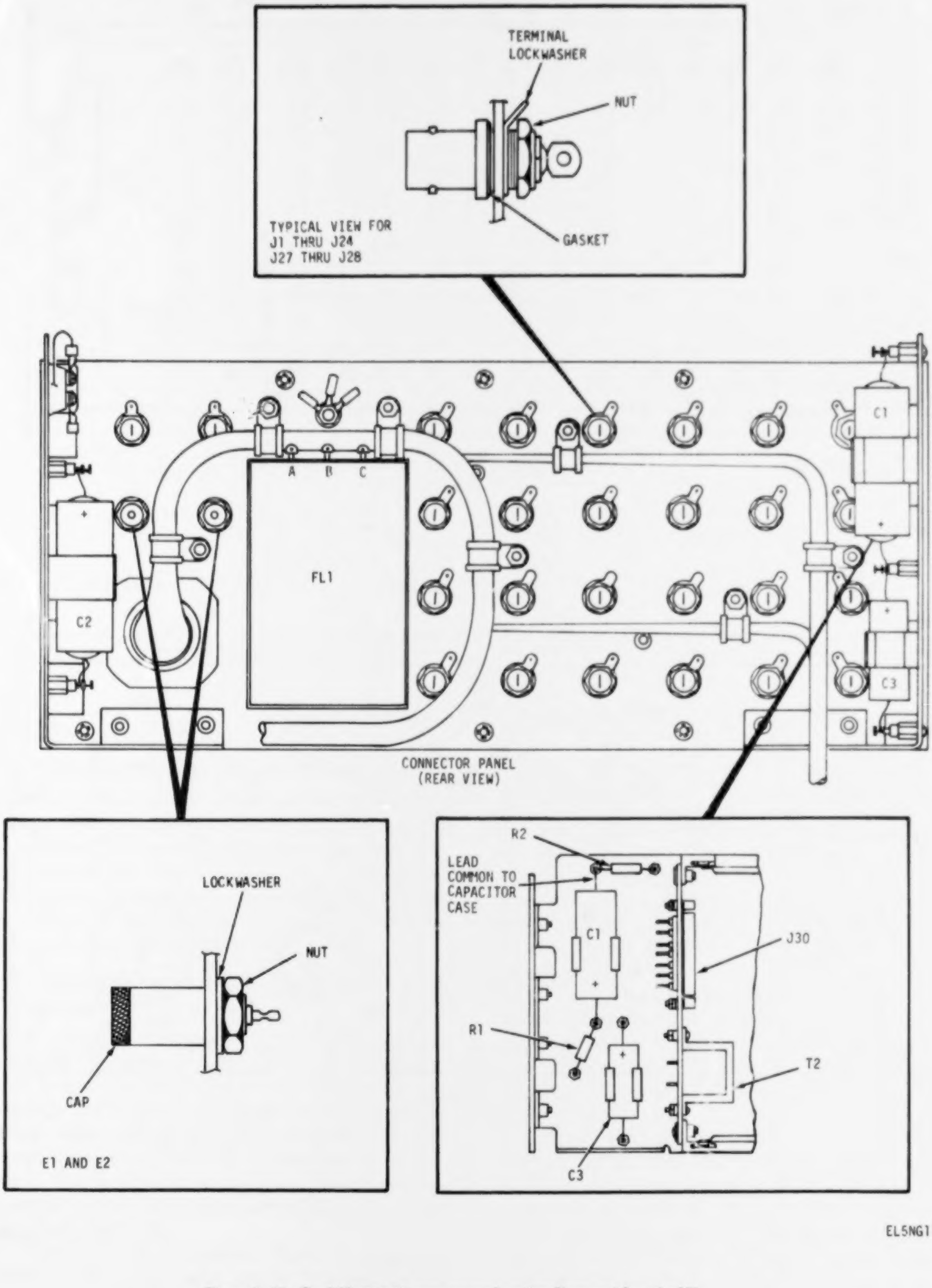

TERMINAL
LOCKWASHER
NUT
GASKET
TYPICAL VIEW FOR
J1 THRU J24
J27 THRU J28
A
B
C
FL1
C1
C2
C3
CONNECTOR PANEL
(REAR VIEW)
LOCKWASHER
NUT
CAP
E1 AND E2
R2
LEAD
COMMON TO
CAPACITOR
CASE
C1
J30
R1
T2
C3
EL5NG119

Figure 3-25. Card file 21A13, component location diagram (sheet 2 of 3).

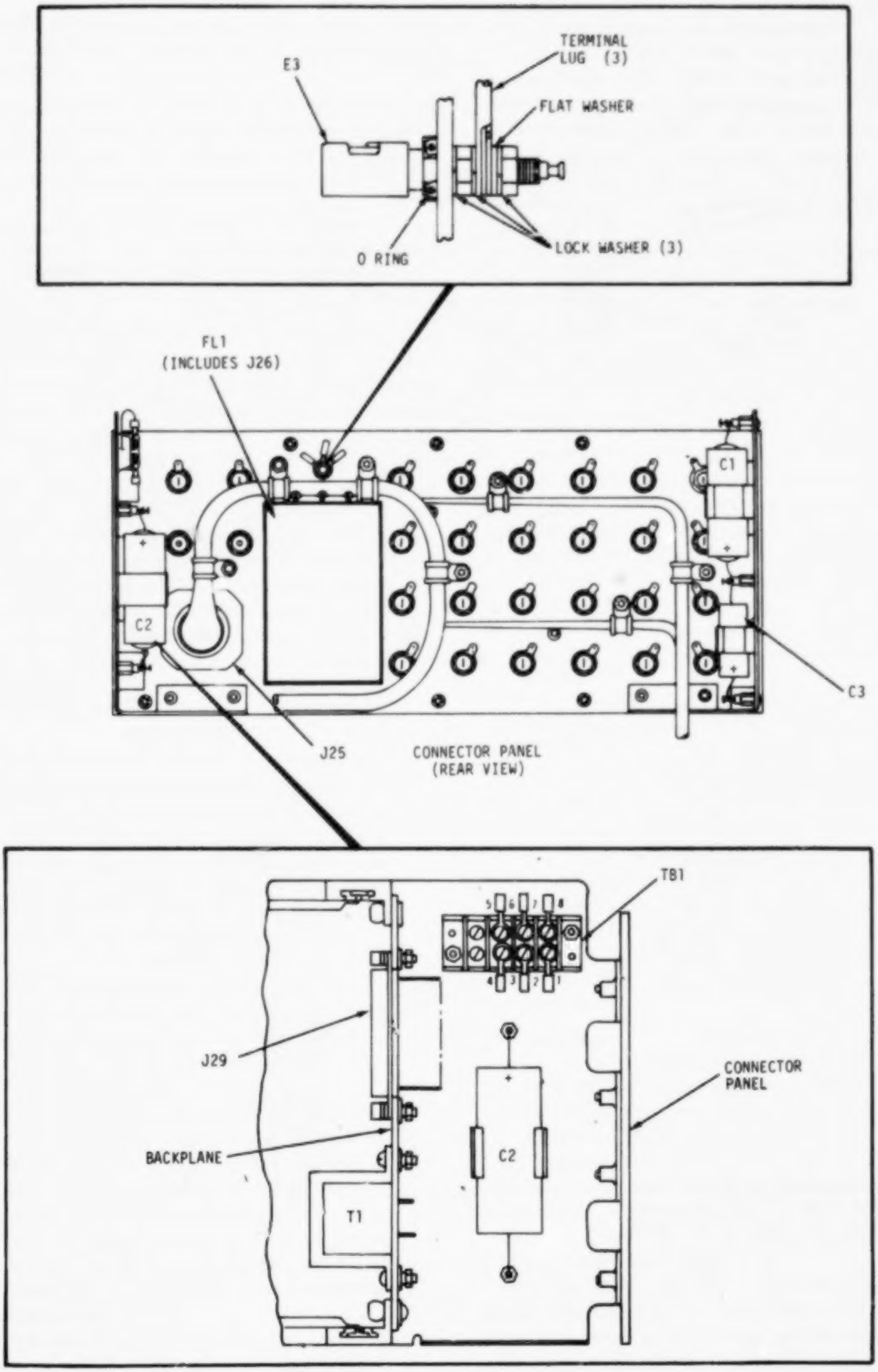
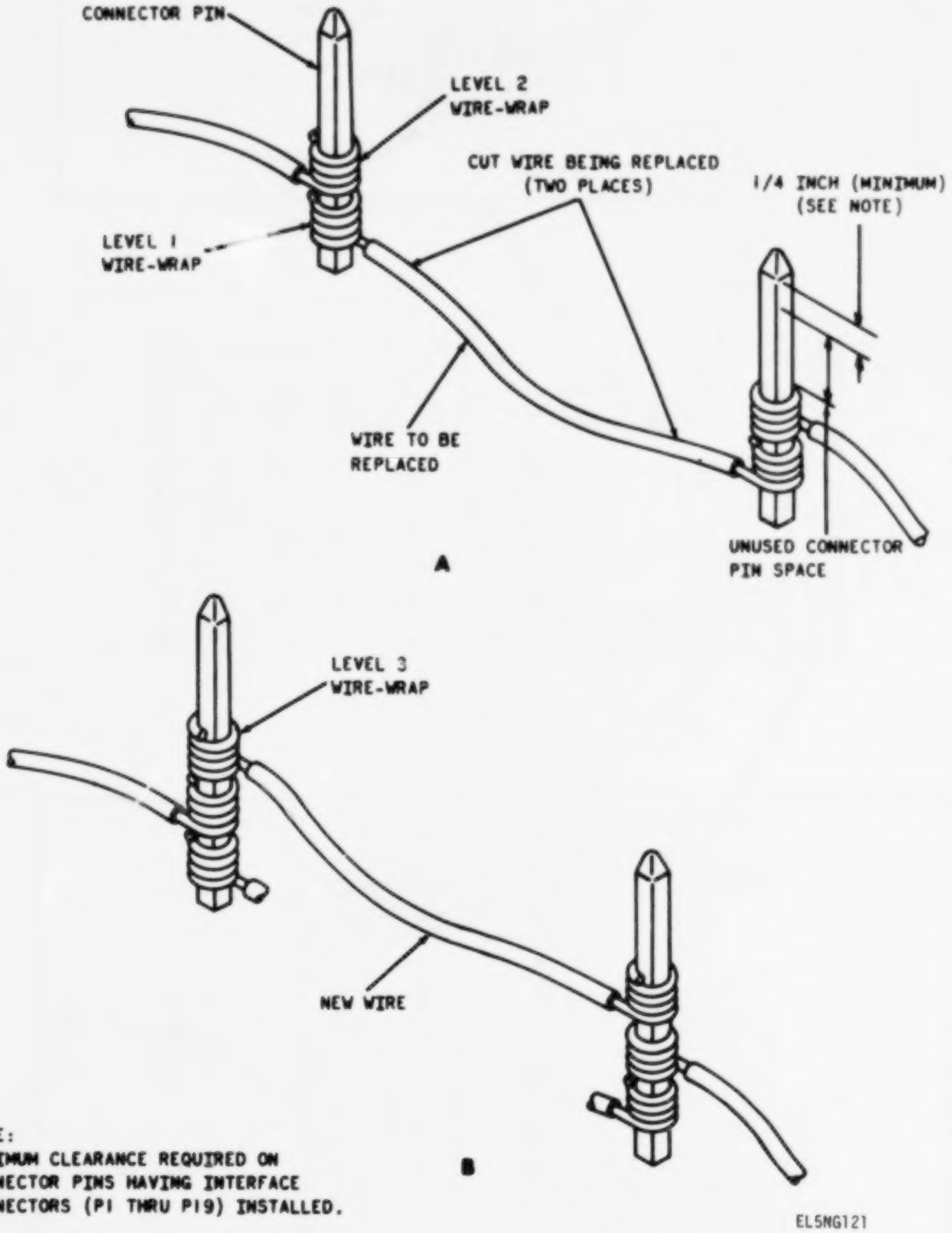

TERMINAL LUG (3)
E3
FLAT WASHER
O RING
LOCK WASHER (3)
FL1 (INCLUDES J26)
C1
C2
C3
J25
CONNECTOR PANEL (REAR VIEW)
TB1
5
6
7
8
4
3
2
1
J29
CONNECTOR PANEL
BACKPLANE
C2
T1
EL5NG120

Figure 3-25. Card file 21A13, component location diagram (sheet 3 of 3).


CONNECTOR PIN
LEVEL 2 WIRE-WRAP
CUT WIRE BEING REPLACED (TWO PLACES)
1/4 INCH (MINIMUM) (SEE NOTE)
LEVEL 1 WIRE-WRAP
WIRE TO BE REPLACED
UNUSED CONNECTOR PIN SPACE
A
LEVEL 3 WIRE-WRAP
NEW WIRE
B
EL5NG121

NOTE:
MINIMUM CLEARANCE REQUIRED ON CONNECTOR PINS HAVING INTERFACE CONNECTORS (P1 THRU P19) INSTALLED.

Figure 3-26. Backplane, wire replacement diagram.

be properly reconnected, the entire wire may be cut off and reconnected at a higher level as shown in B of figure 3-26.

d. Tools Required for Wire-Wrap Repair. The tools required to perform wire-wrap repairs are contained in connector repair tool kit 70730090-009. The specific tools are listed below and shown in figure 3-27.

Tool	*Part No.*
Cut/strip accessory	Gardner-Denver 515654
Unwrapping tool	Gardner-Denver 511203
Wire-wrapping tool	Gardner-Denver 27368AA8
Wrapping bit	Gardner-Denver 508748
Wrapping sleeve	Gardner-Denver 507100

e. Wire-Wrap Repair. Perform the following procedures to replace one or more wires on the backplane. If a connector pin becomes damaged during the unwrapping or wire-wrap procedures, replace the faulty connector pin (para 3-42). Table 3-32 lists the point-to-point wire runs on the backplane. Fiqure 3-28 shows the physical location of the connector pins on the backplane. As shown in figure 3-28, interface connectors P1 through P4 and P6 through P19 are installed on the connector pins in the backplane. To remove an interface connector, hold the housing and pull the connector from the pins. When pulling the connector, do not twist or apply pressure to the connector; twisting the connector could bend the connector pins in the backplane.

(1) Remove card file from case (para 3-37*a*).

CAUTIONS

Backplane wires are solid. To avoid breakage, do not bend or flex wires excessively.

When unwrapping a wire from a connector pin, ensure that broken wire ends or other foreign metal pieces do not drop into connector pins or backplane. Failure to remove all loose conductive materials from backplane can result in serious equipment damage.

NOTES

When more than one wire is attached to a connector pin, it may be necessary to unwrap one or more wires before reaching the wire to be replaced. Tag or otherwise identify these wires to facilitate their replacement.

Rewraping of the stripped portion of a previously unwrapped wire should not be attempted. Always cut off the used portion of the wire end and then restrip wire end as instructed in the appropriate step below.

When reconnecting only one end of one or more existing wires, perform (2) below and then proceed to (6) below for each wire end to be reconnected.

When one or more complete wires are to be replaced, perform (2) below at both ends of wire(s) to be removed. Then proceed to (3) below and repeat procedures for each complete wire to be installed in backplane.

(2) When a level 1 wire-wrap is to be removed but a level 2 wire-wrap above it is not removed, cut level 1 wire from connector pin as shown in figure 3-36. When there is no wire-wrap above the wire-wrap being unwrapped, remove wire from connector pin by placing tip or unwrapping tool (A, fiq. 3-27) under end of wire-wrap and turning tool to pry wire from connector pin.

(3) After both ends of wire are removed from connector pins, note physical routing of wire between pins. Remove wire and cut a replacement wire 4 inches longer than the removed wire.

(4) Using cut/strip accessory (A, fig 3-27, strip 1 inch of insulation from each end of wire.

CAUTION

Ensure that there is slack in each wire being connected on backplane to decrease the probability of equipment failure. If a wire is strung tightly between two pins, it is probable that the wire might be pulled taut against the edge of a third connector pin. Pressure of a taut wire against the edge of a third connector pin, plus vibration, may cause the third connector pin to cut into the wire insulation and cause a short circuit condition.

(5) Perform (7) through (9) below to wire-wrap one end of replacement wire to one of the connector pins from which old wire was removed. Then route wire along path of wire that was removed in (3) above. Repeat (7) through (9) below to wire-wrap other end of wire to its respective connector pin.

(6) When unwrapping tool was used to remove wire end in (2) above, cut off end of wire that was wrapped around connector pin. Using cut/strip accessor (A, fig. 3-27), strip 1 inch of insulation from end of wire. Perform (7) through (9) below to wire-wrap end of wire to connector pin from which wire was removed in (2) above.

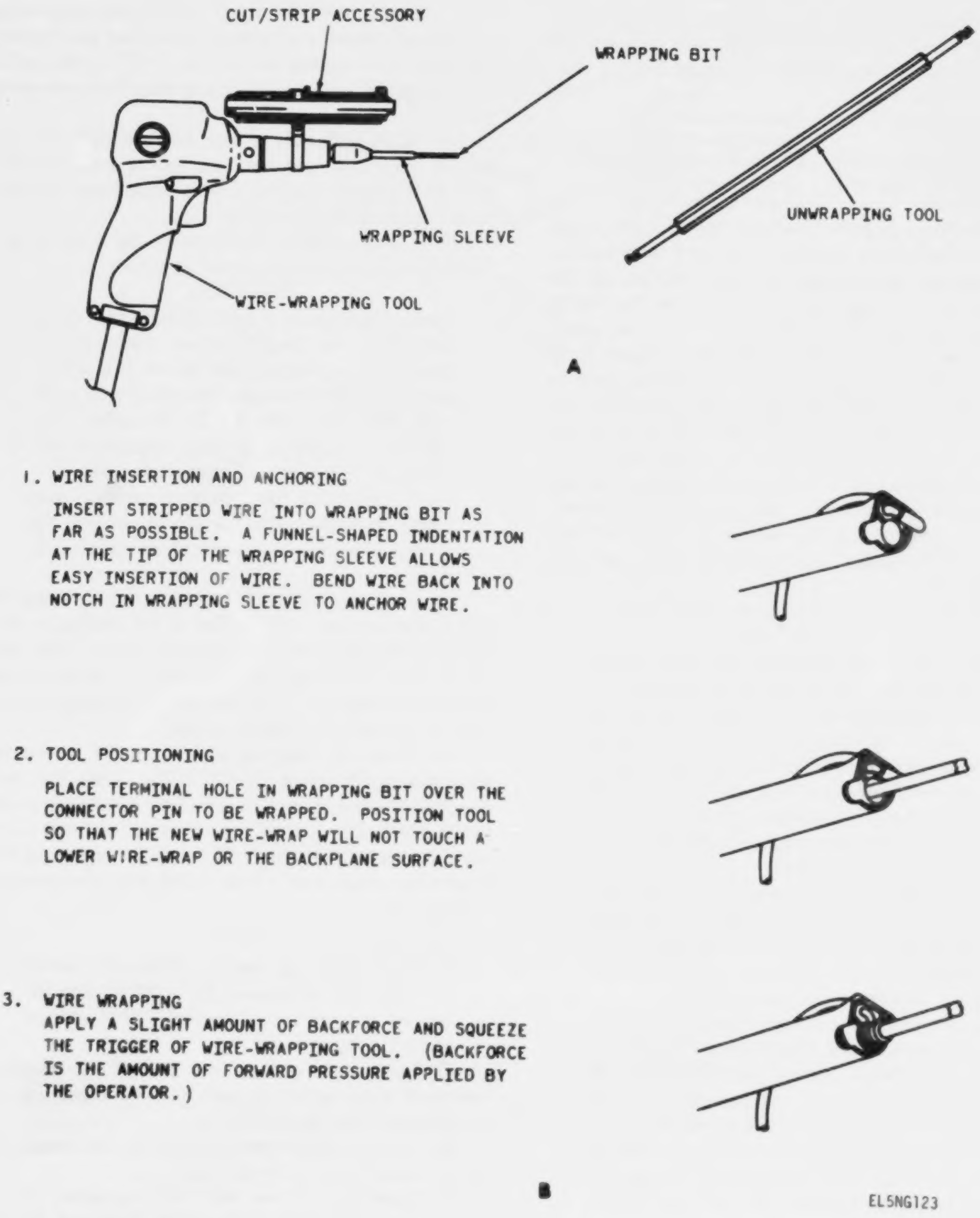
NOTE

In the following steps, wrapping sleeve 507100 and wrapping bit 508748 are installed in wire-wrapping tool 27368AA8 as shown in figure 3-27.

(7) Insert and anchor one end of replacement (stripped) wire as far as possible into small hole of wrapping bit (B1, fig. 3-27).

(8) Position wire-wrapping tool so that wrapping bit is inserted over connector pin.

(9) Carefully position bit over connector pin to depth where first turn of wire-wrap is desired. Do not allow wire-wrap to touch a lower wire-wrap or backplane surface. Momentarily trigger wire-wrapping tool backforce stops and tool runs free. Remove tool from connector pin.


CUT/STRIP ACCESSORY
WRAPPING BIT
WRAPPING SLEEVE
WIRE-WRAPPING TOOL
UNWRAPPING TOOL
A
B
EL5NG123

1. WIRE INSERTION AND ANCHORING

INSERT STRIPPED WIRE INTO WRAPPING BIT AS FAR AS POSSIBLE. A FUNNEL-SHAPED INDENTATION AT THE TIP OF THE WRAPPING SLEEVE ALLOWS EASY INSERTION OF WIRE. BEND WIRE BACK INTO NOTCH IN WRAPPING SLEEVE TO ANCHOR WIRE.

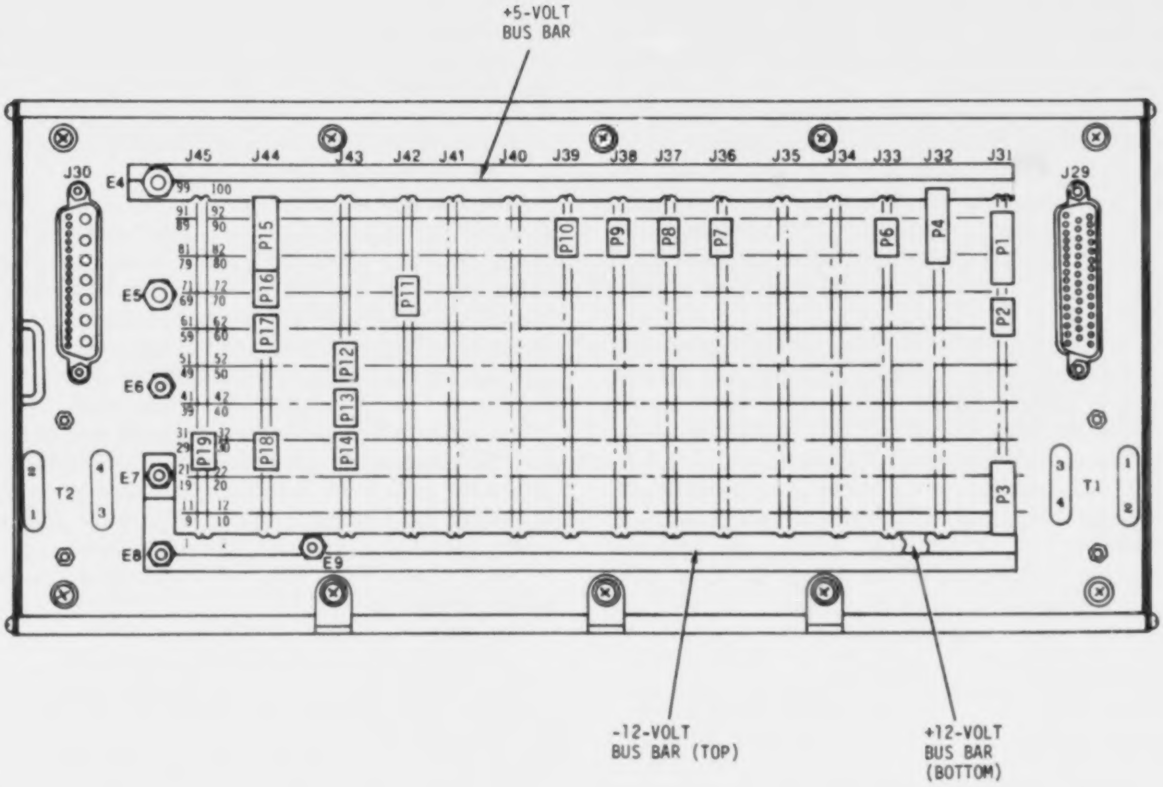
2. TOOL POSITIONING

PLACE TERMINAL HOLE IN WRAPPING BIT OVER THE CONNECTOR PIN TO BE WRAPPED. POSITION TOOL SO THAT THE NEW WIRE-WRAP WILL NOT TOUCH A LOWER WIRE-WRAP OR THE BACKPLANE SURFACE.

3. WIRE WRAPPING

APPLY A SLIGHT AMOUNT OF BACKFORCE AND SQUEEZE THE TRIGGER OF WIRE-WRAPPING TOOL. (BACKFORCE IS THE AMOUNT OF FORWARD PRESSURE APPLIED BY THE OPERATOR.)

Figure 3-27. Wire-wrapping tools and simplified wire installation diagram.


+5-VOLT BUS BAR
J45
J44
J43
J42
J41
J40
J39
J38
J37
J36
J35
J34
J33
J32
J31
J30
J29
E4
E5
E6
E7
E8
E9
99
100
91
92
89
90
81
82
79
80
71
72
69
70
61
62
59
60
51
52
49
50
41
42
39
40
31
32
29
30
21
22
19
20
11
12
9
10
1
P1
P2
P3
P4
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
T1
T2
1
2
3
4
-12-VOLT BUS BAR (TOP)
+12-VOLT BUS BAR (BOTTOM)

NOTES:

1. INTERFACE CONNECTORS P1 THRU P4 AND P6 THRU P19 CONTAIN KEYING PLUGS IN THE FOLLOWING PIN LOCATIONS:

CONN	PIN	CONN	PIN	CONN	PIN
P1	1	P8	9	P14	1
P2	10	P9	9	P15	1
P3	15	P10	9	P16	8
P4	2	P11	6	P17	6
P6	1	P12	8	P18	7
P7	9	P13	2	P19	5

2. TERMINAL E9 IS PART OF BUS BAR CONTAINING PINS E9-1 THRU E9-8.

3. TYPICAL CONNECTOR PIN LOCATION DIAGRAM:

1	3	5	7	9
2	4	6	8	10

10-PIN CONNECTOR

1	3	5	7	9	11	13	15	17	19
2	4	6	8	10	12	14	16	18	20

20-PIN CONNECTOR

EL5NG122

Figure 3-28. Backplane, connector pin location diagram.

(10) Inspect backplane for loose material between connector pins. Ensure that all wires removed from connectors are installed.

(11) Install card file in case (para 3-37*b*).

3-42. Backplane Connector Pin Replacement Procedures

a. General.

(1) There are 100 connector pins 010-7514-503 each in connectors J31 through J45 (fig. 3-28). Each connector pin is installed in a nylon insulator (A of fig. 3-29) that insulates the pin from the backplane with the exception of the pins in locations 5, 6, 95, and 96. Each of these four pins is installed in metal bushing 516-0014-505 that grounds the pin to the backplane. The connector pin in location 1 is installed in a black nylon insulator 302-0002-003. In the other 95 pin

locations, each connector pin is installed to a clear nylon insulator 302-0002-002. When a connector pin is replaced (*c* and *d* below), the associated bushing or insulator is also replaced.

(2) The connector pins in locations 1 through 4 and 97 through 100 of each connector are mechanically bused to the +5-volt, +12-volt, or −12-volt bus bars. Each connector pin is bused to the appropriate bus bar by a power bushing 516-0028-550 as shown in A of figure 3-29. The power bushing is also replaced when the associated connector pin is replaced (*c* and *d* below).

(3) There are eight connector pins 010-7514-503 that can be replaced in the −4.4-volt bus bar. As shown in B of figure 3-29, there are four insulators on the bus bar. Each insulator contains two connector pins that can be replaced (*e* and *f* below).

b. Tools Required for Connector Pin Replacement. Connector repair tool kit 70730090-009 and electrical equipment tool kit TK-105/G contain the tools required for replacement of backplane connector pins. The specific insertion/extraction tools contained in the connector repair kit are listed below.

Tool	*Part No.*
Dynamic bushing insertion tool	Teradyne 600-0107-000
Extraction tool	Teradyne 600-0001-000
Insertion tool	Teradyne 600-0004-000
Insertion tool blade	Teradyne 600-0005-000

c. Connector Pin Removal. Perform the following procedures to remove a connector pin from the backplane.

(1) Remove card file from case (para 3-37*a*).

(2) Remove connector panel (para 3-37*c*).

(3) Remove wires from connector pin(s) to be replaced (para 3-41*e*).

(4) Place tip of extraction tool over faulty pin and slide tool down until it bottoms.

(5) Carefully tap extraction tool until pin dislodges from connector on backplane. Remove pin and its ground bushing or insulator from connector.

NOTE

Perform (6) below when removed connector pin has an associated power bushing installed in the +5-volt, +12-volt, or −12-volt bus bar.

(6) Remove power bushing from bus bar by pulling bushing from backplane with longnose pliers or by pressing bushing out of bus bar with the shank end of a 0.062-inch twist drill.

d. Connector Pin Installation. Perform the following procedures to install a connector pin in the backplane.

(1) Place ground bushing or insulator in connector on backplane.

(2) Insert connector pin in ground bushing or insulator. Ensure that prongs on pin are positioned in the same direction as prongs on adjacent pins.

(3) Using insertion tool with insertion tool blade, place blade in prong of connector pin and slowly push (or tap lightly) on tool until pin bottoms in ground bushing or insulator.

NOTE

Perform (4) below when a power bushing is required on replaced connector pin.

(4) Place power bushing on connector pin. Using dynamic bushing insertion tool, slide power bushing down connector pin until bushing contacts bus bar. When installing bushing in +5-volt or +12-volt bus bar, gently tap tool until bushing is seated in bus bar as shown in figure 3-29 (for +12-volt bus bar it will be necessary to rotate dynamic bushing insertion tool 90 degrees and continue pushing bushing until seated). When installating a bushing a −12-volt bus bar, ensure that bushing is seated in the top-level bus bar as shown in figure 3-29. This is accomplished by carefully seating the bushing to the same depth as adjacent bushing connected into the −12-volt bus bar.

(5) Connect wires removed in *c*(3) above to connect pin(s) (para 3-41*e*).

(6) Install connector panel (para 3-37*c*).

(7) Install card file in case (para 3-37*b*).

e. Connector Pin Removal From −4.4-volt bus bar on the backplane.

(1) Remove card file from case (para 3-37*a*).

(2) Remove connector panel (para 3-37*c*).

(3) Remove wires from connector pin(s) to be replaced (para 3-41*e*).

(4) Remove attaching hardware that secures bus bar to backplane (fig. 3-29).

(5) Carefully remove bus bar from four insulators.

(6) Grasp faulty pin with pair of longnose pliers and push pin until it dislodges from insulator.

f. Connector Pin Insulator in −4.4-Volt Bus Bar. Perform the following procedures to install a connector pin in the −4.4-volt bus bar on the backplane.

(1) Insert connector pin in insulator. Ensure that prongs on pin are positioned in the same direction as prongs on adjacent pins.

(2) Grasp connector pin with pair of longnose pliers and pull pin until it bottoms in insulator.

(3) Install bus bar removed in *e*(5) above in insulators.

(4) Install bus bar on backplane, using hardware removed in *e*(4) above.

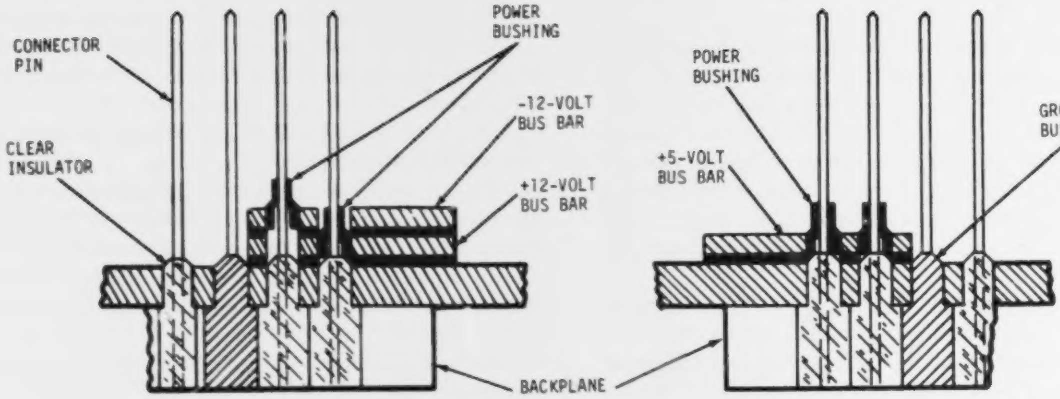
(5) Connect wires removed in *e*(3) above to connector pin(s) (para 3-41*e*).

(6) Install connector panel (para 3-37*c*).

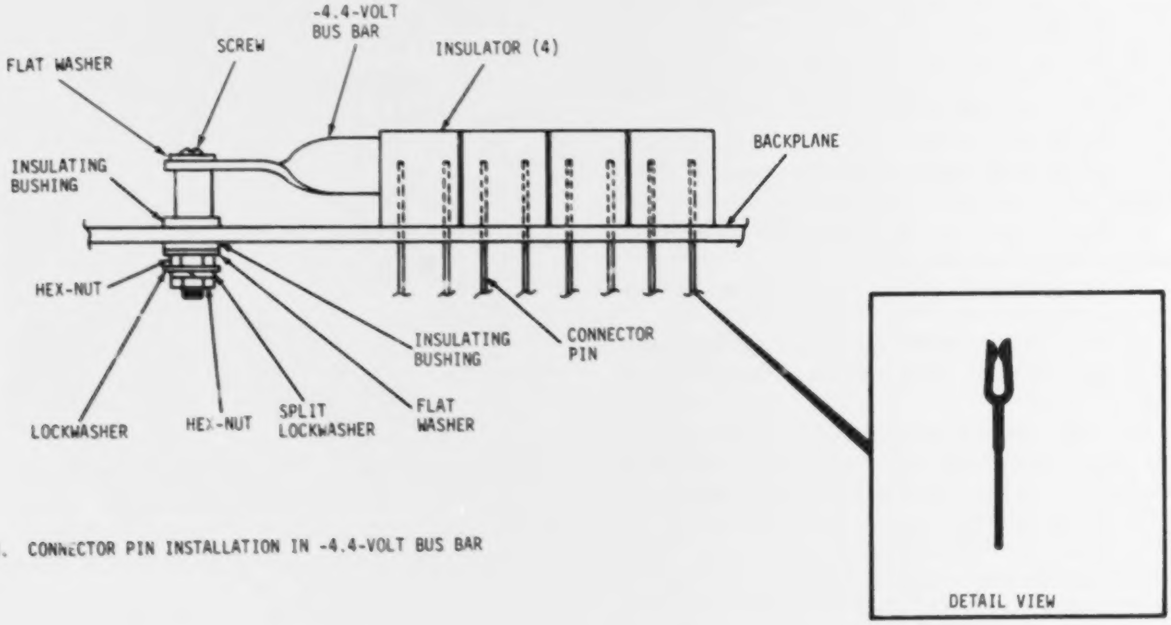
(7) Install card file in case (para 3-37*b*).

3-43. Backplane Interface Connector Repair Procedure

a. General There are 18 interface connectors (P1 through P4 and P6 through P19, fig. 3-28) that plug


CONNECTOR PIN
POWER BUSHING
CLEAR INSULATOR
-12-VOLT BUS BAR
+12-VOLT BUS BAR
POWER BUSHING
GROUND BUSHING
+5-VOLT BUS BAR
BACKPLANE

A. CONNECTOR PIN INSTALLATION IN +5-VOLT, +12-VOLT, AND -12-VOLT BUS BARS


FLAT WASHER
SCREW
-4.4-VOLT BUS BAR
INSULATOR (4)
BACKPLANE
INSULATING BUSHING
HEX-NUT
INSULATING BUSHING
CONNECTOR PIN
LOCKWASHER
HEX-NUT
SPLIT LOCKWASHER
FLAT WASHER
DETAIL VIEW

B. CONNECTOR PIN INSTALLATION IN -4.4-VOLT BUS BAR

EL5NG124

Figure 3-29. Backplane, connector pin installation diagram.

onto connector pins on the backplane. Each interface connector is a 10-pin or a 20-pin connector. As shown in figure 3-30, each interface connector consists of a locking clip housing, one keying plug, and one electrical contact for each functional pin location in the connector. Repair of the interface connector conists of replacing an electrical contact (*c* below), replacing the keying plug (*d* below), or replacing the locking clip housing (*e*) below). The card file must be removed from the case (para 3-37*a*) and the connector panel removed (para 3-37*c*) to gain access to the backplane interface connectors. Install connector panel (para 3-37 *c*) and card file in case (para 3-37*b*) after repair procedures have been completed.

b. Tools Required for Connector Repair. Connector repair tool kit 70730090-009 and electrical equipment tool kit TK-105/G contain the tools required for reapir of backplane interface connectors. The specific extraction and crimp tools contained in the connector repair tool kit are listed below.

Tool	*Part No.*
Certi-crimp tool	AMP 90289-1
Extraction tool	AMP 91084-1

c. Electrical Contact Replacement Procedures. Perform the following procedures to remove and install a replacement electrical contact SM-A-942065 in the locking clip housing.

(1) Remove applicable interface connector from backplane by holding connector housing and pulling connector from backplane pins.

(2) Insert extraction tool in tool slot in housing (fig. 3-30) to mechanically release all contacts from housing.

(3) Remove only the faulty contact from housing. Remove tool from housing.

(4) Using diagonal cutting pliers, cut faulty contact from wire.

(5) Strip between 1/2 and 5/32 inch of insulation from end of wire. Check stripped wire for broken or frayed ends.

(6) Using certi-crimp hand tool, crimp replacement contact to stripped wire. Lightly pull on crimped contact to ensure that crimp is mechanically secure.

(7) Orient electrical contact so the locking tab on contact faces tool slot in housing as shown in figure 3-30. Insert contact in housing until it seats. Lightly pull on contact wire to ensure that contact is properly seated in housing. (Although the contact is free to move in housing, the locking tab prevents the contact from being removed from the housing without the use of the extraction tool.) Ensure that other contacts and keying plug in housing are properly seated.

(8) Install interface connector in appropriate backplane pins.

d. Keying Plug Replacement Procedures. Perform the following procedures to remove and install a replacement keying plug SM-A-942067 in the locking clip housing.

(1) Remove applicable interface connector from backplane by holding connector housing and pulling connector from backplane pins.

(2) Insert extraction tool in tool slot in housing (fig 3-30) to mechanically release all contacts and keying plug.

(3) Remove faulty keying plug from housing. Remove tool from housing.

(4) Orient replacement keying plug so that locking tab on plug faces tool slot in housing as shown in figure 3-30. Insert keying plug in housing until it seats. Lightly pull on plug to ensure that it is properly seated in housing. Ensure that contacts in housing are properly seated.

(5) Install interface connector on appropriate backplane pins.

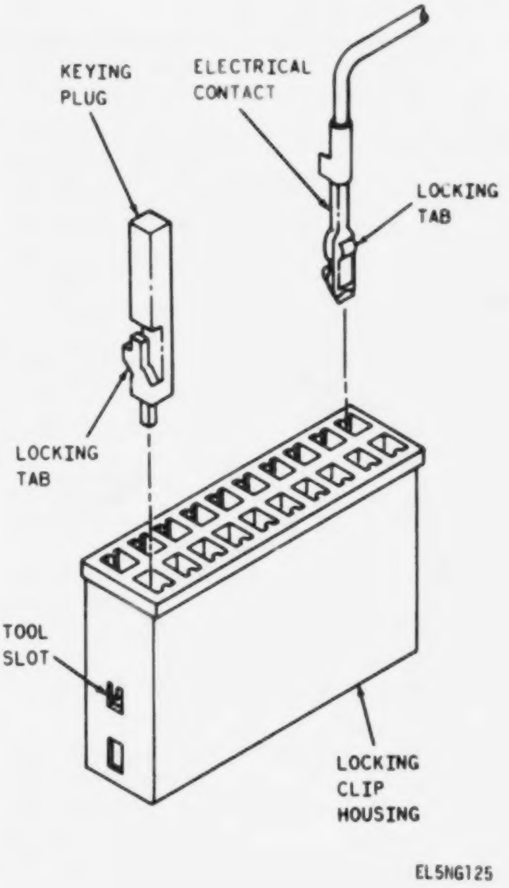


Figure 3-30. Typical interface connector, component location diagram.

e. Locking Clip Housing Replacement Procedures. The replacement procedures consist of removing the keying plug and electrical contacts, one at a time, from the faulty housing and installing the items in the replacement housing. There are four types of housings used on the backplane. The type of housing used by each interface connector is listed and identified in table 3-28. The two 10-pin connectors, SM-A-942068 and SM-A-942147, are identical except that SM-A-942147 has a small protruding key on one end of the housing. The two 20-pin connectors, SM-A-942069 and SM-A-942146, are identical except that SM-A-942146 has a small indented keyway on one end of the housing. Perform the following procedures to replace a faulty locking clip housing.

(1) Remove applicable interface connector from backplane by holding connector housing and pulling connector from backplane pins.

(2) Insert extraction tool in tool slot in housing (fig. 3-30) to mechanically release all contacts and locking plug in housing.

NOTE

Perform (3) through (5) below for keying plug and each electrical contact in the housing, one at a time, to ensure proper positioning of electrical contacts and keying plug in replacement housing.

Table 3-28. Locking Clip Housing Data

Interface connector number	Number of pins	Part number
P1	20	SM-A-942069
P2	10	SM-A-942068
P3	20	SM-A-942069
P4	20	SM-A-942146
P6 through P14	10	SM-A-942068
P15	20	SM-A-942146
P16	10	SM-A-942147
P17 through P19	10	SM-A-942068

(3) Note location of item to be removed and then remove it from housing.

(4) Inspect item for damage. Replace damaged contacts (*c* above). Replace damaged keying plug (*d* above).

(5) Install item in replacement housing location noted in (3) above. Ensure that contacts and keying plug are oriented and installed in housing as shown in figure 3-30. Lightly pull on contact wires to ensure that contacts are properly seated in housing. Lightly pull on plug to ensure that it is properly seated in housing.

(6) Install interface connector on appropriate backplane pins.

3-44. Connector Panel Repair Procedures

a. General. The repair procedures for the connector panel consist of replacing one or more of the components mounted on the panel or performing a wire or connector repair. To gain access to the components and wiring on the connector panel for repair purposes, it is necessary to remove the card file from the case. The connector panel may then be removed from the card file.

b. Tools Required. Electronic equipment tool kit TK-105/G contains the common tools required in the following repair procedures. The connector J25 repair procedures (*g* below) require the following tools from connector repair tool kit 70730090-009.

Tool	*Part No.*
Crimp Tool	M22520/1-01
Crimp turret (used with crimp tool)	M22520/1-02
Extraction tool	MS24256R20
Insertion tool	MS24256A20

c. General Component Replacement Procedures. Perform the following procedures to gain access to the wiring and components on the connector panel. Except for the replacement of the contacts in connector J25 (*g* below), there are no special tools required in the repair of the connector panel.

(1) Remove card file from case (para 3-37*a*).

(2) Remove connector panel from card file frame (para 3-37*c*).

(3) There are no unique procedures required in the replacement of the components on the panel. Some components require the use of adhesive, part substitution, and special attaching hardware as described in *d* through *h* below.

(4) After the connector panel is repaired, attach panel to card file frame (para 3-37*c*).

(5) Install card file in case (para 3-37*b*).

d. Binding Post E3 Replacement Procedures.

(1) Remove E3 from panel.

(2) Discard insulator (SC-B-16499), washer (SC-B-12477), 0-ring (SC-C-16495-3), and washer (MS45901-4) supplied with replacement E3.

(3) Install replacement E3 in panel, using two lockwashers MS35333-73 in place of items discarded in (2) above. Refer to sheet 3 of figure 3-25 for installation of E3 and associated hardware.

e. Lightning Arrester Holder E1 and E2 Replacement Procedures.

(1) Remove faulty E1 or E2.

(2) Clean mating surface on panel where replacement E1 or E2 will be installed.

(3) Coat mating surface with MIL-A-46146, Type I, primer.

(4) After primer dries, coat mating surfaces of panel and E1 or E2 with MIL-A-46146, Type I, adhesive and then install E1 or E2 on panel. Refer to sheet

2 of figure 3-25 for installation of E1 or E2 and associated hardware.

f. Connector J1 through J24, J27, or J28 Replacement Procedures.

(1) Remove faulty connector.

(2) Discard internal-tooth lockwasher supplied with replacement connector and use terminal lockwasher SM-B-603975 when installing connector as shown on sheet 2 of figure 3-25.

(3) When replacing J27 or J28, clean mating surface on panel where replacement connector will be installed. Coat mating surface with MIL-A-46146, Type I, primer. After primer dries, coat mating surfaces of panel and connector with MIL-A-46146, Type I, adhesive and then install connector.

g. Connector J25 Repair Procedures. The repair of J25 consists of replacing faulty wires and faulty contacts (MS3193A20-20A). The special tools required for the replacement of a faulty contact are listed in *b* above. Perform the following steps to replace a faulty contact.

(1) Insert extraction tool in face of connector. Insert tool into connector until it bottoms and closes around faulty contact retaining ring.

(2) Hold tool in position to keep retaining ring closed and then push plunger on tool to push contact out of connector.

(3) Cut damaged contact from wire. Strip between ½ and ¾ inch of insulation from end of wire. Check stripped wire for broken or frayed ends that may prevent a good crimp connection.

(4) Using crimp tool, crimp replacement contact to wire. Ensure that contact is securely connected to wire.

(5) Place insertion tool or replacement contact and position tool tip until it butts against shoulder of contact. Press contact into connector until shoulder of contact snaps in place. Remove tool from connector.

(6) Pull lightly on wire of replaced contact to ensure that contact is properly installed in connector.

h. RFI Filter FL1 Replacement Procedures.

(1) Unsolder wires from FL1. Tag unsoldered wire to ensure that proper connections are made to replacement FL1.

(2) Remove four sets of screws, lockwashers, and flat washers (fig. 3-25, sheet 1) that secure FL1 (J26 POWER IN) to connector panel.

(3) Remove FL1.

(4) Inspect shielding gasket mounted between FL1 and connector panel. If necessary, use new gasket SM-A-942096 when installing replacement FL1.

(5) Install replacement FL1, using screws, lockwashers, and flat washers removed in (2) above.

(6) Solder wires to replacement FL1.

Section X. PRINTED CIRCUIT BOARD REPAIR

3-45. Introduction

This section contains the repair procedures for the printed circuit boards in the RAU and on the front panel. The repair procedures are also applicable to the printed circuit board in the power supply.

3-46. Repair Procedures

Bench top repair center PRC-150A is used for printed circuit board repairs. The PRC-150A contains the soldering tools and accessories needed for circuit board repairs. Use the tools and repair procedures as described in the maintenance and operation manual supplied with the PRC-150A. Follow the repair requirements listed in *a* through *e* below when replacing a component on a circuit board.

a. Moisture Prevention. Any surface or trapped moisture on a circuit board is a potential source of trouble. Perform the following procedures to ensure that moisture is removed from the circuit board.

(1) Inspect board and remove any moisture.

(2) When equipment to be repaired has been stored in a hotter or colder environment, allow it to temperature soak to ambient temperature of work area.

b. Componet Removal. Use a soldering iron with temperature and wattage ratings consistent with the connections to be desoldered; also, use a vacuum-operated solder extraction device to prevent damage to the circuit board and its components.

WARNING

Isopropyl alcohol is highly volatile. Do not use near an open flame or sparks. Keep container closed. Avoid prolonged breathing of vapor. Use in a well-ventilated area.

CAUTION

When removing solder from a component lead, avoid excessive temperatures or prolonged heat application at any given point of contact to prevent serious damage to the lands and pads (terminals) on the printed wiring board.

(1) Carefully remove solder from each lead of component to be removed.

(2) After solder has been vacuumed from a connection point, use a soldering aid and carefully break any solder bridges that may remain between component lead and pad on printed wiring board.

(3) Use longnose pliers or an integrated circuit removal tool, as applicable, and remove component from printed wiring board.

(4) Use isopropyl alcohol and a stiff brush and thoroughly clean board surface in area of removed component.

c. Component Installation. Use a soldering iron with temperature and wattage ratings consistent with the connections to be soldered to prevent damage to the printed wiring board and the component being installed.

(1) Form leads with an appropriate forming tool and cut leads as necessary for proper installation on printed wiring board. Insert leads in pads on board and then gently bend each lead on interconnection side of board. This step ensures that component is retained in proper position during soldering.

CAUTION

When soldering a component lead, avoid excessive temperatures or prolonged heat application at the point of contact to prevent serious damage to the component or board.

(2) Use 60/40 rosin core solder that conforms to Specification QQ-S-571 and carefully solder each lead to the pad.

(3) Use isopropyl alcohol and a stiff brush and thoroughly clean installed component and immediate board areas where soldering was performed.

(4) Inspect board to ensure that all solder splashes, oil, grease, soldering flux, or any other foreign residues are removed from board.

(5) Perform a final cleaning of reparied board areas, using a cotton swab soaked in isopropyl alcohol.

d. Temperature Soak. Temperature soak each repair board as directed in *a* above. The boards should be conformal coated (*e* below) as soon as possible after the temperature soak.

e. Conformal Coating. In these procedures, use a camel-hair brush and a conformal coating that complies with MIL-I-46058, Type JR. Follow the manufacturer's mixing and application instructions to ensure that the conformal coating provides maximum protection to the components and board.

(1) Apply a thin layer of conformal coating to replaced component and surrounding area of board surface that was cleaned or disturbed.

(2) Cure coated board at ambient room temperature or, if practical, at elevated temperature as recommended by conformal coating manufacturer's instructions.

Section XI. WIRE RUN LISTS

3-47. Introduction

This section contains the wire run lists that provide point-to-point wire run information for the major assemblies in the TD-976/G except for the power supply. The major assemblies are defined as the RAU, front panel, power supply, card file, and the backplane in the card file. The wiring data for the power supply is in chapter 4. The wire run lists in this section are listed below. There are two wiring diagrams in this section that support the wire run lists. These wire run lists and wiring diagrams are described in paragraph 3-48.

a. Table 3-29 is the RAU wire run list.

b. Table 3-30 is the front panel wire run list.

c. Table 3-31 is the card file (less backplane) wire run list.

d. Table 3-32 is the card file backplane wire run list.

e. Table 3-33 is the cable marker sleeve marking information.

f. Figure 3-31 is the TD-976/G simplified overall wiring diagram.

g. Figure 3-32 is the interface connector-to-backplane connector wiring diagram matrix.

3-48. Wire Run Lists

a. Use of Wire Run List. Each of the wire run lists in this section contains double-ended wiring entries. As double-ended wiring entries, each wire termination is listed under the "From" column in the list. For example, a wire between TB1-1 and J30-1 will be listed twice in the list. From TB1-1 to J30-2 and from J30-1 to TB1-1. This condition allows the user to use any teminal or pin location on any assembly as the starting point for checking a given wire run. All the entries in the "From" column are listed in alphanumerical order. In turn, the termination point at the opposite end of the wire appears under the "To" column. Except for the RAU wire run list, the wire run lists contain a "Signal name" column. The column lists the signal name or mnemonic code of the functional signal on each wire. The mnemonic codes are defined in table 1-2. The signal names and mnemonic codes are also on the associated input and output terminals or pins of the schematic diagrams in this manual.

b. TD-976/G Simplified Overall Wiring Diagram. Figure 3-31 shows the overall interconnections between the major assemblies in the TD-976/G. The front panel contains a wiring harness that terminates in connectors J3, P1 and P2. Connectors P1 and P2 mate with connectors J29 and J30, respectively, on the card file. Connector J3 mates with connector P1 on the power supply. The RAU requires a system-supplied cable to connect A1J1 to connector J25 on the card file (connector panel). The internal wiring in the card file is basically between the connectors on the connector panel, connectors in the backplane, and discrete components mounted on the card file frame. Interface connectors P1 through P4 and P6 through P19 and 10-pin and 20-pin connectors (fig. 3-28) that mate with selected connector pins of the backplane connectors. The card file wiring is further described in *e* below.

c. RAU Wire Run List. The list in table 3-29 contains the point-to-point wire runs between the components in the RAU. The component locations on the RAU are shown in figure 3-13. The associated schematic diagram is figure FO-19.

d. *Front Panel Wire Run List.* The list in table 3-30 contains the point-to-point wire runs between the components on the front panel. The wiring that makes up the wiring harness between the components on the front panel and connectors P1, P2, and J3 are also in this table. The component locations on the front panel are shown in figure 3-19. The associated schematic diagram is figures FO-17 and FO-18.

e. *Card File and Card File Backplane Wire Run Lists.* The card file wire runs are divided into the card file wire run list in table 3-31 and the card file backplane wire run list in table 3-32. These are explained in (1) and (2) below.

(1) *Card File Wire Run List.* Table 3-31 contains the wiring from connectors J1 through J28 on the connector panel that terminates in one of interface connectors (P1 through P19, less P5) or at one of the terminals in the card file. The table also contains the wiring associated with the card file discrete components (R1, R2, TB1, C1, C2, C3, E1 through E9, and T1 and T2) and connector J30. There are no "J26" entries in the table. The wires associated with J26 are listed as "FL1" entries in the table. For example, the wire from J26-B appears as FL1-B in the table. When tracing a wire run that terminates at a pin in one of the interface connectors (P1 through P19, less P5), the wiring diagram matrix in figure 3-32 is used to locate the connector pin and connector on the backplane that mates with the interface connector. Use of the matrix is described in *f* below. The component locations on the card file are shown in figure 3-25. The associated schematic diagram for the card file is figure FO-20.

(2) *Card File Backplane Wire Run List.* Table 3-32 contains the point-to-point wire runs between backplane connectors J29 and J31 through J45. All the wire terminations in this table are physical wire-wraps to connector pins in one of the backplane connectors. The "Level" column in table 3-32 identifies the location of the wire on the connector pin (fig. 3-26). Figures 3-28 shows the location of backplane connectors J29 ;and J31 through J45 on the backplane in the card file. The figure also shows the physical location of pins 1 through 100 in connectors J31 through J45. Figure 3-28 also shows the locations of interface connectors P1 through P4 and P6 through P19 on the associated backplane connectors. Table 3-32 also lists the wires to terminals E9-1 through E9-6 on the backplane. When a wire run being checked terminates at a connector pin that mates with a pin in an interface connector, the wiring diagram matrix in figure 3-32 must be used to determine the connector pin in the interface connector that is used in the specific wire run being checked. Use of the matrix is described in *f* below.

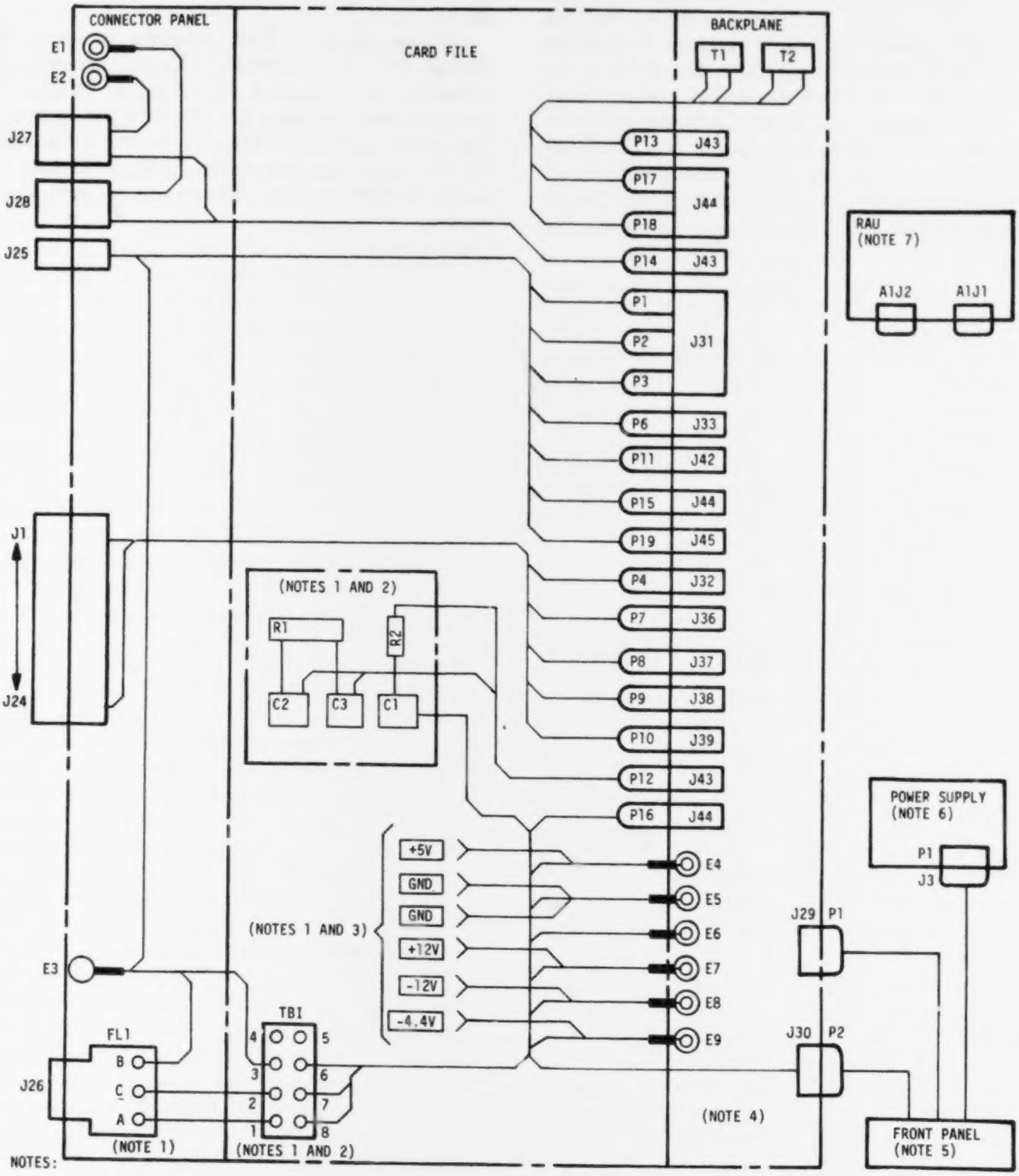
f. *Use of Wiring Diagram Matrix.* The matrix in figure 3-32 shows the pin connections between the pins in interface connectors P1 through P4 and P6 through P19 and the pins in the applicable backplane connectors (J31 through J33, J36 through J39, and J42 through J45). The matrix is used under one of two conditions: When the pin number in one of the interface connectors is known or when one of the pin numbers in one of the backplane connectors is known. Use of the matrix is described in (1) below when a wire run being check in table 3-31 terminates at a pin in one of the interface connectors. Use of the matrix is described in (2) below for checking a wire run when a pin number in one of the backplane connectors is known. The pin number in one of the backplane connectors is selected by one of two conditions: 1) It could be a faulty input or output pin location for the plug-in card installed in a given backplane connector; or 2) it could be the pin and backplane connector identified in table 3-32 as result of checking a given wire run.

(1) Assume the wire run being checked in table 3-31 is from J13-CC to P7-3. Locate interface connector P7 at the top of the matrix in figure 3-32. Observe that P7 mates with backplane connector J36. In the extreme left-hand column, locate pin 3 of the interface connector. Then trace to the right, in the same horizontal row, and locate the pin number that appears under the P7/J36 column. Observe the pin number is 83. Therefore, it is determined that P7-3 mates with J36-83. The wire run check continues by checking pin 83 on the schematic of the plug-in card in connector J36 (DGP card 21A6) and by checking table 3-32 for an entry in the "From" column for J36-83 for any further continuation of the wire run. In this example, there is no entry for J36-83 in table 3-32. Therefore, the wire run terminates at pin 83 of the card that is plugged into connector J36.

(2) Assume that the wire run from pin 90 of the plug-in card in backplane connector J31 (AD card 21A1) is to be checked. First, check table 3-32 to determine if there is any wiring between J31-90 and any other backplane connectors. In this case, there is a wire run between J31-90 and J29-8. Referring to figure 3-31 shows that J29 mates with front panel connector P1. Refer to front panel wire run list in table 3-30 to complete tracing of this segment of the wire run. After checking table 3-32 for possible wire runs between backplane connectors, then refer to figure 3-32 and check for possible wire runs leaving backplane connectors by means of interface connectors. For the above example, figure 3-32 shows that backplane connector J31 appears in the columns under interface connectors P1, P2, and P3. This indicates that the three interface connectors mate with back-

plane connector J31. Locate the specific column under the three J31 columns that contains pin 90. Observe that pin 90 appears under the P1 column. To find the pin in P1 that mates with pin 90 in J31, trace to the left of pin 90, on the same horizontal row, and note that the associated pin in the extreme left-hand column for the interface connector is pin 18. Therefore, backplane connector J31-90 mates with interface connector P1-18. The wire run check is continued by locating P1-18 under the "From" column in table 3-31 which shows a wire run between P1-18 and J25-J.

g. Sleeve Markers. Each interface connector (P1 through P4 and P6 through P18) and the wires connected to TB1-1 through TB1-8 and E3 through E9 contain sleeve markers for identification purposes. The sleeve markers contain the mating information for the connectors and wires. Table 3-33 lists the sleeve markers and the information on each sleeve marker.

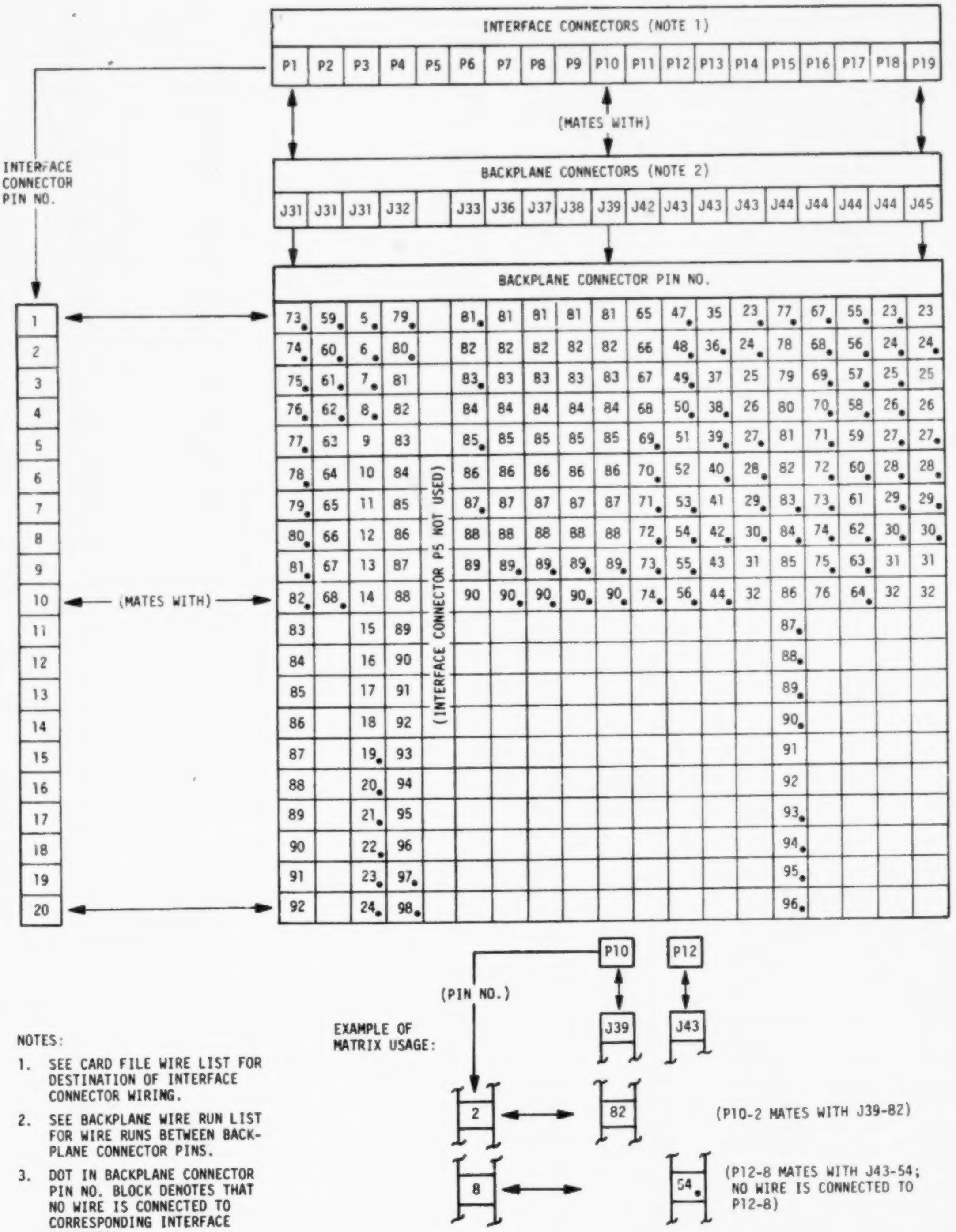

CONNECTOR PANEL
CARD FILE
BACKPLANE
T1
T2
E1
E2
J27
J28
J25
P13
J43
P17
J44
P18
P14
J43
RAU
(NOTE 7)
A1J2
A1J1
P1
P2
J31
P3
P6
J33
P11
J42
P15
J44
P19
J45
J1
J24
(NOTES 1 AND 2)
R1
R2
C2
C3
C1
P4
J32
P7
J36
P8
J37
P9
J38
P10
J39
P12
J43
P16
J44
POWER SUPPLY
(NOTE 6)
P1
J3
+5V
GND
GND
+12V
-12V
-4.4V
(NOTES 1 AND 3)
E4
E5
E6
E7
E8
E9
J29
P1
J30
P2
E3
TB1
FL1
B
C
A
J26
1
2
3
4
5
6
7
8
(NOTE 1)
(NOTES 1 AND 2)
(NOTE 4)
FRONT PANEL
(NOTE 5)

NOTES:

1. WIRE RUNS BETWEEN COMPONENTS ON CONNECTOR PANEL, P1 THRU P4, P6 THRU P19, J30, POWER TEST POINTS, E4 THRU E9, C1, C2, C3, R1, R2, AND TB1 ARE IN CARD FILE WIRE RUN LIST.
2. DISCRETE COMPONENTS C1, C2, C3, R1, R2, AND TB1 ARE MOUNTED ON SIDES OF CARD FILE AS SHOWN IN CARD FILE, COMPONENT LOCATION DIAGRAM.
3. POWER TEST POINTS ARE MOUNTED ON FRONT OF CARD FILE FRAME.
4. WIRE RUNS BETWEEN CONNECTORS J29 AND J31 THRU J45 ARE IN BACKPLANE WIRE RUN LIST.
5. WIRE RUNS BETWEEN FRONT PANEL COMPONENTS ARE IN FRONT PANEL WIRE RUN LIST.
6. WIRE RUNS BETWEEN POWER SUPPLY COMPONENTS ARE IN POWER SUPPLY WIRE RUN LIST.
7. WIRE RUNS BETWEEN RAU COMPONENTS ARE IN RAU WIRE RUN LIST. A1J1 ON RAU IS CONNECTED TO J25 ON CONNECTOR PANEL BY A SYSTEM-SUPPLIED CABLE.

EL5NG126

Figure 3-31. TD-976/G, simplified overall wiring diagram.


INTERFACE CONNECTORS (NOTE 1)
(MATES WITH)
BACKPLANE CONNECTORS (NOTE 2)
INTERFACE CONNECTOR PIN NO.
BACKPLANE CONNECTOR PIN NO.
(MATES WITH)
(INTERFACE CONNECTOR P5 NOT USED)
EXAMPLE OF MATRIX USAGE:
(PIN NO.)
P10
P12
J39
J43
2
82
8
54•
(P10-2 MATES WITH J39-82)
(P12-8 MATES WITH J43-54; NO WIRE IS CONNECTED TO P12-8)
EL5NG127

INTERFACE CONNECTORS (NOTE 1)	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19
BACKPLANE CONNECTORS (NOTE 2)	J31	J31	J31	J32		J33	J36	J37	J38	J39	J42	J43	J43	J43	J44	J44	J44	J44	J45
INTERFACE CONNECTOR PIN NO.	BACKPLANE CONNECTOR PIN NO.																		
1	73•	59•	5•	79•	(INTERFACE CONNECTOR P5 NOT USED)	81•	81	81	81	81	65	47•	35	23•	77•	67•	55•	23•	23
2	74•	60•	6•	80•		82	82	82	82	82	66	48•	36•	24•	78	68•	56•	24•	24•
3	75•	61•	7•	81		83•	83	83	83	83	67	49•	37	25	79	69•	57•	25•	25
4	76•	62•	8•	82		84	84	84	84	84	68	50•	38•	26	80	70•	58•	26•	26
5	77•	63	9	83		85•	85	85	85	85	69•	51	39•	27•	81	71•	59	27•	27•
6	78•	64	10	84		86	86	86	86	86	70•	52	40•	28•	82	72•	60•	28•	28•
7	79•	65	11	85		87•	87	87	87	87	71•	53•	41	29•	83•	73•	61	29•	29•
8	80•	66	12	86		88	88	88	88	88	72•	54•	42•	30•	84•	74•	62•	30•	30•
9	81•	67	13	87		89	89•	89•	89•	89•	73•	55•	43	31	85	75•	63•	31	31
10	82•	68•	14	88		90	90•	90•	90•	90•	74•	56•	44•	32	86	76	64•	32	32
11	83		15	89											87•				
12	84		16	90											88•				
13	85		17	91											89•				
14	86		18	92											90•				
15	87		19•	93											91				
16	88		20•	94											92				
17	89		21•	95											93•				
18	90		22•	96											94•				
19	91		23•	97•											95•				
20	92		24•	98•											96•				

NOTES:

1. SEE CARD FILE WIRE LIST FOR DESTINATION OF INTERFACE CONNECTOR WIRING.
2. SEE BACKPLANE WIRE RUN LIST FOR WIRE RUNS BETWEEN BACKPLANE CONNECTOR PINS.
3. DOT IN BACKPLANE CONNECTOR PIN NO. BLOCK DENOTES THAT NO WIRE IS CONNECTED TO CORRESPONDING INTERFACE CONNECTOR.

Figure 3-32. Interface connector-to-backplane connector wiring diagram matrix.

Table 3-29. RAU Wire Run List

From[1]	To[1]
A1E1	J4-4
A1E2	J4-1
A1E3	J5-4
A1E4	J5-1
A1E5	S1-4
A1E6	S1-2
A1E6	S1-5
A1E7	J1-1
A1E8	S1-3
A1E9	S4-5
A1E10	J2-1
A1E11	J1-4
A1E12	J2-4
A1E13	S2-2
A1E14	DS3-1
A1E15	DS2-1
A1E16	J3-A
A1E17	S5-1
A1E18	S5-3
A1E19	S4-6
A1E20	S4-3
A1E21	S4-1
A1E22	S3-1
A1E23	S3-3
A1E24	S2-1
A1E25	S2-3
A1E26	DS1-1
DS1-1	A1E26
DS1-2 (C)	S2-2
DS1-2 (C)	S3-2
DS2-1	A1E15
DS2-2 (C)	DS3-2
DS2-2 (C)	S5-2
DS3-1	A1E14
DS3-2 (C)	DS2-2 (C)
DS3-2 (C)	S4-2
J1-1	A1E7
J1-4	A1E11
J2-1	A1E10
J2-4	A1E12
J3-A	A1E16
J3-B	S5-2
J3-C	S5-6
J4-1	A1E2
J4-4	A1E1
J5-1	A1E4
J5-4	A1E3
S1-1	S1-3
S1-2	A1E6
S1-3	A1E8
S1-3	S1-1
S1-4	A1E5
S1-5	A1E6
S2-1	A1E24
S2-2	DS1-2 (C)
S2-2	A1E13
S2-3	A1E25
S3-1	A1E22
S3-2	DS1-2 (C)
S3-2	S4-2
S3-3	A1E23
S4-1	A1E21
S4-2	DS3-2 (C)
S4-2	S3-2
S4-3	A1E20
S4-5	A1E9
S4-5	S5-5
S4-6	S5-6
S4-6	A1E19
S5-1	A1E17
S5-2	DS2-2 (C)
S5-2	J3-B
S5-3	A1E18
S5-5	S4-5
S5-6	J3-C
S5-6	S4-6

[1] (C) Denotes cathode.

Table 3-30. Front Panel Wire Run List

From	To	Signal name
A1E1	P2-11	TCP
A1E2	XDS5-1	--[1]
A1E3	J3-7	DC INDICATOR ENABLE
A1E4	XDS5-2	+5VDC
A1E5	S8-3	--[1]
A1E6	XDS4-1	--[1]
A1E7	P1-45	PWRLT
A1E8	XDS4-2	--[1]
A1E9	XDS3-1	--[1]
A1E10	P2-13	RCP
A1E11	XDS3-2	--[1]
A1E12	S8-5	--[1]
A1E13	P1-1	FTLB1
A1E14	P1-2	FTLB2
A1E15	P1-3	FTLB4
A1E16	P1-4	FTLB8
A1E17	P1-5	FTLB16
A1E18	S8-1	GND
A1E26	P1-29	OCH8LPS
A1E27	P1-6	ICH8LPS
A1E28	P1-28	OCH7LPS
A1E29	P1-7	ICH7LPS
A1E30	P1-27	OCH6LPS
A1E31	P1-8	ICH6LPS
A1E32	P1-9	ICH5LPS
A1E33	P1-26	OCH5LPS
A1E34	P1-25	OCH4LPS
A1E35	P1-10	ICH4LPS
A1E36	P1-11	ICH3LPS
A1E37	P1-24	OCH3LPS
A1E38	P1-12	ICH2LPS
A1E39	P1-23	OCH2LPS
A1E40	P1-13	ICH1LPS
A1E41	P1-22	OCH1LPS
A1E42	P1-30	AVCALS
A1E43	XDS1-1	--[1]
A1E44	XDS2-2	+5VDC
A1E45	XDS1-2	+5VDC
A1E46	XDS2-1	--[1]
A1E47	P1-31	DVCALS
A1E48	P1-21	DMLPS
A1E49	P1-14	SGCLPS
A1E50	P1-15	SGSLPS
A1E51	P1-20	EQLPS
A1E52	S3-C (1)	GND
A1E52	P2-15	GND
A1E53	P2-16	+5VDC
C1-1	J2-A	LEAR
C1-2	E2	GND
C2-1	J2-C	LMIC
C2-2	E2	GND
C3-1	S5-3	LDTL−
C3-2	E2	GND
E1	STP 1	GND
E2	J2-B	GND
E2	C1-2	GND
E2	C2-2	GND
E2	C3-2	GND
E2	STP 4	GND
E2	STP 6	GND
J1-CC	P1-41	TLFOM
J2-A	C1-1	LEAR
J2-A	P1-32	LEAR
J2-B	E2	GND
J2-C	C2-1	LMIC
J2-C	P1-38	LMIC
J3-1	P2-1	REF
J3-2	P2-2	FMDG
J3-3	P2-6	−4.4VDC
J3-4	P2-4	45 MA (−)
J3-6	L1-2	45 MA CURRENT (+)
J3-7	A1E3	DC INDICATOR ENABLE
J3-8	J3-9	+12VDC
J3-9	J3-8	+12VDC
J3-10	J3-11	NOT USED
J3-11	J3-10	NOT USED
J3-13	J3-15	−4.4VDC
J3-15	J3-13	−4.4VDC
J3-16	J3-17	−12VDC
J3-17	J3-16	−12VDC
J3-A1	XF2-2	ACHOTO
J3-A2	XF1-2	ACNEUTO
J3-A3	P2-A3	+12VDC
J3-A4	P2-A4	−12VDC
J3-A5	P2-A5	GND
J3-A6	P2-A6	GND
J3-A7	P2-A7	+5VDC
L1-1	R1-1	45 MA CURRENT (+)
L1-1	S8-2	45 MA CURRENT (+)
L1-2	J3-6	45 MA CURRENT (+)
L1-2	R1-2	45 MA CURRENT (+)
P1-1	A1E13	FTLB1
P1-2	A1E14	FTLB2
P1-3	A1E15	FTLB4
P1-4	A1E16	FTLB8
P1-5	A1E17	FTLB16
P1-6	A1E27	ICH8LPS
P1-7	A1E29	ICH7LPS
P1-8	A1E31	ICH6LPS
P1-9	A1E32	ICH5LPS
P1-10	A1E35	ICH4LPS
P1-11	A1E36	ICH3LPS
P1-12	A1E38	ICH2LPS
P1-13	A1E40	ICH1LPS
P1-14	A1E49	SGCLPS
P1-15	A1E50	SGSLPS
P1-16	S1-2	GND
P1-17	S2-2	GND
P1-18	S2-1	CFNRM−
P1-19	S1-3	LOOP−
P1-20	A1E51	EQLPS
P1-21	A1E48	DMLPS
P1-22	A1E41	OCH1LPS
P1-23	A1E39	OCH2LPS
P1-24	A1E37	OCH3LPS
P1-25	A1E34	OCH4LPS
P1-26	A1E33	OCH5LPS
P1-27	A1E30	OCH6LPS
P1-28	A1E28	OCH7LPS
P1-29	A1E26	OCH8LPS
P1-30	A1E42	AVCALS
P1-31	A1E47	DVCALS

See footnote at end of table.

Table 3-30. Front Panel Wire Run List—Continued

From	To	Signal name
P1-32	J2-A	LEAR
P1-33	STP 3	GND
P1-34	S5-4	AVRNG-
P1-35	S5-6	DVRNG-
P1-36	S5-1	LATL-
P1-37	S5-3	LDTL-
P1-38	J2-C	LMIC
P1-39	STP 5	GND
P1-40	S4-NO (1)	INAT
P1-41	J1-CC	TLFOM
P1-42	STP 2	GND
P1-43	S3-NO (1)	AARSSW
P1-44	XLS1 (-)	AALRM-
P1-45	A1E7	PWRLT
P2-1	J3-1	REF
P2-2	J3-2	FMDG
P2-4	J3-4	45 MA (-)
P2-6	J3-3	-4.4VDC
P2-7	S2-4	PDET
P2-8	S2-5	GND
P2-11	A1E1	TCP
P2-12	S8-6	GND
P2-13	A1E10	RCP
P2-15	A1E52	DC GND
P2-16	A1E53	+5VDC
P2-17	S4-C (1)	+12VDC
P2-A1	S9-6	ACHOT
P2-A2	S9-3	ACNEUT
P2-A3	J3-A3	+12VDC
P2-A4	J3-A4	-12VDC
P2-A5	J3-A5	GND
P2-A6	J3-A6	GND
P2-A7	J3-A7	+5VDC
R1-1	L1-1	45 MA CURRENT (+)
R1-2	L1-2	45 MA CURRENT (+)
S1-2	P1-16	GND
S1-3	P1-19	LOOP-
S2-1	P1-18	CFNRM-
S2-2	P1-17	GND
S2-4	P2-7	PDET
S2-5	P2-8	GND
S3-C (1)	S7-2	GND
S3-C (1)	A1E52	GND
S3-NO (1)	P1-43	AARSSW
S4-C (1)	XLS1 (+)	+12VDC
S4-C (1)	P2-17	+12VDC
S4-NO (1)	P1-40	INAT
S5-1	P1-36	LATL-
S5-2	S7-3	--[1]
S5-3	C3-1	LDTL-
S5-3	P1-37	LDTL-
S5-4	P1-34	AVRNG-
S5-5	S7-1	--[1]
S5-6	P1-35	DVRNG-
S7-1	S5-5	--[1]
S7-2	S3-C (1)	GND
S7-3	S5-2	--[1]
S8-1	S8-6	GND
S8-1	A1E18	GND
S8-2	L1-1	45 MA CURRENT (+)
S8-3	S8-4	--[1]
S8-3	A1E5	--[1]
S8-4	S8-3	--[1]
S8-5	A1E12	--[1]
S8-6	S8-1	GND
S8-6	P2-12	GND
S9-2	XF1-1	
S9-3	P2-A2	ACNEUT
S9-5	XF2-1	--[1]
S9-6	P2-A1	ACHOT
STP 1	E1	GND
STP 2	P1-42	GND
STP 3	P1-33	GND
STP 4	E2	GND
STP 5	P1-39	GND
STP 6	E2	GND
XDS1-1	A1E43	--[1]
XDS1-2	A1E45	+5VDC
XDS2-1	A1E46	--[1]
XDS2-2	A1E44	+5VDC
XDS3-1	A1E9	--[1]
XDS3-2	A1E11	--[1]
XDS4-1	A1E6	--[1]
XDS4-2	A1E8	--[1]
XDS5-1	A1E2	--[1]
XDS5-2	A1E4	+5VDC
XDS6-1	XF2-2	ACHOTO
XDS6-2	XF1-2	ACNEUTO
XF1-1	S9-2	--[1]
XF1-2	J3-A2	ACNEUTO
XF1-2	XDS6-2	ACNEUTO
XF2-1	S9-5	--[1]
XF2-2	J3-A1	ACHOTO
XF2-2	XDS6-1	ACHOTO
XLS1 (-)	P1-44	AALRM-
XLS1 (+)	S4-C (1)	+12VDC

[1] Signal name not assigned to internal wiring. See front panel schematic diagram for functional usage.

Table 3-31. Card File Wire Run List

From	To	Signal name
C1-2	J30-11	TCP
C1-2	T1-4	TCP
C2-1	R1	—[1]
C2-2	J30-07	PDET
C2-2	P12-5	PDET
C3-1	P12-6	GND
C3-1	J30-08	GND
C3-2	R1	—[1]
E1	J28-CC	SGIN1
E2	J27-CC	SGOUT1
E3	TB1-3	FMGD
E3	FL1-B	FMGD
E3	J25-A	FMGD
E4	J30-16	+5VDC
E4	J30-A7	+5VDC
E4	TP+5V	+5VDC
E5	J30-A5	GND
E5	J30-A6	GND
E5	TP-GND	GND
E5	TP-GND	GND
E6	J30-02	FMGD
E6	J30-12	FMGD
E6	J30-15	FMGD
E6	R2-2	FMGD
E6	TB1-6	FMGD
E7	J30-17	+12VDC
E7	J30-A3	+12VDC
E7	TP+12V	+12VDC
E8	TP−12V	−12VDC
E8	J30-A4	−12VDC
E9	TP−4.4V	−4.4VDC
E9	J30-06	−4.4VDC
FL1-A	TB1-1	ACHOT
FL1-B	E3	FMGD
FL1-C	TB1-2	ACNEUT
J1-CC	P4-8	PCMGP1
J1-STP	STP-1	PCMGP1G
J2-CC	P4-7	PCMGP2
J2-STP	STP-3	PCMGP2G
J3-CC	P4-15	PCMGP3
J3-STP	STP-5	PCMGP3G
J4-CC	P4-11	PCMGP4
J4-STP	STP-7	PCMGP4G
J5-CC	P4-16	PCMGP5
J5-STP	STP-9	PCMGP5G
J6-CC	P4-3	PCMGP6
J6-STP	STP-11	PCMGP6G
J7-CC	P4-12	PCMGP7
J7-STP	STP-13	PCMGP7G
J8-CC	P4-4	PCMGP8
J8-STP	STP-15	PCMGP8G
J9-CC	P7-5	OGRPD1
J9-STP	STP-17	OGRPG1
J10-CC	P8-5	OGRPD2
J10-STP	STP-19	OGRPG2
J11-CC	P9-5	OGRPD3
J11-STP	STP-21	OGRPG3
J12-CC	P10-5	OGRPD4
J12-STP	STP-23	OGRPG4
J13-CC	P7-3	OGRPD5
J13-STP	STP-25	OGRPG5
J14-CC	P8-3	OGRPD6
J14-STP	STP-27	OGRPG6
J15-CC	P9-3	OGRPD7
J15-STP	STP-29	OGRPG7
J16-CC	P10-3	OGRPD8
J16-STP	STP-31	OGRPG8
J17-CC	P7-7	OGRP1TM
J17-STP	STP-33	OGRP1TG
J18-CC	P8-7	OGRP2TM
J18-STP	STP-35	OGRP2TG
J19-CC	P9-7	OGRP3TM
J19-STP	STP-37	OGRP3TG
J20-CC	P10-7	OGRP4TM
J20-STP	STP-39	OGRP4TG
J21-CC	P7-1	OGRP5TM
J21-STP	STP-41	OGRP5TG
J22-CC	P8-1	OGRP6TM
J22-STP	STP-43	OGRP6TG
J23-CC	P9-1	OGRP7TM
J23-STP	STP-45	OGRP7TG
J24-CC	P10-1	OGRP8TM
J24-STP	STP-47	OGRP8TG
J25-A	E3	FMGD
J25-B	P3-9	ICH1LPS
J25-C	P19-10	DVEXO
J25-D	P6-8	D12I
J25-E	P6-10	DDI−
J25-F	P6-9	D75I
J25-G	P1-17	DMLPS
J25-H	P3-7	ICH4LPS
J25-J	P1-18	ICH6LPS
J25-K	P11-4	DDRV−
J25-L	P6-2	DDSD−
J25-M	P3-14	OCH6LPS
J25-N	P2-9	ICH5LPS
J25-P	P2-6	ICH7LPS
J25-R	P6-4	DDRY−
J25-T	P2-5	DDCALS
J25-U	P15-9	PTT−
J25-V	P2-8	EQLPS
J25-W	P1-14	OCH1LPS
J25-X	P15-10	RDTL−
J25-Y	P19-9	DVEXO−
J25-Z	P3-6	EXAT
J25-a	P3-8	ICH8LPS
J25-b	P3-13	SGSLPS
J25-c	P15-2	AVRNG−
J25-d	P1-20	OCH3LPS
J25-e	P6-6	DDRG−
J25-f	P3-12	OCH7LPS
J25-g	P1-16	OCH4LPS
J25-h	P19-3	DVEXI
J25-i	P15-15	DC GND
J25-j	P1-13	OCH5LPS
J25-k	P19-4	GND
J25-m	P15-16	CMBUS
J25-n	P1-12	SGCLPS
J25-p	P11-2	D75O
J25-r	P2-7	CNSAUD−

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[1] See footnote at end of table.

Table 3-31. Card File Wire Run List—Continued

From	To	Signal name
J25-s	P15-5	REAR
J25-t	P1-19	RDVCALS
J25-u	P1-15	OCH2LPS
J25-v	P3-10	ICH2LPS
J25-w	P11-3	D120−
J25-x	P19-1	DVEXI−
J25-y	P15-4	RMIC
J25-z	P15-6	RATL−
J25-AA	P15-3	DVRNG−
J25-BB	P3-11	RAVCALS
J25-CC	P1-11	OCHBLPS
J25-DD	P3-5	ICH3LPS
J25-EE	P11-1	D120
J27-CC	E2	SGOUT1
J27-CC	P14-9	SGOUT1
J27-STP	STP-49	SGOUT2
J28-CC	E1	SGIN1
J28-CC	P14-3	SGIN1
J28-STP	STP-51	SGIN2
J30-A1	TB1-8	ACHOT
J30-A2	TB1-7	ACNEUT
J30-A3	E7	+12VDC
J30-A4	E8	−12VDC
J30-A5	E5	GND
J30-A6	E5	GND
J30-A7	E4	+5VDC
J30-01	P16-10	REF
J30-02	E6	FMGD
J30-04	R2-2	45 MA−
J30-06	E9	−4.4VDC
J30-07	C2-2	PDET
J30-08	C3-1	GND
J30-11	C1-2	TCP
J30-12	E6	FMGD
J30-13	T2-4	RCP
J30-15	E6	GND
J30-16	E4	+5VDC
J30-17	E7	+12VDC
P1-11	J25-CC	OCH8LPS
P1-12	J25-n	SGCLPS
P1-13	J25-j	OCH5LPS
P1-14	J25-W	OCH1LPS
P1-15	J25-u	OCH2LPS
P1-16	J25-g	OCH4LPS
P1-17	J25-G	DMLPS
P1-18	J25-J	ICH6LPS
P1-19	J25-t	RDVCALS
P1-20	J25-d	OCH3LPS
P2-5	J25-T	DDCALS
P2-6	J25-P	ICH7LPS
P2-7	J25-r	CNSAUD−
P2-8	J25-V	EQLPS
P2-9	J25-N	ICH5LPS
P3-5	J25-DD	ICH3LPS
P3-6	J25-Z	EXAT
P3-7	J25-H	ICH4LPS
P3-8	J25-a	ICH8LPS
P3-9	J25-B	ICH1LPS
P3-10	J25-v	ICH2LPS
P3-11	J25-BB	RAVCALS
P3-12	J25-f	OCH7LPS
P3-13	J25-b	SGSLPS
P3-14	J25-M	OCH6LPS
P4-3	J6-CC	PCMGP6
P4-4	J8-CC	PCMGP8
P4-5	STP-12	PCMGP6G
P4-6	STP-16	PCMGP8G
P4-7	J2-CC	PCMGP2
P4-8	J1-CC	PCMGP1
P4-9	STP-4	PCMGP2G
P4-10	STP-2	PCMGP1G
P4-11	J4-CC	PCMGP4
P4-12	J7-CC	PCMGP7
P4-13	STP-8	PCMGP4G
P4-14	STP-14	PCMGP7G
P4-15	J3-CC	PCMGP3
P4-16	J5-CC	PCMGP5
P4-17	STP-6	PCMGP3G
P4-18	STP-10	PCMGP5G
P6-2	J25-L	DDSD−
P6-4	J25-R	DDRY−
P6-6	J25-e	DDRG−
P6-8	J25-D	D12I
P6-9	J25-F	D75I
P6-10	J25-E	DDI−
P7-1	J21-CC	OGRP5TM
P7-2	STP-42	OGRP5TG
P7-3	J13-CC	OGRPD5
P7-4	STP-26	OGRPG5
P7-5	J9-CC	OGRPD1
P7-6	STP-18	OGRPG1
P7-7	J17-CC	OGRP1TM
P7-8	STP-34	OGRP1TG
P8-1	J22 C	OGRP6TM
P8-2	STP-44	OGRP6TG
P8-3	J14-CC	OGRPD6
P8-4	STP-28	OGRPG6
P8-5	J10-CC	OGRPD2
P8-6	STP-20	OGRPG2
P8-7	J18-CC	OGRP2TM
P8-8	STP-36	OGRP2TG
P9-1	J23-CC	OGRP7TM
P9-2	STP-46	OGRP7TG
P9-3	J15-CC	OGRPD7
P9-4	STP-30	OGRPG7
P9-5	J11-CC	OGRPD3
P9-6	STP-22	OGRPG3
P9-7	J19-CC	OGRP3TM
P9-8	STP-38	OGRP3TG
P10-1	J24-CC	OGRP8TM
P10-2	STP-48	OGRP8TG
P10-3	J16-CC	OGRPD8
P10-4	STP-32	OGRPG8
P10-5	J12-CC	OGRPD4
P10-6	STP-24	OGRPG4
P10-7	J20-CC	OGRP4TM
P10-8	STP-40	OGRP4TG
P11-1	J25-EE	D120
P11-2	J25-p	D750
P11-3	J25-w	D120−
P11-4	J25-K	DDRV−
P12-5	C2-2	PDET

Table 3-31. Card File Wire Run List—Continued

From	To	Signal name
P12-6	C3-1	GND
P13-1	T2-3	RAVCP
P13-3	T1-3	TAVCP
P13-7	T1-4	TCP
P13-9	T2-4	RCP
P14-3	J28-CC	SGIN1
P14-4	STP-52	SGIN2
P14-9	J27-CC	SGOUT1
P14-10	STP-50	SGOUT2
P15-2	J25-c	AVRNG−
P15-3	J25-AA	DVRNG−
P15-4	J25-y	RMIC
P15-5	J25-s	REAR
P15-6	J25-z	RATL−
P15-9	J25-U	PTT−
P15-10	J25-X	RDTL−
P15-15	J25-i	DC GND
P15-16	J25-m	CMBUS
P16-10	J30-01	REF
P17-5	T2-1	RAVOW1
P17-7	T2-2	RAVOW2
P18-9	T1-1	TAVOW1
P18-10	T1-2	TAVOW2
P19-1	J25-x	DVEXI−
P19-3	J25-h	DVEXI
P19-4	J25-k	GND
P19-9	J25-Y	DVEXO−
P19-10	J25-C	DVEXO
R1	C2-1	—[1]
R1	C3-2	—[1]
R2-2	E6	FMGD
R2-2	J30-04	45 MA−
STP-1	J1-STP	PCMGP1G
STP-2	P4-10	PCMGP1G
STP-3	J2-STP	PCMGP2G
STP-4	P4-9	PCMGP2G
STP-5	J3-STP	PCMGP3G
STP-6	P4-17	PCMGP3G
STP-7	J4-STP	PCMGP4G
STP-8	P4-13	PCMGP4G
STP-9	J5-STP	PCMGP5G
STP-10	P4-18	PCMGP5G
STP-11	J6-STP	PCMGP6G
STP-12	P4-5	PCMGP6G
STP-13	J7-STP	PCMGP7G
STP-14	P4-14	PCMGP7G
STP-15	J8-STP	PCMGP8G
STP-16	P4-6	PCMGP8G
STP-17	J9-STP	OGRPG1
STP-18	P7-6	OGRPG1
STP-19	J10-STP	OGRPG2
STP-20	P8-6	OGRPG2
STP-21	J11-STP	OGRPG3
STP-22	P9-6	OGRPG3
STP-23	J12-STP	OGRPG4
STP-24	P10-6	OGRPG4
STP-25	J13-STP	OGRPG5
STP-26	P7-4	OGRPG5
STP-27	J14-STP	OGRPG6
STP-28	P8-4	OGRPG6
STP-29	J15-STP	OGRPG7
STP-30	P9-4	OGRPG7
STP-31	J16-STP	OGRPG8
STP-32	P10-4	OGRPG8
STP-33	J17-STP	OGRP1TG
STP-34	P7-8	OGRP1TG
STP-35	J18-STP	OGRP2TG
STP-36	P8-8	OGRP2TG
STP-37	J19-STP	OGRP3TG
STP-38	P9-8	OGRP3TG
STP-39	J20-STP	OGRP4TG
STP-40	P10-8	OGRP4TG
STP-41	J21-STP	OGRP5TG
STP-42	P7-2	OGRP5TG
STP-43	J22-STP	OGRP6TG
STP-44	P8-2	OGRP6TG
STP-45	J23-STP	OGRP7TG
STP-46	P9-2	OGRP7TG
STP-47	J24-STP	OGRP8TG
STP-48	P10-2	OGRP8TG
STP-49	J27-STP	SGOUT2
STP-50	P14-10	SGOUT2
STP-51	J28-STP	SGIN2
STP-52	P14-4	SGIN2
T1-1	P18-9	TAVOW1
T1-2	P18-10	TAVOW2
T1-3	P13-3	TAVCP
T1-4	P13-7	TCP
T1-4	C1-2	TCP
T2-1	P17-5	RAVOW1
T2-2	P17-7	RAVOW2
T2-3	P13-1	RAVCP
T2-4	P13-9	RCP
T2-4	J30-13	RCP
TB1-1	FL1-A	ACHOT
TB1-2	FL1-C	ACNEUT
TB1-3	E3	FMGD
TB1-6	E6	FMGD
TB1-7	J30-A2	ACNEUT
TB1-8	J30-A1	ACHOT
TP-GND	E5	GND
TP-GND	E5	GND
TP+5V	E4	+5VDC
TP+12V	E7	+12VDC
TP−12V	E8	−12VDC
TP−4.4V	E9	−4.4VDC

[1] Signal name not assigned to internal wiring. See front panel schematic diagram for functional usage.

Table 3-32. Card File Backplane Wire Run List

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
E9-1	1	J35-93	1	–4.4VDC
E9-1	2	J35-94	1	–4.4VDC
E9-2	1	J36-93	1	–4.4VDC
E9-2	2	J36-94	1	–4.4VDC
E9-3	1	J37-93	1	–4.4VDC
E9-3	2	J37-94	1	–4.4VDC
E9-4	1	J38-93	1	–4.4VDC
E9-4	2	J38-94	1	–4.4VDC
E9-5	1	J39-93	1	–4.4VDC
E9-5	2	J39-94	1	–4.4VDC
E9-6	1	J40-93	1	–4.4VDC
E9-6	2	J40-94	1	–4.4VDC
J29-1	1	J44-87	1	FTLB1
J29-2	1	J44-10	1	FTLB2
J29-3	1	J44-9	1	FTLB4
J29-4	1	J44-8	1	FTLB8
J29-5	1	J44-7	1	FTLB16
J29-6	1	J31-12	1	ICH8LPS
J29-7	1	J31-64	1	ICH7LPS
J29-8	1	J31-90	1	ICH6LPS
J29-9	1	J31-67	1	ICH5LPS
J29-10	1	J31-11	1	ICH4LPS
J29-11	1	J31-9	1	ICH3LPS
J29-12	1	J31-14	1	ICH2LPS
J29-13	1	J31-13	1	ICH1LPS
J29-14	1	J31-84	1	SGCLPS
J29-15	1	J31-17	1	SGCLPS
J29-16	1	J31-95	2	GND
J29-17	1	J31-96	2	GND
J29-18	1	J44-11	2	CFNRM–
J29-19	1	J43-89	1	LOOP–
J29-20	1	J31-66	1	EQLPS
J29-21	1	J31-89	1	DMLPS
J29-22	1	J31-86	1	OCH1LPS
J29-23	1	J31-87	1	OCH2LPS
J29-24	1	J31-92	1	OCH3LPS
J29-25	1	J31-88	1	OCH4LPS
J29-26	1	J31-85	1	OCH5LPS
J29-27	1	J31-18	1	OCH6LPS
J29-28	1	J31-16	1	OCH7LPS
J29-29	1	J31-83	1	OCH8LPS
J29-30	1	J31-40	1	AVCALS
J29-31	1	J31-70	1	DVCALS
J29-32	1	J44-71	1	LEAR
J29-33	1	J44-72	1	GND
J29-34	1	J44-18	2	AVRNG–
J29-35	1	J44-20	2	DVRNG–
J29-36	1	J44-89	1	LATL–
J29-37	1	J44-83	2	LDTL–
J29-38	1	J44-93	1	LMIC
J29-39	1	J44-96	2	GND
J29-40	1	J31-36	1	INAT
J29-41	1	J35-23	1	TLFOMF
J29-42	1	J45-22	1	GND
J29-43	1	J31-25	1	AARSSW
J29-44	1	J31-94	1	AALRM–
J29-45	1	J31-80	1	PWRLT
J31-7	1	J32-23	1	GFMTC–
J31-8	1	J32-9	1	PRS–
J31-9	1	J29-11	1	ICH3LPS
J31-11	1	J29-10	1	ICH4LPS
J31-12	1	J29-6	1	ICH8LPS
J31-13	1	J29-13	1	ICH1LPS
J31-14	1	J29-12	1	ICH2LPS
J31-16	1	J29-28	1	OCH7LPS
J31-17	1	J29-15	1	SGSLPS
J31-18	1	J29-27	1	OCH6LPS
J31-20	1	J44-14	1	ALRMT
J31-21	1	J36-26	1	IGS1–
J31-22	1	J38-26	1	IGS3–
J31-23	1	J43-79	1	XMTERR
J31-24	1	J37-26	1	IGS2–
J31-25	1	J29-43	1	AARSSW
J31-26	1	J39-26	1	IGS4–
J31-27	1	J40-70	1	RDEP2
J31-28	1	J38-53	1	IGS7–
J31-29	1	J39-53	1	IGS8–
J31-30	1	J36-53	1	IGS5–
J31-31	1	J37-53	1	IGS6–
J31-33	1	J40-37	1	RDFALT
J31-35	1	J40-14	1	RNOCLK
J31-36	1	J29-40	1	INAT
J31-37	1	J44-51	1	AVCAL–
J31-40	1	J29-30	1	AVCALS
J31-41	1	J32-64	1	GF1
J31-42	1	J32-65	1	GF2
J31-43	1	J32-66	1	GF4
J31-44	1	J32-50	1	GF8–
J31-45	1	J32-38	1	GFMST
J31-46	1	J32-63	1	GF8
J31-47	1	J32-19	1	IDLE
J31-48	1	J31-79	1	ADCT02
J31-49	1	J41-25	1	SYNC8
J31-50	1	J40-28	1	RDEP2–
J31-51	1	J32-8	1	GS
J31-53	1	J32-40	1	DS
J31-55	1	J32-20	1	IDLE–
J31-59	1	J42-86	1	DDCAL–
J31-64	1	J29-7	1	ICH7LPS
J31-66	1	J29-20	1	EQLPS
J31-67	1	J29-9	1	ICH5LPS
J31-70	1	J29-31	1	DVCALS
J31-71	1	J45-79	1	DVCAL–
J31-74	1	J35-37	1	TDFALT
J31-75	1	J31-77	1	ADCT01
J31-77	1	J31-75	1	ADCT01
J31-79	1	J31-48	1	ADCT02
J31-80	1	J29-45	1	PWRLT
J31-82	1	J31-93	1	ADCT03
J31-83	1	J29-29	1	OCH8LPS
J31-84	1	J29-14	1	SGCLPS
J31-85	1	J29-26	1	OCH5LPS
J31-86	1	J29-22	1	OCH1LPS
J31-87	1	J29-23	1	OCH2LPS
J31-88	1	J29-25	1	OCH4LPS
J31-89	1	J29-21	1	DMLPS
J31-90	1	J29-8	1	ICH6LPS
J31-92	1	J29-24	1	OCH3LPS
J31-93	1	J31-82	1	ADCT03
J31-94	1	J29-44	1	AALRM–
J31-95	2	J29-16	1	GND
J31-96	2	I29-17	1	GND

Table 3-32. Card File Backplane Wire Run List—Continued

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J32-7	1	J32-49	1	GTMCT02
J32-8	1	J31-51	1	GS
J32-9	1	J31-8	1	PRS-
J32-9	2	J33-93	2	PRS-
J32-10	1	J32-54	1	GTMCT03
J32-11	1	J39-44	1	ACT8
J32-12	1	J36-28	1	ACT1
J32-13	1	J37-28	1	ACT2
J32-14	1	J38-28	1	ACT3
J32-15	1	J39-28	1	ACT4
J32-16	1	J36-44	1	ACT5
J32-17	1	J38-44	1	ACT7
J32-18	1	J37-44	1	ACT6
J32-19	1	J31-47	1	IDLE
J32-20	1	J31-55	1	IDLE-
J32-21	1	J32-22	1	GTMCT01
J32-22	1	J32-21	1	GTMCT01
J32-23	1	J31-7	1	GFMTC-
J32-24	1	J35-8	1	PULLUP
J32-25	1	J37-73	1	OGRP2T
J32-26	1	J36-73	1	OGRP1T
J32-27	1	J39-73	1	OGRP4T
J32-28	1	J38-73	1	OGRP3T
J32-29	1	J37-76	1	OGRP6T
J32-30	1	J36-76	1	OGRP5T
J32-31	1	J39-76	1	OGRP8T
J32-32	1	J38-76	1	OGRP7T
J32-33	1	J32-52	1	GTMCT04
J32-34	1	J34-88	1	576 KHZ 1
J32-35	1	J37-42	1	APAT2
J32-36	1	J36-42	1	APAT1
J32-37	1	J32-53	1	GTMCT06
J32-38	1	J31-45	1	GFMST
J32-39	1	J32-67	1	GTMCT05
J32-40	1	J31-53	1	DS
J32-41	1	J36-80	1	OGRP1D
J32-42	1	J37-80	1	OGRP2D
J32-43	1	J39-80	1	OGRP4D
J32-44	1	J38-80	1	OGRP3D
J32-45	1	J37-90	1	OGRP6D
J32-46	1	J36-90	1	OGRP5D
J32-47	1	J39-90	1	OGRP8D
J32-48	1	J38-90	1	OGRP7D
J32-49	1	J32-7	1	GTMCT02
J32-50	1	J31-44	1	GF8-
J32-52	1	J32-33	1	GTMCT04
J32-53	1	J32-37	1	GTMCT06
J32-54	1	J32-10	1	GTMCT03
J32-55	1	J37-23	1	IGRP2D
J32-56	1	J36-23	1	IGRP1D
J32-57	1	J39-23	1	IGRP4D
J32-58	1	J38-23	1	IGRP3D
J32-59	1	J36-46	1	IGRP5D
J32-60	1	J37-46	1	IGRP6D
J32-61	1	J38-46	1	IGRP7D
J32-62	1	J39-46	1	IGRP8D
J32-63	1	J31-46	1	GF8
J32-64	1	J31-41	1	GF1
J32-65	1	J31-42	1	GF2
J32-66	1	J31-43	1	GF4
J32-67	1	J32-39	1	GTMCT05
J32-68	1	J38-8	1	RST3
J32-69	1	J39-8	1	RST4
J32-70	1	J36-8	1	RST1
J32-71	1	J37-30	1	RST6
J32-72	1	J38-30	1	RST7
J32-73	1	J36-30	1	RST5
J32-74	1	J37-8	1	RST2
J32-75	1	J39-30	1	RST8
J33-7	1	J33-88	1	D12I
J33-9	1	J33-27	1	DDI-
J33-11	1	J34-89	1	DDCLK
J33-13	1	J43-67	1	75CLK
J33-17	1	J42-43	1	D75EN
J33-25	1	J42-55	1	D12EN
J33-27	1	J33-9	1	DDI-
J33-27	2	J33-90	2	DDI-
J33-29	1	J33-89	1	D75I
J33-31	1	J33-35	1	DECT05
J33-33	1	J33-53	1	DECT04
J33-35	1	J33-31	1	DECT05
J33-39	1	J33-75	1	DDSD-
J33-41	1	J33-63	1	DECT01
J33-47	1	J33-83	1	DECT03
J33-49	1	J33-77	1	DDRY-
J33-53	1	J33-33	1	DECT04
J33-55	1	J33-65	1	DECT02
J33-61	1	J34-55	1	TTYOWI
J33-63	1	J33-41	1	DECT01
J33-65	1	J33-55	1	DECT02
J33-69	1	J33-79	1	DDRG-
J33-73	1	J34-51	1	RTTYOW
J33-75	1	J33-39	1	DDSD-
J33-75	2	J33-82	2	DDSD-
J33-77	1	J33-49	1	DDRY-
J33-77	2	J33-84	2	DDRY-
J33-79	1	J33-69	1	DDRG-
J33-79	2	J33-86	2	DDRG-
J33-82	1	J42-87	1	DDSD-
J33-82	2	J33-75	2	DDSD-
J33-83	1	J33-47	1	DECT03
J33-84	1	J42-94	1	DDRY-
J33-84	2	J33-77	2	DDRY-
J33-85	1	J34-7	1	TDLTTY
J33-86	1	J42-91	1	DDRG-
J33-86	2	J33-79	2	DDRG-
J33-87	1	J34-12	1	TCLK-
J33-88	1	J33-7	1	D12I
J33-89	1	J33-29	1	D75I
J33-90	2	J33-27	2	DDI-
J33-91	1	J34-53	1	TDTAOW
J33-93	1	J34-79	1	PRS-
J33-93	2	J32-9	2	PRS-
J34-7	1	J33-85	1	TDLTTY
J34-7	2	J35-48	1	TDLTTY
J34-8	1	J35-56	1	TSCODE-
J34-10	1	J45-73	1	DVOWI
J34-11	1	J35-29	1	TSREST
J34-12	1	J33-87	1	TCLK-
J34-12	2	J35-7	2	TCLK-
J34-13	1	J35-55	1	TSCODE
J34-14	1	J35-85	1	TFCET

Table 3-32. Card File Backplane Wire Run List—Continued

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J34-15	1	J34-87	1	MOCT03
J34-16	1	J39-22	1	RCOM4
J34-17	1	J38-24	1	RCOM7
J34-18	1	J38-22	1	RCOM3
J34-23	1	J35-52	1	TFCT04
J34-26	1	J35-21	1	TFC11-
J34-25	1	J34-38	1	MOCT02
J34-27	1	J43-85	1	NRZOUT
J34-28	1	J35-54	1	TFCT02
J34-29	1	J39-24	1	RCOM8
J34-30	1	J35-17	1	TFCT01
J34-31	1	J35-50	1	TFCT08
J34-33	1	J36-22	1	RCOM1
J34-34	1	J35-74	1	TDVOW
J34-35	1	J37-22	1	RCOM2
J34-38	1	J34-25	1	MOCT02
J34-39	1	J35-22	1	96 CHE
J34-41	1	J36-24	1	RCOM5
J34-43	1	J37-24	1	RCOM6
J34-45	1	J35-9	1	TCLK
J34-50	1	J35-26	1	TDEP4
J34-51	1	J33-73	1	RTTYOW
J34-53	1	J33-91	1	TDTAOW
J34-53	2	J35-24	1	TDTAOW
J34-55	1	J33-61	1	TTYOWI
J34-57	1	J34-91	1	MOCT01
J34-61	1	J35-68	1	TDAP24-
J34-65	1	J44-47	1	1.6 KHZ
J34-67	1	J44-23	1	6.4 KHZ
J34-69	1	J39-9	1	GRP 4
J34-70	1	J38-9	1	GRP 3
J34-71	1	J37-21	1	GRP 6
J34-72	1	J36-21	1	GRP 5
J34-73	1	J38-21	1	GRP 7
J34-75	1	J39-21	1	GRP 8
J34-78	1	J36-9	1	GRP 1
J34-79	1	J33-93	1	PRS-
J34-79	2	J42-15	2	PRS-
J34-80	1	J37-9	1	GRP 2
J34-81	1	J35-63	1	TBCT02
J34-83	1	J35-62	1	TGRPE-
J34-84	1	J35-65	1	TBCT01
J34-86	1	J35-61	1	TBCT04
J34-87	1	J34-15	1	MOCT03
J34-88	1	J32-34	1	576 KHZ 1
J34-89	1	J33-11	1	DDCLK
J34-90	1	J35-13	1	TMASCLK
J34-91	1	J34-57	1	MOCT01
J34-92	1	J35-59	1	48 CHE
J34-93	1	J36-7	1	CHAN
J34-94	1	J36-39	1	576 KHZ 2
J35-7	2	J34-12	2	TCLK-
J35-8	1	J32-24	1	PULLUP
J35-8	2	J35-20	2	PULLUP
J35-9	2	J36-11	2	TCLK
J35-9	1	J34-45	1	TCLK
J35-11	1	J35-27	1	TTCCT01
J35-12	1	J35-19	1	TNOCLK-
J35-13	1	J34-90	1	TMASCLK
J35-13	2	J43-77	1	TMASCLK
J35-16	1	J35-25	1	TTCCT02
J35-17	1	J34-30	1	TFCT01
J35-19	1	J35-12	1	TNOCLK
J35-20	1	J35-28	1	PULLUP
J35-20	2	J35-8	2	PULLUP
J35-21	1	J34-26	1	TFC11-
J35-22	1	J34-39	1	96 CHE
J35-22	2	J40-22	2	96 CHE
J35-23	1	J29-41	1	TLFOMF
J35-24	1	J34-53	2	TDTAOW
J35-25	1	J35-16	1	TTCCT02
J35-26	1	J34-50	1	TDEP4
J35-27	1	J35-11	1	TTCCT01
J35-28	1	J35-20	1	PULLUP
J35-28	2	J35-57	1	PULLUP
J35-29	1	J34-11	1	TSREST
J35-30	1	J38-20	1	TCHAN7
J35-33	1	J39-20	1	TCHAN8
J35-35	1	J37-20	1	TCHAN6
J35-37	1	J31-74	1	TDFALT
J35-39	1	J36-10	1	TCHN1
J35-40	1	J37-10	1	TCHN2
J35-41	1	J39-10	1	TCHN4
J35-42	1	J38-10	1	TCHN3
J35-43	1	J37-12	1	TCHN6
J35-44	1	J36-12	1	TCHN5
J35-45	1	J39-12	1	TCHN8
J35-46	1	J38-12	1	TCHN7
J35-48	1	J34-7	2	TDLTTY
J35-50	1	J34-31	1	TFCT08
J35-52	1	J34-23	1	TFCT04
J35-54	1	J34-28	1	TFCT02
J35-55	1	J34-13	1	TSCODE
J35-56	1	J34-8	1	TSCODE-
J35-57	1	J35-28	2	PULLUP
J35-59	2	J36-18	2	48 CHE
J35-59	1	J34-92	1	48 CHE
J35-61	1	J34-86	1	TBCT04
J35-62	1	J34-83	1	TGRPE-
J35-63	1	J34-81	1	TBCT02
J35-65	1	J34-84	1	TBCT01
J35-68	1	J34-61	1	TDAP24-
J35-70	1	J35-96	2	TCGND
J35-72	1	J45-92	1	TDVOWC-
J35-74	1	J34-34	1	TDVOW
J35-74	2	J45-93	1	TDVOW
J35-76	1	J37-19	1	TCHAN2
J35-78	1	J38-19	1	TCHAN3
J35-80	1	J39-19	1	TCHAN4
J35-82	1	J36-20	1	TCHAN5
J35-85	1	J34-14	1	TFCET
J35-86	1	J36-19	1	TCHAN1
J35-93	1	E9-1	1	-4.4VDC
J35-94	1	E9-1	2	-4.4VDC
J35-96	2	J35-70	1	TCGND
J36-7	1	J34-93	1	CHAN
J36-7	2	J36-27	2	CHAN
J36-8	1	J32-70	1	RST1
J36-9	1	J34-78	1	GRP 1
J36-10	1	J35-39	1	TCHN1
J36-11	1	J37-11	1	TCLK
J36-11	2	J35-9	2	TCLK

Table 3-38. Card File Backplane Wire Run List—Continued

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J36-12	1	J35-44	1	TCHN5
J36-13	1	J40-86	1	TCHAN1
J36-14	1	J37-14	1	RCLK−
J36-15	1	J40-82	1	RCHAN5
J36-16	1	J40-44	1	RCHN5
J36-17	1	J40-39	1	RCHN1
J36-18	1	J37-18	1	48 CHE
J36-18	2	J35-59	2	48 CHE
J36-19	1	J35-86	1	TCHAN1
J36-20	1	J35-82	1	TCHAN5
J36-21	1	J34-72	1	GRP 5
J36-22	1	J34-33	1	RCOM1
J36-23	1	J32-56	1	IGRP1D
J36-24	1	J34-41	1	RCOM5
J36-26	1	J31-21	1	IGS1−
J36-27	1	J37-27	1	CHAN
J36-27	2	J36-7	2	CHAN
J36-28	1	J32-12	1	ACT1
J36-30	1	J32-73	1	RST5
J36-33	1	J36-43	1	SDATA
J36-35	1	J37-35	1	RMSYNC−
J36-39	1	J34-94	1	576 KHZ 2
J36-39	2	J37-39	2	576 KHZ 2
J36-42	1	J32-36	1	APAT1
J36-42	2	J38-42	1	APAT1
J36-43	1	J36-33	1	SDATA
J36-43	2	J37-43	2	SDATA
J36-44	1	J32-16	1	ACT5
J36-46	1	J32-59	1	IGRP5D
J36-49	1	J36-51	1	DGPCT05
J36-50	1	J36-52	1	DGPCT01
J36-51	1	J36-49	1	DGPCT05
J36-52	1	J36-50	1	DGPCT01
J36-53	1	J31-30	1	IGS5−
J36-61	1	J36-95	2	GND1
J36-73	1	J32-26	1	OGRP1T
J36-76	1	J32-30	1	OGRP5T
J36-80	1	J32-41	1	OGRP1D
J36-90	1	J32-46	1	OGRP5D
J36-93	1	E9-2	1	−4.4VDC
J36-94	1	E9-2	2	−4.4VDC
J36-95	2	J36-61	1	GND1
J37-7	1	J38-7	1	CHAN
J37-7	2	J37-27	2	CHAN
J37-8	1	J32-74	1	RST2
J37-9	1	J34-80	1	GRP 2
J37-10	1	J35-40	1	TCHN2
J37-11	1	J36-11	1	TCLK
J37-11	2	J38-11	2	TCLK
J37-12	1	J35-43	1	TCHN6
J37-13	1	J40-76	1	RCHAN2
J37-14	1	J36-14	1	RCLK−
J37-14	2	J38-14	2	RCLK−
J37-15	1	J40-35	1	RCHAN6
J37-16	1	J40-43	1	RCHN6
J37-17	1	J40-40	1	RCHN2
J37-18	2	J38-18	2	48 CHE
J37-18	1	J36-18	1	48 CHE
J37-19	1	J35-76	1	TCHAN2
J37-20	1	J35-35	1	TCHAN6

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J37-21	1	J34-71	1	GRP 6
J37-22	1	J34-35	1	RCOM2
J37-23	1	J32-55	1	IGRP2D
J37-24	1	J34-43	1	RCOM6
J37-26	1	J31-24	1	IGS2−
J37-27	1	J36-27	1	CHAN
J37-27	2	J37-7	2	CHAN
J37-28	1	J32-13	1	ACT2
J37-30	1	J32-71	1	RST6
J37-33	1	J37-43	1	SDATA
J37-33	2	J38-33	2	SDATA
J37-35	1	J36-35	1	RMSYNC−
J37-35	2	J38-35	2	RMSYNC−
J37-39	1	J38-39	1	576 KHZ 2
J37-39	2	J36-39	2	576 KHZ 2
J37-42	1	J32-35	1	APAT2
J37-42	2	J39-42	2	APAT2
J37-43	1	J37-33	1	SDATA
J37-43	2	J36-43	2	SDATA
J37-44	1	J32-13	1	ACT6
J37-46	1	J32-60	1	IGRP6D
J37-49	1	J37-51	1	DGPCT06
J37-50	1	J37-52	1	DGPCT02
J37-51	1	J37-49	1	DGPCT06
J37-52	1	J37-50	1	DGPCT02
J37-53	1	J31-31	1	IGS6−
J37-61	1	J37-95	2	GND2
J37-73	1	J32-25	1	OGRP2T
J37-76	1	J32-29	1	OGRP6T
J37-80	1	J32-42	1	OGRP2D
J37-90	1	J32-45	1	OGRP6D
J37-93	1	E9-3	1	−4.4VDC
J37-94	1	E9-3	2	−4.4VDC
J37-95	2	J37-61	1	GND2
J38-7	1	J37-7	1	CHAN
J38-7	2	J38-27	2	CHAN
J38-8	1	J32-68	1	RST3
J38-9	1	J34-70	1	GRP 3
J38-10	1	J35-42	1	TCHN3
J38-11	1	J39-11	1	TCLK
J38-11	2	J37-11	2	TCLK
J38-12	1	J35-46	1	TCHN7
J38-14	1	J39-14	1	RCLK−
J38-14	2	J37-14	2	RCLK−
J38-13	1	J40-78	1	RCHAN3
J38-15	1	J40-30	1	RCHAN7
J38-16	1	J40-46	1	RCHN7
J38-17	1	J40-42	1	RCHN3
J38-18	2	J37-18	2	48 CHE
J38-18	1	J39-18	1	48 CHE
J38-19	1	J35-78	1	TCHAN3
J38-20	1	J35-30	1	TCHAN7
J38-21	1	J34-73	1	GRP 7
J38-22	1	J34-18	1	RCOM3
J38-23	1	J32-58	1	IGRP3D
J38-24	1	J34-17	1	RCOM7
J38-26	1	J31-22	1	IGS3−
J38-27	1	J39-27	1	CHAN
J38-27	2	J38-7	2	CHAN

Table 3-32. Card File Backplane Wire Run List—Continued

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J38-28	1	J32-14	1	ACT3
J38-30	1	J32-72	1	RST7
J38-33	1	J38-43	1	SDATA
J38-33	2	J37-33	2	SDATA
J38-35	1	J39-35	1	RMSYNC-
J38-35	2	J37-35	2	RMSYNC-
J38-39	1	J37-39	1	576 KHZ 2
J38-39	2	J39-39	1	576 KHZ 2
J38-42	1	J36-42	2	APAT1
J38-43	1	J38-33	1	SDATA
J38-43	2	J39-43	2	SDATA
J38-44	1	J32-17	1	ACT7
J38-46	1	J32-61	1	IGRP7D
J38-49	1	J38-51	1	DGPCT07
J38-50	1	J38-52	1	DGPCT03
J38-51	1	J38-49	1	DGPCT07
J38-52	1	J38-50	1	DGPCT03
J38-53	1	J31-28	1	IGS7-
J38-61	1	J38-95	2	GND3
J38-73	1	J32-28	1	OGRP3T
J38-76	1	J32-32	1	OGRP7T
J38-80	1	J32-44	1	OGRP3D
J38-90	1	J32-48	1	OGRP7D
J38-93	1	E9-4	1	−4.4VDC
J38-94	1	E9-4	2	−4.4VDC
J38-95	2	J38-61	1	GND3
J39-7	2	J39-27	2	CHAN
J39-8	1	J32-69	1	RST4
J39-9	1	J34-69	1	GRP 4
J39-10	1	J35-41	1	TCHN4
J39-11	1	J38-11	1	TCLK
J39-11	2	J45-94	1	TCLK
J39-12	1	J35-45	1	TCHN8
J39-13	1	J40-80	1	RCHAN4
J39-14	1	J38-14	1	RCLK-
J39-14	2	J40-7	2	RCLK-
J39-15	1	J40-33	1	RCHAN8
J39-16	1	J40-45	1	RCHN8
J39-17	1	J40-41	1	RCHN4
J39-18	1	J38-18	1	48 CHE
J39-18	2	J40-59	2	48 CHE
J39-19	1	J35-80	1	TCHAN4
J39-20	1	J35-33	1	TCHAN8
J39-21	1	J34-75	1	GRP 8
J39-22	1	J34-16	1	RCOM4
J39-23	1	J32-57	1	IGRP4D
J39-24	1	J34-29	1	RCOM8
J39-26	1	J31-26	1	IGS4-
J39-27	1	J38-27	1	CHAN
J39-27	2	J39-7	2	CHAN
J39-28	1	J32-15	1	ACT4
J39-30	1	J32-75	1	RST8
J39-33	1	J39-43	1	SDATA
J39-33	2	J41-51	2	SDATA
J39-35	1	J38-35	1	RMSYNC-
J39-35	2	J40-8	2	RMSYNC-
J39-39	1	J38-39	2	576 KHZ 2
J39-42	2	J37-42	2	APAT2
J39-43	1	J39-33	1	SDATA
J39-43	2	J38-43	2	SDATA
J39-44	1	J32-11	1	ACT8
J39-46	1	J32-62	1	IGRP8D
J39-49	1	J39-51	1	DGPCT08
J39-50	1	J39-52	1	DGPCT04
J39-51	1	J39-49	1	DGPCT08
J39-52	1	J39-50	1	DGPCT04
J39-53	1	J31-29	1	IGS8-
J39-61	1	J39-95	2	GND4
J39-73	1	J32-27	1	OGRP4T
J39-76	1	J32-31	1	OGRP8T
J39-80	1	J32-43	1	OGRP4D
J39-90	1	J32-47	1	OGRP8D
J39-93	1	E9-5	1	−4.4VDC
J39-94	1	E9-5	2	−4.4VDC
J39-95	2	J39-61	1	GND4
J40-7	1	J41-9	1	RCLK-
J40-7	2	J39-14	2	RCLK-
J40-8	1	J41-29	1	RMSYNC-
J40-8	2	J39-35	2	RMSYNC-
J40-9	1	J41-33	1	RCLK
J40-11	1	J40-27	1	RTCCT01
J40-12	1	J40-19	1	RNOCLK-
J40-13	1	J42-8	1	RMASCLK
J40-14	1	J31-35	1	RNOCLK
J40-14	2	J45-81	1	RNOCLK
J40-15	1	J41-63	1	RLBMF-
J40-16	1	J40-25	1	RTCCT02
J40-18	1	J41-83	1	R341BT
J40-19	2	J41-93	1	RNOCLK-
J40-19	1	J40-12	1	RNOCLK-
J40-20	1	J43-63	1	RPHF
J40-22	2	J35-22	2	96 CHE
J40-22	1	J45-63	1	96 CHE
J40-24	1	J42-27	1	RDTAOW
J40-25	1	J40-16	1	RTCCT02
J40-26	1	J41-7	1	RDEP4
J40-27	1	J40-11	1	RTCCT01
J40-28	1	J31-50	1	RDEP2-
J40-30	1	J38-15	1	RCHAN7
J40-32	1	J41-37	1	RSREST-
J40-33	1	J39-15	1	RCHAN8
J40-35	1	J37-15	1	RCHAN6
J40-37	1	J31-33	1	RDFALT
J40-39	1	J36-17	1	RCHN1
J40-40	1	J37-17	1	RCHN2
J40-41	1	J39-17	1	RCHN4
J40-42	1	J38-17	1	RCHN3
J40-43	1	J37-16	1	RCHN6
J40-44	1	J36-16	1	RCHN5
J40-45	1	J39-16	1	RCHN8
J40-46	1	J38-16	1	RCHN7
J40-48	1	J41-61	1	RDLTTY
J40-55	1	J41-57	1	RSCODE
J40-56	1	J41-59	1	RSCODE-
J40-57	1	J41-87	1	RFSYNC-
J40-58	1	J41-91	1	R341BT-
J40-59	1	J45-67	1	48 CHE
J40-59	2	J39-18	2	48 CHE

Table 3-32. Card File Backplane Wire Run List—Continued

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J40-68	1	J41-43	1	RDAP24–
J40-70	1	J31-27	1	RDEP2
J40-72	1	J45-91	1	RDVOWC–
J40-74	1	J45-86	1	RDVOW
J40-76	1	J37-13	1	RCHAN2
J40-78	1	J38-13	1	RCHAN3
J40-80	1	J39-13	1	RCHAN4
J40-82	1	J36-15	1	RCHAN5
J40-85	1	J41-39	1	RFCET
J40-86	1	J36-13	1	RCHAN1
J40-93	1	E9-6	1	–4.4VDC
J40-94	1	E9-6	2	–4.4VDC
J41-7	1	J40-26	1	RDEP4
J41-9	1	J40-7	1	RCLK–
J41-9	2	J42-47	2	RCLK–
J41-15	1	J43-61	1	RDATA
J41-25	1	J31-49	1	SYNC8
J41-27	1	J41-77	1	FSCT02
J41-29	1	J40-8	1	RMSYNC–
J41-31	1	J41-55	1	FSCT03
J41-33	2	J45-75	1	RCLK
J41-33	1	J40-9	1	RCLK
J41-37	1	J40-32	1	RSREST–
J41-39	1	J40-85	1	RFCET
J41-41	1	J41-89	1	FSCT01
J41-43	1	J40-68	1	RDAP24–
J41-51	2	J39-33	2	SDATA
J41-51	1	J42-85	1	SDATA
J41-55	1	J41-31	1	FSCT03
J41-57	1	J40-55	1	RSCODE
J41-59	1	J40-56	1	RSCODE–
J41-61	1	J40-48	1	RDLTTY
J41-61	2	J42-29	1	RDLTTY
J41-63	2	J42-23	1	RLBMF–
J41-63	1	J40-15	1	RLBMF–
J41-65	1	J42-49	1	SYNC8–
J41-77	1	J41-27	1	FSCT02
J41-79	1	J43-59	1	RMSYNC
J41-83	1	J40-18	1	R341BT
J41-87	1	J40-57	1	RFSYNC–
J41-89	1	J41-41	1	FSCT01
J41-91	1	J40-58	1	R341BT–
J41-93	1	J40-19	2	RNOCLK–
J42-8	1	J40-13	1	RMASCLK
J42-8	2	J43-75	2	RMASCLK
J42-9	1	J42-68	1	DDRV–
J42-10	1	J42-31	1	DDCT04
J42-11	1	J42-61	1	DDCT05
J42-15	1	J44-53	1	PRS–
J42-15	2	J34-79	2	PRS–
J42-21	1	J42-83	1	DDCT03
J42-23	1	J41-63	2	RLBMF–
J42-27	1	J40-24	1	RDTAOW
J42-29	1	J41-61	2	RDLTTY
J42-31	1	J42-10	1	DDCT04
J42-33	1	J42-89	1	DDCT02
J42-35	1	J42-92	1	DDCT01
J42-37	1	J42-66	1	D75O
J42-43	1	J33-17	1	D75EN
J42-47	1	J45-85	1	RCLK–
J42-47	2	J41-9	2	RCLK–
J42-49	1	J41-65	1	SYNC8–
J42-49	2	J45-88	1	SYNC8–
J42-55	1	J33-25	1	D12EN
J42-61	1	J42-11	1	DDCT05
J42-66	1	J42-37	1	D75O
J42-68	1	J42-9	1	DDRV–
J42-68	2	J42-90	1	DDRV–
J42-83	1	J42-21	1	DDCT03
J42-85	1	J41-51	1	SDATA
J42-85	2	J45-89	1	SDATA
J42-86	1	J31-59	1	DDCAL–
J42-86	2	J42-93	1	DDCAL–
J42-87	1	J33-82	1	DDSD–
J42-89	1	J42-33	1	DDCT02
J42-90	1	J42-68	2	DDRV–
J42-91	1	J33-86	1	DDRG–
J42-92	1	J42-35	1	DDCT01
J42-93	1	J42-86	2	DDCAL–
J42-94	1	J33-84	1	DDRY–
J43-26	1	J43-39	1	SGIN2
J43-32	1	J43-33	1	SGOUT2
J43-33	1	J43-32	1	SGOUT2
J43-39	1	J43-26	1	SGIN2
J43-47	1	J44-15	1	CABFLT
J43-52	1	J43-96	2	GND
J43-55	1	J43-83	1	DRCT02
J43-57	1	J43-87	1	DRCT01
J43-59	1	J41-79	1	RMSYNC
J43-61	1	J41-15	1	RDATA
J43-63	1	J40-20	1	RPHF
J43-67	1	J33-13	1	75CLK
J43-71	1	J44-11	1	CFNRM–
J43-75	1	J42-8	2	RMASCLK
J43-77	1	J35-13	2	TMASCLK
J43-79	1	J31-23	1	XMTERR
J43-81	1	J40-14	2	RNOCLK
J43-83	1	J43-55	1	DRCT02
J43-85	1	J34-27	1	NRZOUT
J43-87	1	J43-57	1	DRCT01
J43-89	1	J29-19	1	LOOP–
J43-96	2	J43-52	1	GND
J44-7	1	J29-5	1	FTLB16
J44-8	1	J29-4	1	FTLB8
J44-9	1	J29-3	1	FTLB4
J44-10	1	J29-2	1	FTLB2
J44-11	1	J43-71	1	CFNRM–
J44-11	2	J29-18	1	CFNRM–
J44-14	1	J31-20	1	ALRMT
J44-15	1	J43-47	1	CABFLT
J44-18	1	J44-78	1	AVRNG–
J44-18	2	J29-34	1	AVRNG–
J44-20	1	J44-79	1	DVRNG–
J44-20	2	J29-35	1	DVRNG–
J44-21	1	J44-44	1	AVCT01
J44-23	1	J34-67	1	6.4 KHZ
J44-27	1	J45-39	1	DVRNGS
J44-33	1	J44-80	1	RMIC
J44-43	1	J44-81	1	REAR
J44-44	1	J44-21	1	AVCT01
J44-47	1	J34-65	1	1.6 KHZ

Table 3-32. Card File Backplane Wire Run List—Continued

From		To		Signal name
Conn/pin	Level	Conn/pin	Level	
J44-50	1	J44-76	1	REF
J44-51	1	J31-37	1	AVCAL-
J44-53	1	J42-15	1	PRS-
J44-65	1	J45-19	1	DVEAR
J44-67	1	J45-21	1	DVMIC
J44-71	1	J29-32	1	LEAR
J44-72	1	J29-33	1	GND
J44-76	1	J44-50	1	REF
J44-78	1	J44-18	1	AVRNG-
J44-79	1	J44-20	1	DVRNG-
J44-80	1	J44-33	1	RMIC
J44-81	1	J44-43	1	REAR
J44-83	2	J29-37	1	LDTL-
J44-83	1	J45-59	1	LDTL-
J44-86	1	J45-76	1	RDTL-
J44-87	1	J29-1	1	FTLB1
J44-89	1	J29-36	1	LATL-
J44-93	1	J29-38	1	LMIC
J44-96	2	J29-39	1	GND
J45-19	1	J44-65	1	DVEAR
J45-21	1	J44-67	1	DVMIC
J45-22	1	J29-42	1	GND
J45-29	1	J45-87	1	DVCT01
J45-31	1	J45-53	1	DVEXO-
J45-32	1	J45-55	1	DVEXO
J45-39	1	J44-27	1	DVRNGS
J45-45	1	J45-77	1	DVCT02
J45-53	1	J45-31	1	DVEXO-
J45-55	1	J45-32	1	DVEXO
J45-59	1	J44-83	1	LDTL-
J45-63	1	J40-22	1	96 CHE
J45-67	1	J40-59	1	48 CHE
J45-73	1	J34-10	1	DVOWI
J45-75	1	J41-33	2	RCLK
J45-76	1	J44-86	1	RDTL-
J45-77	1	J45-45	1	DVCT02
J45-79	1	J31-71	1	DVCAL-
J45-85	1	J42-47	1	RCLK-
J45-86	1	J40-74	1	RDVOW
J45-87	1	J45-29	1	DVCT01
J45-88	1	J42-49	2	SYNC8-
J45-89	1	J42-85	2	SDATA
J45-91	1	J40-72	1	RDVOWC-
J45-92	1	J35-72	1	TDVOWC-
J45-93	1	J35-74	2	TDVOW
J45-94	1	J39-11	2	TCLK

Table 3-33. Cable Marker Sleeve Marking Information

Connector terminal	Marker sleeve part number	Marker information
E3	SM-D-941761-020	Mates with A13E3
E4	SM-D-941761-021	Mates with A13E4
E5	SM-D-941761-022	Mates with A13E5
E6	SM-D-941761-023	Mates with A13E6
E7	SM-D-941761-024	Mates with A13E7
E8	SM-D-941761-025	Mates with A13E8
E9	SM-D-941761-026	Mates with A13E9
P1	SM-D-941761-001	Mates with A13J31, Pins 73-92
P2	SM-D-941761-002	Mates with A13J31, Pins 59-68
P3	SM-D-941761-003	Mates with A13J31, Pins 5-24
P4	SM-D-941761-004	Mates with A13J32, Pins 79-98
P5 (not used)		
P6	SM-D-941761-006	Mates with A13J33, Pins 81-90
P7	SM-D-941761-007	Mates with A13J36, Pins 81-90
P8	SM-D-941761-008	Mates with A13J37, Pins 81-90
P9	SM-D-941761-009	Mates with A13J38, Pins 81-90
P10	SM-D-941761-010	Mates with A13J39, Pins 81-90
P11	SM-D-941761-011	Mates with A13J42, Pins 65-74
P12	SM-D-941761-012	Mates with A13J43, Pins 47-56
P13	SM-D-941761-013	Mates with A13J43, Pins 35-44
P14	SM-D-941761-014	Mates with A13J43, Pins 23-32
P15	SM-D-941761-015	Mates with A13J44, Pins 77-96
P16	SM-D-941761-016	Mates with A13J44, Pins 67-76
P17	SM-D-941761-017	Mates with A13J44, Pins 55-64
P18	SM-D-941761-018	Mates with A13J44, Pins 23-32
P19	SM-D-941761-019	Mates with A13J45, Pins 23-32
TB1-1	SM-D-941761-027	Mates with A13TB1-1
TB1-2	SM-D-941761-028	Mates with A13TB1-2
TB1-3	SM-D-941761-029	Mates with A13TB1-3
TB1-4	SM-D-941761-030	Mates with A13TB1-6
TB1-5	SM-D-941761-031	Mates with A13TB1-7
TB1-6	SM-D-941761-032	Mates with A13TB1-8
TB1-7	SM-D-941761-033	Mates with A13J29
TB1-8	SM-D-941761-034	Mates with A13J30

CHAPTER 4

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL

WARNING

HIGH VOLTAGE (up to 400 volts ac and dc) is present in the power supply. DEATH ON CONTACT or serious injury may result if personnel fail to observe safety precautions when performing maintenance on an energized power supply with cover removed.

4-1. Introduction

This chapter contains the visual inspection, test, troubleshooting, and maintenance procedures authorized for use by maintenance personnel at the general support maintenance level. Complete repair of the power supply in the TD-976/G is authorized at this level of maintenance.

4-2. Maintenance Concept

a. General. The power supply is a solid state device that produces regulated +5, +12, −12, and −4.4-volt outputs from an external 115-volt, 60 Hz source. The power supply also produces a regulated 45-milliampere cable current output. Personnel performing troubleshooting and maintenance on the power supply circuits should be familiar with general maintenance and troubleshooting techniques involving high-voltage circuits. Personnel should also have an understanding of the theory of operation of the power supply.

b. Maintenance Application. When a power supply is received at the general support level, it will be given a visual inspection as directed in section III. The visual inspection determines if the unit should be repaired before it is tested as instructed in section III. The electrical tests in section III are performed initially as a receiving test to detect a specific fault symptom. The fault symptom determines which one of the two troubleshooting tables in section IV is to be used to isolate the faulty components. The two troubleshooting tables are step-by-step procedures that are performed until the faulty components are identified. The power supply breakout box is used in the test and troubleshooting procedures to provide the 115-volt ac source power for the power supply and to provide electrical loads for the power supply outputs. After the faulty components in a power supply are identified, the appropriate repair procedures in section V will be performed to correct the faulty condition. When the repair function is completed, the electrical tests in section III are performed as the final performance test to ensure that the power supply is repaired and ready to be returned to stock or to a user.

c. Jumpers P1 through P7. The circuit card in the power supply contains removable jumpers P1 through P7. These jumpers are removed in the course of troubleshooting the power supply as directed in the troubleshooting tables. By systematically removing the jumpers as directed in the troubleshooting procedures, the faulty functional circuit(s) in the power supply can be isolated. This isolation capability allows the fault symptom to be isolated to the stage level.

Section II. TOOLS AND TEST EQUIPMENT

4-3. Introduction

This section contains a list of the tools and test equipment authorized for use in the performance of a general support maintenance on the TD-976/G. The use of these tools and test equipment is authorized in the maintenance allocation chart in TM 11-7025-202-12.

4-4. Tools and Test Equipment

The tools and test equipment required for maintenance of the power supply are listed in table 4-1. The following information is provided in the tables.

a. Tools and Test Equipment Column. This column lists the official name or functional name of the tool or test equipment.

b. Military Designation/Manufacturer's Part No. Column. This column lists the manufacturer's part number (followed by the manufacturer's name in parentheses) when the military designation is not assigned or available.

c. NSN or FSCM Column. This column lists the National stock number or the Federal supply code for the manufacturer when the National stock number is not assigned or available. This information is defined and listed in the RPSTL (TM 11-7025-202-34P).

d. Use Column. This column lists a brief application description and paragraph references where the item is used in the procedures.

Table 4-1. General Support Tools and Test Equipment List

Tools and test equipment	Military designation/ manufacturer's part No.	NSN or FSCM	Use
Bench top repair center.	PRC-150A (Pace).	3439-00-445-5965	Circuit card repair (para 4-19).
Locking insert tools consisting of:	----	----	Locking insert replacement (para 4-18).
Extraction tool.	1227-02 (Heli-Coil)	5120-00-138-6803	For 2-56 inserts.
Extraction tool.	1227-06 (Heli-Coil)	5120-00-245-9539	For 4-40 and 8-32 inserts.
Extraction tool.	1227-6 (Heli-Coil)	5120-00-723-6833	For 10-32 inserts.
Insertion tool.	551-02 (Heli-Coil)	----	For 2-56 inserts.
Insertion tool.	7551-04 (Heli-Coil)	5120-00-816-5703	For 4-40 inserts.
Insertion tool.	7551-2 (Heli-Coil)	5120-00-237-4669	For 8-32 inserts.
Insertion tool.	7552-3 (Heli-Coil)	5120-00-797-2404	For 10-32 inserts.
Tang breakoff tool.	3695-02 (Heli-Coil)	5120-00-410-9156	For 2-56 inserts.
Tang breakoff tool.	3695-04 (Heli-Coil)	5120-00-793-1073	For 4-40 inserts.
Tang breakoff tool.	3695-2 (Heli-Coil)	5120-00-776-9519	For 8-32 inserts.
Tang breakoff tool.	3695-3 (Heli-Coil)	5120-00-793-1076	For 10-32 inserts.
Connector repair tool kit.	70730090-009 (Martin Marietta).	04939 (FSCM)	Connector repair (para 4-19).
Digital multimeter (DMM).	3490A (Hewlett-Packard).	6625-01-010-9255	Testing and troubleshooting (para 4-9, 4-13).
Electronic equipment tool kit.	TK-105/G.	5180-00-610-8177	Disassembly and assembly (para 4-20).
Oscilloscope.	OS-261/U.	6625-00-127-0079	Testing and troubleshooting (para 4-9, 4-13).
Power supply.	DCR-80-10 (Raytheon).	55938 (FSCM)	Troubleshooting (para 4-13).
Power supply breakout box.	70730040-009 (Martin Marietta).	04939 (FSCM)	Testing and troubleshooting (para 4-9, 4-13).

Section III. POWER SUPPLY INSPECTION AND TEST PROCEDURES

4-5. Introduction

This section contains the inspection and test procedures performed on each power supply returned from the user. The test procedures are repeated on each repaired power supply as the performance standards to ensure that the unit is ready to be returned to stock or the user.

4-6. Visual Inspection Procedures

The visual inspection procedures in table 4-2 will be performed on each power supply before the test procedures in paragraph 4-9 are used. The location of components in the power supply are shown in figures 4-1 and 4-2. All defects discovered during the visual inspection will be corrected before energizing the power supply and performing the dynamic test procedures. Power supply repair procedures are in section V.

4-7. Tools and Test Equipment Required for Power Supply Tests

Table 4-3 lists the test equipment required for performing the power supply electrical tests. There are no special tools required in the performance of the tests.

Table 4-2. Power Supply Inspection Procedures

Step	Procedure	Inspection
1	Remove cover from heat sink assembly by removing four sets of screws and washers securing cover to assembly.	*a.* Missing or damaged cover. *b.* Missing screws or washers.
2	Inspect wiring.	*a.* Pinched or frayed wires. *b.* Loose or damaged wire terminations.
3	Inspect heat sink mounted components.	*a.* Heat damaged components. *b.* Physically damaged components. *c.* Loose components. *d.* Heat sink (housing) physical damage.
4	Inspect capacitor C1 (large capacitor).	*a.* Damaged or loose + and − terminals. *b.* Damaged or loose loop clamps.

Table 4-2. Power Supply Inspection Procedures—Continued

Step	Procedure	Inspection
5	Inspect circuit card components.	*a.* Heat damaged components. *b.* Physically damaged components. *c.* Presence of foreign material. *d.* Damaged printed circuit card.
6	Check circuit card jumpers P1 through P7. P1 in J1 and J2 P2 in J6 and J7 P3 in J8 and J9 P4 in J12 and J13 P5 in J15 and J16 P6 in J18 and J19 P7 in J21 and J22	*a.* Properly installed. *b.* Missing or damaged.

Table 4-2. Power Supply Inspection Procedures—Continued

Step	Procedure	Inspection
7	Inspect connector P1.	*a.* Presence of foreign material between pins. *b.* Missing, damaged, bent, pushed, or out-of-alignment pins. *c.* Damaged connector housing. *d.* Damaged or missing guide pins on each side of connector P1.
8	Install cover on heat sink assembly, using four sets of screws and washers removed in step 1.	

Table 4-3. Test Equipment Required for Power Supply Tests

Test equipment	Qty	NSN or part No.
Digital multimeter 3490A.	1	6625-01-010-9255
Oscilloscope OS-261/U.	1	6625-00-127-0079
Power supply breakout box.	1	70730040-009 (Martin Marietta)

4-8. Test Functional Description

The power supply test procedures in table 4-4 are divided into five functional circuit tests. Each circuit test has one or more normal indications listed opposite the appropriate step in the table. The normal indications are used to determine if the circuit being tested is operational or faulty. It is possible that one of the three adjustments in the power supply may be out of adjustment and cause a faulty indication in the test. The adjustments of these three controls are incorporated into the test procedures below.

a. DC Output Voltage Tests. These tests are dynamic checks of the regulation circuits, output voltage levels, and ripple voltage content of the +5-, +12-, −12-, and −4.4-volt outputs of the power supply. The +5-volt regulation circuit contains one adjustment (R34), which is performed as part of the test procedures when the +5-volt output is out of tolerance.

b. +5-Volt Crowbar Test. This test is a dynamic check of the +5-volt crowbar circuit. The test forces the +5-volt output into an out-of-tolerance condition that causes the +5-volt crowbar circuit to activate and shut down the power supply outputs.

c. DC Monitor Test. This test is a dynamic check of the dc monitor circuit. Functional operation of the dc monitor circuit is checked with the normal dc output voltages applied; then, it is checked by removing each dc output voltage, one at a time.

d. 45 MA Cable Current Regulation Test. This test is a dynamic check of the regulation circuits ability to regulate the 45-milliampere current under different load conditions. The ripple voltage content on the cable current output is also checked in this test. The cable current regulation circuit contains one adjustment (R72), which is performed as part of the test procedures when the regulated cable current is out of tolerance.

e. 45 MA Cable Current Crowbar Circuit Test. This test is a dynamic check of the cable current crowbar circuit. The test forces the cable current output into an out-of-tolerance condition that causes the cable current crowbar circuit to activate and shut down the cable current output. The cable current crowbar circuit contains one adjustment (R67), which is performed as part of the test procedures when the circuit does not activate in the test procedures. In a functional power supply, activation of the cable current crowbar circuit does not shut down or affect the four low-voltage outputs from the power supply.

4-9. Test Procedures

WARNING

When cable current crowbar circuit is faulty, up to 300 volts dc may be present at +4.500V and RTN TEST POINTS when 45MA TEST LOAD switch is set to CROWBAR. DEATH or serious injury may occur upon contact with noninsulated probes in these test points.

a. Test Requirements.

(1) *Receiving Test.* Perform the procedures in *b* below on each power supply returned from a user. The test will confirm that the power supply is faulty or that the problem can be corrected by performing one or more of the three adjustments in the unit. The test also serves as the initial troubleshooting procedure by determining which functional circuits are faulty and which of the troubleshooting tables in section IV will be used to isolate the faulty components.

(2) *Performance Test.* Perform the procedures in *b* below on each power supply that has been adjusted or repaired. Each time an adjustment or repair is performed, all the test procedures will be repeated to insure that the power supply is operationally ready to be returned to the user or stock.

b. Test Procedures.

(1) Perform the procedures in table 4-4 to test a power supply. The acceptable outputs or conditions being checked are listed under the "Normal indication" column after the procedures that require an indication. When all the procedures are performed without an abnormal indication, the power supply is returned to the user or stock.

(2) When an abnormal indication is obtained for a given step, perform the adjustment procedure listed under the "Normal indication" column. If there is no adjustment procedure listed for a given step, or if it is determined that the adjustment cannot correct the abnormal indication, then the procedures in the appropriate troubleshooting table in section IV will be performed to isolate the malfunction.

(3) There are two troubleshooting tables in section IV. Use table 4-6 when an abnormal condition is obtained for any one of steps 5 through 13. Use table 4-7 when an abnormal condition is obtained for any one of steps 14 through 19.

WARNING

> DEATH or SERIOUS INJURY may occur upon contact with high voltage components in an energized power supply. To prevent contact with power supply components, ensure that cover is properly installed on power supply before performing the test procedures in table 4-4.

c. +5-Volt Adjustment Procedure. Perform the following adjustment procedure when directed in table 4-4. Controls on the power supply breakout box are set in the positions as directed in table 4-4.

(1) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(2) Remove cover from power supply by removing four sets oı screws and washers securing cover to heat sink assembly.

WARNING

> DEATH or SERIOUS INJURY may occur upon contact with components in an energized power supply. Use extreme caution when performing adjustment procedure.

(3) Set AC POWER switch to ON.

(4) Adjust R34 (fig. 4-1) on circuit card for +5.0 ±0.005-volt indication on DMM. (DMM is connected to +5V and GND TEST POINTS on breakout box.) If the +5-volt crowbar circuit energizes (DMM indication goes to zero) during adjustment of R34, adjust R34 to center position and then set AC POWER switch to OFF and back to ON to reset crowbar circuit. When adjustment cannot be made, proceed to the troubleshooting procedures in table 4-6.

(5) Set AC POWER switch to OFF.

(6) Install cover on power supply, using screws and washers removed in (2) above.

(7) Set AC POWER switch to ON and repeat step 5 in table 4-4.

d. 45 MA Cable Current Adjustment Procedure. Perform the following adjustment procedure when directed in table 4-4. Controls on the power supply breakout box are set in the positions as directed in table 4-4.

(1) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(2) Remove cover from power supply by removing four sets of screws and washers securing cover to heat sink.

WARNING

> DEATH or SERIOUS INJURY may occur upon contact with components in energized power supply. Use extreme caution when performing adjustment procedure.

(3) Set AC.POWER switch to ON.

(4) Rotate 45MA TEST LOAD switch to ADJ and then connect DMM leads to +4.500V and RTN TEST POINTS.

(5) Adjust R72 (fig. 4-1) on circuit card for +4.5 ±0.01-volt indication on DMM. If the 45 ma cable current crowbar energizes (DMM indication is less than 2.0 volts), rotate R72 to approximate center position and then set AC POWER switch to OFF and back to ON. If the 45 ma cable current crowbar energizes again (DMM indication is still less than 2.0 volts), proceed to (9) below.

(6) Set AC POWER switch to OFF.

(7) Install cover on power supply, using screws and washers removed in (2) above.

(8) Set AC POWER switch to ON and proceed to step 15 in table 4-4.

(9) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(10) Remove jumper P7 from J21 and J22 on circuit card in power supply (fig. 4-1).

(11) Set AC POWER switch to ON. Adjust R72 for +4.5 ±0.01-volt indication on DMM. When adjustment cannot be made, proceed to troubleshooting procedures in table 4-7.

(12) Set AC POWER switch to OFF. Install jumper P7 in J21 and J22 on circuit card.

(13) Set AC POWER switch to ON. Observe that DMM indicates +4.5 ±0.01 volts. If DDM indication is less than 2.0 volts, perform the 45 ma cable current crowbar adjustment procedure in *e* below.

(14) Proceed to step 15 in table 4-4.

e. 45 MA Cable Current Crowbar Adjustment Procedure. Perform the following adjustment procedure when directed in *d* above or in table 4-4. Controls on the power supply breakout box are set in the positions as directed in table 4-4.

(1) On breakout box, set AC POWER switch to

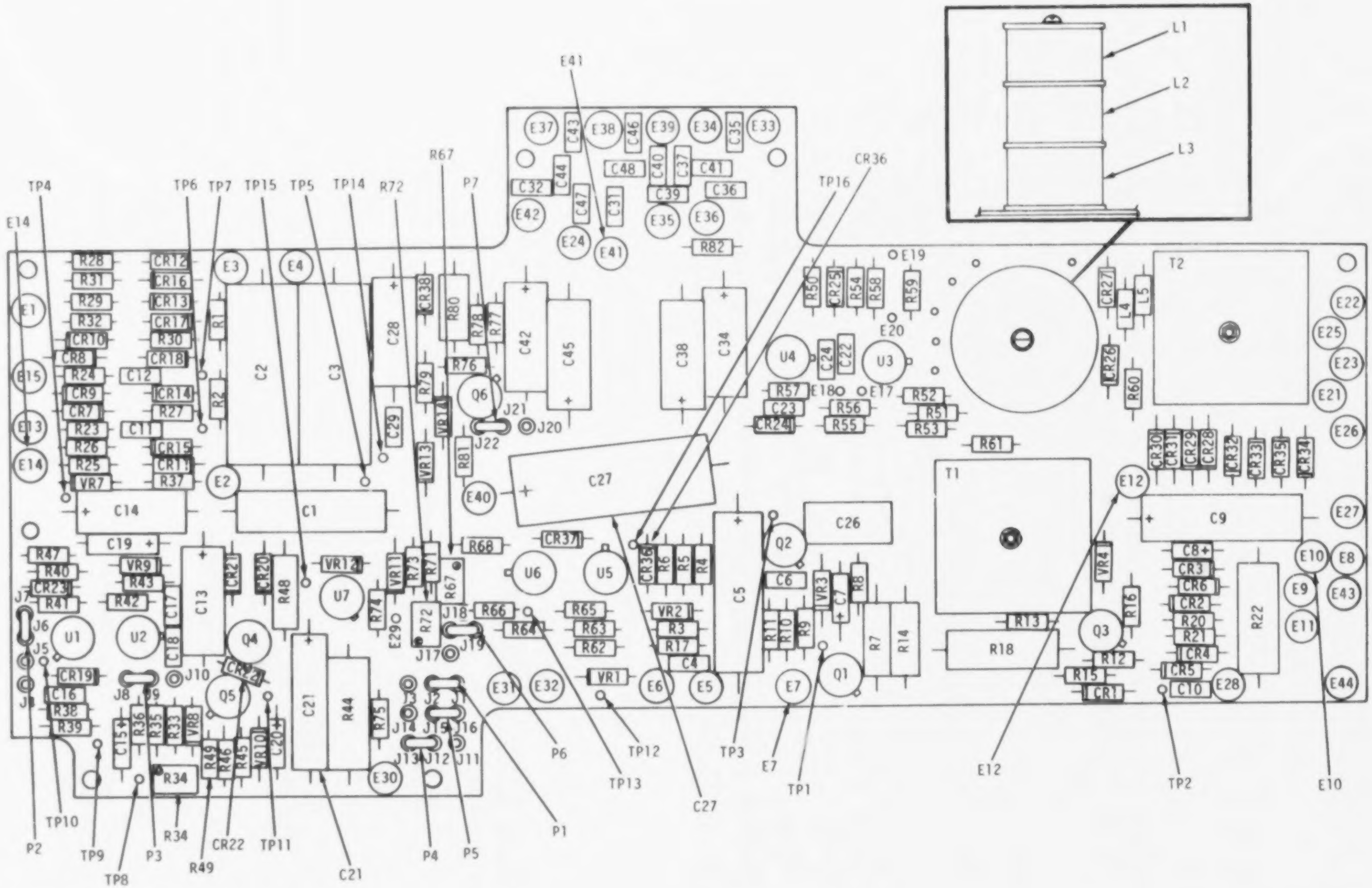
L1
L2
L3
E41
R67
CR36
TP4
TP6
TP7
TP15
TP5
TP14
R72
P7
TP16
E14
T2
T1
E12
E10
TP2
TP1
E7
TP3
C27
TP13
TP12
P6
P1
P5
P4
C21
TP11
CR22
R49
R34
P3
TP8
TP9
TP10
P2
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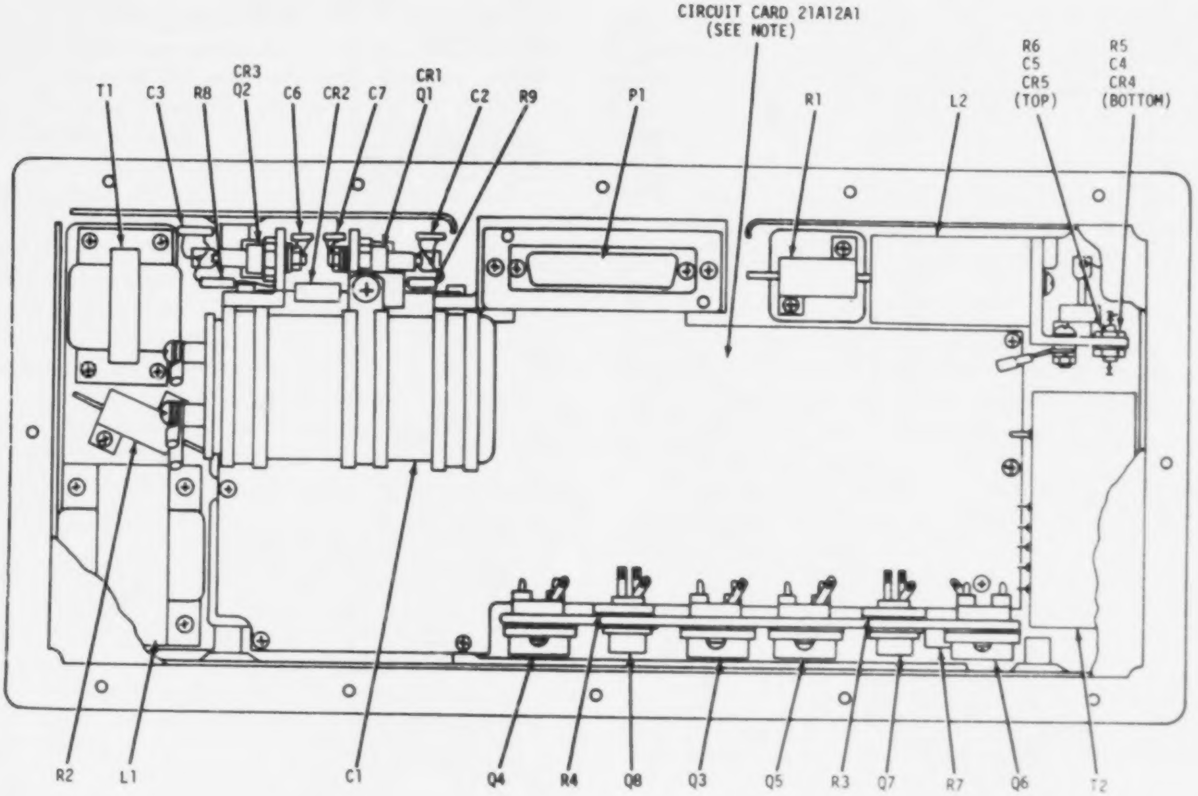
Figure 4-1. Circuit card 21A12A1 components location diagram.


CIRCUIT CARD 21A12A1
(SEE NOTE)
T1
C3
R8
CR3
Q2
C6
CR2
C7
CR1
Q1
C2
R9
P1
R1
L2
R6
C5
CR5
(TOP)
R5
C4
CR4
(BOTTOM)
R2
L1
C1
Q4
R4
Q8
Q3
Q5
R3
Q7
R7
Q6
T2

NOTE:
SEE CIRCUIT CARD 21A12A1 COMPONENT LOCATION DIAGRAM
FOR IDENTIFICATION OF COMPONENTS ON CIRCUIT CARD.

EL5NG147

Figure 4-2. Heat sink components location diagram.

OFF. Observe that AC POWER ON indicator is out.

(2) If installed, remove cover from power supply by removing four sets of screws and washers securing cover to heat sink.

(3) Connect DMM LEADS TO TP12 and E14 on circuit card in power supply.

WARNING

DEATH or SERIOUS INJURY may occur upon contact with components in energized power supply. Use extreme caution when performing adjustment procedure.

(4) Set AC POWER switch to ON.

(5) Adjust R67 (fig. 4-1) on circuit card for 0.000 ±0.005-volt indication on DMM. When adjustment cannot be made, proceed to troubleshooting procedures in table 4-7.

(6) Set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(7) Install cover on power supply, using screws and washers removed in (2) above.

(8) Set AC POWER switch to ON and then proceed to step 16 in table 4-4.

Table 4-4. Power Supply Test Procedures

Step	Procedure	Normal indication
	SETUP PROCEDURES	
1	On power supply breakout box, set switches as follows: AC POWER to OFF. MONITOR TEST − 4.4V to ON. MONITOR TEST + 12V to ON. MONITOR TEST − 12V to ON. +5V CROWBAR TEST to OFF. 45MA TEST LOAD to MIN. VOLTAGE TEST +5V to MIN. VOLTAGE TEST − 4.4V to MIN. VOLTAGE TEST + 12V to MIN. VOLTAGE TEST − 12V to MIN. NOTE All switches and test points in the following procedures are on the breakout box unless otherwise indicated.	
2	Connect breakout box ac power cord (P2) to 115-volt, 60 Hz power source. Set AC POWER switch to ON and observe that AC POWER ON indicator lights and blower fan energizes. Set AC POWER switch to OFF.	This test confirms that AC POWER fuse is not blown and AC POWER ON indicator lights on breakout box.
3	Connect test equipment and power supply as shown in figure 4-3. (Connectors P3 and P4 on breakout box are not used in the test procedures.)	
	DC OUTPUT VOLTAGE TEST	
4	Set AC POWER switch to ON.	AC POWER ON indicator lights. Disregard other indicators at this time.
5	Using DMM, measure dc voltages between: +5V and GND TEST POINTS.	+5.0 ±0.005 volts. If voltage is out of tolerance but within range of +5.55 to +4.45 volts, perform adjustment procedure in paragraph 4-9c. Then repeat this step.
	−4.4V and GND TEST POINTS.	−4.5 ± 0.4 volts.
	+12V and GND TEST POINTS.	+12 ± 1.3 volts.
	−12V and GND TEST POINTS.	−12 ± 1.3 volts.
6	Set four VOLTAGE TEST switches to MAX. Using DMM, measure dc voltages between:	
	+5V and GND TEST POINTS.	+5 ± 0.25 volts.
	−4.4V and GND TEST POINTS.	−4.5 ± 0.4 volts.
	+12V and GND TEST POINTS.	+12 ± 1.3 volts.
	−12V AND GND TEST POINTS.	−12 ± 1.3 volts.
7	Set four VOLTAGE TEST switches to MIN.	
8	Using oscilloscope, measure the ripple voltage between: *Test Points* — *Voltage measured*	
	+5V and GND — +5-volt output	Less than 300 millivolts peak to peak.
	−4.4V and GND — −4.4-volt output	Less than 200 millivolts peak to peak.
	+12V and GND — +12-volt output	Less than 300 millivolts peak to peak.
	−12V and GND — −12-volt output	Less than 300 millivolts peak to peak.
	DC MONITOR TEST	
9	One at a time, set MONITOR TEST −4.4V, +12V, and −12V switches to OFF and then back to ON.	DC POWER indicator is lit when three switches are in ON position. DC POWER indication is out when each switch is in OFF position.
	+5-VOLT CROWBAR TEST	
10	Connect DMM leads to +5V and GND TEST POINTS.	
11	Set four VOLTAGE TEST switches to MAX.	
12	Set +5V CROWBAR TEST switch to ON and then back to OFF.	DMM indicates less than 0.05 volt.
13	Set AC POWER switch to OFF and then back to ON.	DMM indicates +5.0 ± 0.25 volts.

Table 4-4. Power Supply Test Procedures—Continued

Step	Procedure	Normal indication
	45 MA CABLE CURRENT REGULATION TEST	
	WARNING When cable current crowbar circuit is faulty, up to 300 volts dc may be present at +4.500V and RTN TEST POINTS when 45MA TEST LOAD switch is set to CROWBAR. DEATH or serious injury may occur upon contact with non-insulated probes in these test points.	
14	Rotate 45MA TEST LOAD switch to ADJ and connect DMM leads to +4.500V and RTN TEST POINTS. Observe indication on DMM.	+4.5 ± 0.01 volts. *a.* If voltage is out of tolerance but within range of 4.5 ± 0.5 volts, perform adjustment procedure in paragraph 4-9*d*. *b.* If voltage is less than 2.0 volts, set AC POWER switch to OFF and back to ON to reset 45 ma cable current crowbar circuit. If normal indication is not obtained, perform adjustment procedure in paragraph 4-9*d*.
15	Connect DMM leads to ±2.529V and RTN TEST POINTS. Rotate 45 MA TEST LOAD switch to MIN, NOM, and MAX positions. Observe DMM indication at each switch position.	−2.529 ± 0.1 volts at each position. If voltage is out of tolerance but within range of −3.0 to −2.0 volts, perform adjustment procedure in paragraph 4-9*d* if they have not already been performed (step 14 above); otherwise, proceed to troubleshooting procedures in table 4-7.
	45 MA CABLE CURRENT CROWBAR TEST	
16	Set VOLTAGE TEST +5V switch to MIN.	Ignore MONITOR TEST DC POWER indicator.
17	Rotate 45MA TEST LOAD switch to ADJ, and connect DMM leads to +4.500V and RTN TEST POINTS. Observe indication on DMM.	+4.5 ± 0.01 volts.
18	Rotate 45MA TEST LOAD switch to CROWBAR and then back to ADJ. Observe indication on DMM.	Less than +2.0 volts. If crowbar function does not occur, perform adjustment procedure in paragraph 4-9e.
19	Set AC POWER switch to OFF and then back to ON. Observe indication on DMM.	+4.5 ± 0.01 volts.
20	Set AC POWER switch to OFF.	VOLTAGE TEST (4) indicators are out.
21	Disconnect test setup.	

Section IV. POWER SUPPLY TROUBLESHOOTING PROCEDURES

4-10. Introduction

This section contains the troubleshooting procedures for isolating a faulty electrical component in the power supply. There are two troubleshooting tables in this section; the troubleshooting table that will be used to locate a specific type of malfunction is determined by performing the power supply test procedures in section III. The procedures in section III must be performed before attempting to troubleshoot an energized power supply.

4-11. Tools and Test Equipment Required for Power Supply Troubleshooting

The tools and test equipment required for performing the troubleshooting procedures are listed in table 4-5.

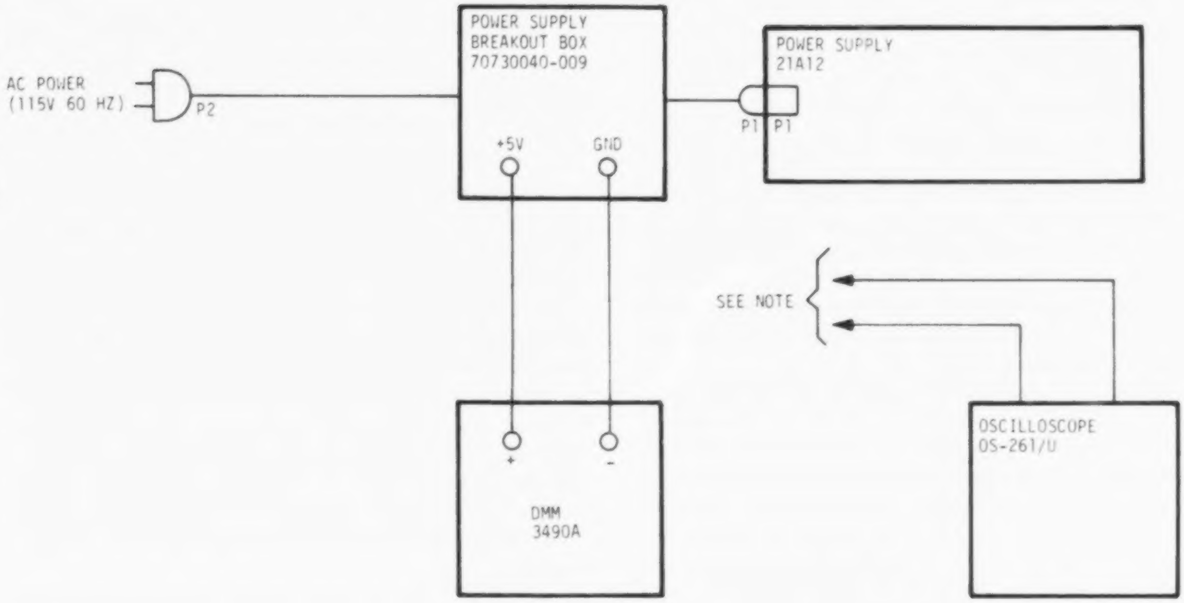
4-12. Troubleshooting Techniques

a. General. When a faulty power supply is received for repair, the inspection and test procedures in section III are part of the overall troubleshooting function. In section III, the overall physical and electrical operation of the faulty power supply is evaluated as described in *b* and *c* below. This section contains the troubleshooting information for locating the malfunction in the power supply (*d* below).

b. Visual Inspection. With the cover removed from the heat sink assembly, the electrical components and wiring are inspected as directed in table 4-2. The power supply should not be energized for dynamic troubleshooting before confirming that there is no visible damage to electrical components in the unit.

c. Test Procedures. The test procedures in table 4-4 confirm that the power supply is faulty and that the faulty condition is not caused by an adjustment that is out of tolerance. The procedures in table 4-4 also determine which one of the two troubleshooting tables is to be used to troubleshoot the faulty power supply.

d. Troubleshooting. The troubleshooting procedures in tables 4-6 and 4-7 are dynamic checks performed with the power supply energized. The procedures consist of checking ac and dc voltage levels and monitoring selected waveforms at key test points in the circuits. The procedures in troubleshooting tables must be performed in the sequence they are presented. The



NOTE:
CONNECT OSCILLOSCOPE
AS DIRECTED IN PROCEDURES.

EL5NG153

Figure 4-3. Power supply test setup diagram.

circuit card in the power supply contains seven removable jumpers (P1 through P7). By removing one or more of the jumpers as directed in the troubleshooting procedures, the faulty functional circuit(s) in the power supply can be isolated. This isolation capability allows the fault symptom to be isolated to the stage level.

e. Troubleshooting Aids. The following troubleshooting aids are available to troubleshoot a faulty power supply.

(1) *Power supply breakout box.* This breakout box contains the switches, resistive loads, and test points that allow testing and troubleshooting of the power supply in a bench test configuration. The breakout box requires a 115-volt ±10 percent, 45-65 Hz, 160-watt external power source.

(2) *Schematic diagram.* Figure FO-14 is the power supply schematic diagram. It includes the schematic diagram for the circuit card (circuit card assembly SM-D-941852) mounted on the heat sink assembly (heat sink).

(3) *Component location diagrams.* Figure 4-1 is the component location diagram for the circuit card. The electrical components that are not mounted on the circuit card itself are mounted on the heat sink; figure 4-2 shows the location of these components. The RPSTL that contains the list of part numbers and disassembly illustrations is in TM 11-7025-202-34P.

(4) *Wire run list.* Table 4-9, the power supply wire run list, contains the point-to-point wire runs between the components on the heat sink and the wiring terminals (E's) on the circuit card.

4-13. Troubleshooting Procedures

a. General. The troubleshooting procedures in this paragraph are used when the test procedures in table 4-4 are performed and an abnormal indication is detected in one of the steps. If the abnormal indication occurred in steps 5 through 13 in table 4-4, troubleshooting table 4-6 is used to isolate the malfunction. If the abnormal indication occurred in steps 14 through 19, troubleshooting table 4-7 is used to isolate the malfunction.

b. Use of Troubleshooting Tables. Table 4-6 contains the troubleshooting procedures for checking the circuits that perform the 115-volt ac-to-dc conversion functions and the circuits that produce the four regulated dc output voltages. Table 4-7 contains the troubleshooting procedures for checking the circuits that produce and regulate the 45 ma cable current out-

Table 4-5. Test Equipment Required for Power Supply Troubleshooting

Test equipment	Qty	NSN or part No.
Digital multimeter (DMM)	1	6625-01-010-9255
Oscilloscope OS-261/U	1	6625-00-127-0079
Power supply	1	DCR-80-10 (Raytheon)
Power supply breakout box	1	70730040-009 (Martin Marietta)

put. Each table contains the following troubleshooting information.

(1) The "Procedure/normal indication" column contains the test equipment setup configurations and equipment control settings. It also contains the normal indication when the procedure requires a measurement or a waveform check.

(2) The "If indication is abnormal" column contains an entry when there is a normal indication required in the "Procedure/normal indication" column for a given step. The entry contains the troubleshooting action that is performed to isolate the malfunction and lists the components most likely to cause the specific malfunction. When the listed components are not faulty, refer to the power supply schematic and wire run list and check the wiring and other components associated with the designated components.

(3) Functional headings are added in the center of the tables to separate the functional circuits being checked. These functional headings are described in c below.

c. *Troubleshooting Functional Description.* The troubleshooting procedures in table 4-6 check the dc power supply circuits as described in (1) through (15) below. In turn, the troubleshooting procedures in table 4-7 check the cable power supply circuits as described in (16) through (18) below.

(1) *Isolation checks.* These checks (step 1 of table 4-6) determine if the collectors (case) of Q3 through Q8, cathodes (mounting stud) of CR1, CR3, CR4, and CR5, and anodes (mounting stud) of Q1 and Q2 are properly insulated from the heat sink assembly (chassis ground).

(2) *115 v ac input resistance checks.* These checks (step 2) determine if components connected across the 115-volt ac input terminals are shorted. If one of the components is shorted, it could cause the AC POWER fuse on the breakout box to open when the AC POWER switch is set to ON.

(3) *Heat sink transistor checks.* In these checks (step 3), each transistor (Q3 through Q8) is removed from the heat sink and checked to see if it is faulty. Removing the transistors also serves to isolate some of the functional circuits for troubleshooting.

(4) *Control voltage checks.* These checks (steps 7 through 11) determine if the dc control voltages that power the control circuits are present and within tolerance.

(5) *Control circuits checks.* These checks (steps 12 through 24) determine if the control circuits are faulty.

(6) *+5-volt crowbar overvoltage circuit checks.* These checks (steps 25 through 27) determine if the crowbar circuit is faulty. An external power supply is used to simulate the overvoltage condition.

(7) *Chopper circuit checks.* These checks (steps 28 through 33) determine if the chopper circuit is faulty. The checks also determine if one of the dc output voltage circuits or the cable current output circuit is faulty to the extent that the output circuit creates an excessive load on the chopper circuit and causes it to malfunction.

(8) *Active filter circuit checks.* These checks (steps 34 through 37) determine if the active filter circuit contains an open or shorted fault condition. An external power supply is used to power the isolated active filter circuit in these checks.

(9) *Functional dc output voltage checks.* These checks (steps 38 through 47) determine if the dc output voltages (+12, +5, −4.4, and −12 volts) are missing. The checks are performed as a precautionary procedure before energizing the power supply in later steps. If the +5-volt dc output is missing, the power supply cannot be energized until the fault is repaired. The regulation of the dc outputs is checked in later steps as described in (11) through (14) below.

(10) *Active filter circuit ripple check.* This check (step 48) determines if the active filter circuit is faulty under normal operating conditions.

(11) *+5 v output and +5-volt crowbar circuit checks.* These checks (steps 49 through 52) determine if the +5-volt regulation circuits are faulty under minimum and maximum loading conditions. A dynamic check of the +5-volt crowbar circuit is also performed.

(12) *−4.4 v output circuit check.* This check (step 53) determines if the −4.4-volt regulation circuits are faulty under minimum and maximum loading conditions.

(13) *+12 v output circuit check.* This check (step 54) determines if the +12-volt regulation circuits are faulty under minimum and maximum loading conditions.

(14) *−12 v output circuit check.* This check (step 55) determines if the −12-volt regulation circuits are

faulty under minimum and maximum loading conditions.

(15) *Dc monitor circuit check.* This check (step 56) determines if the dc monitor circuit is faulty.

(16) *Isolation checks.* These checks (steps 1 through 3 of table 4-7) determine if the collectors (case) of Q7 and Q8 and cathodes of CR4 and CR5 are shorted to the heat sink (chassis ground).

(17) *45 ma cable current regulation circuit checks.* These checks (steps 7 through 18) determine if the 45 ma cable current regulation circuits are faulty. In this test, the 45 ma crowbar circuit is disconnected to prevent interaction by the circuits.

(18) *45 ma cable current crowbar circuit checks.* These checks (steps 19 through 24) determine if the 45 ma crowbar circuit is faulty under dynamic operating conditions.

d. Troubleshooting Procedures. Perform the troubleshooting procedures in table 4-6 or 4-7. Perform all the steps in sequence presented; otherwise, the power supply circuits may not be properly configured for a given check and an erroneous indication could be obtained. When the malfunction is detected and the faulty component(s) or wiring is isolated, perform the appropriate repair procedures as directed in section V. After the repair has been performed, proceed through the remaining steps in the table. This ensures that there are no more malfunctions in the unit and that the power supply is returned to its normal operating configuration. In the course of performing the troubleshooting procedures, one or more of jumpers P1 through P7 on the circuit card and transistors Q3 through Q8 on the heat sink are removed. These items are replaced in the later steps of the tables. In both troubleshooting tables, the power supply is returned to its operating configuration by the end of the procedural steps. When the procedures in the appropriate troubleshooting table are completed and the appropriate repairs have been made, perform the procedures in table 4-4 as the final performance standards to ensure that the power supply is operational.

Table 4-6. DC Power Supply Circuits Troubleshooting Procedures

Step	Procedure/normal indication	If indication is abnormal
	WARNING DEATH or SERIOUS INJURY may occur upon contact with components in the power supply. Up to 400 volts ac and dc are present on exposed electrical components when the cover is removed from an energized power supply. Do not perform any adjustments or circuit modifications or apply power until directed in the following procedures.	
	ISOLATION CHECKS	
1	*a.* If installed, remove cover from heat sink. Remove jumper P4 from J12 and J13, P5 from J15 and J16, and P6 from J18 and J19 on circuit card. *b.* Using DMM, check resistance between heat sink assembly (chassis) and transistor collectors (case) listed below. *(– lead)* / *(+ lead)* / *Normal indication* Chassis / Q3 / Greater than 1 megohm Chassis / Q4 / Greater than 1 megohm Chassis / Q5 / Greater than 1 megohm Chassis / Q6 / Greater than 1 megohm Chassis / Q7 / Greater than 1 megohm Chassis / Q8 / Greater than 1 megohm	Remove transistor(s) as directed in paragraph 4-14*a* and check for faulty insulator. Install transistor and known good insulator on heat sink as directed in paragraph 4-14*b*. Repeat insulation checks before proceeding to *c* below.
	c. Install jumper P4 in J12 and J13, P5 in J15 and J16, and P6 in J18 and J19 on circuit card. *d.* Using DMM, check resistance between heat sink assembly (chassis) and mounting studs of components listed below. *(– lead)* / *(+ lead)* / *Normal indication* Chassis / CR1 / Greater than 1 megohm Chassis / CR3 / Greater than 1 megohm Chassis / CR4 / Greater than 50K ohms Chassis / CR5 / Greater than 50K ohms Chassis / Q1 / Greater than 1 megohm Chassis / Q2 / Greater than 1 megohm	Remove component as directed in paragraph 4-14*d* and check for faulty insulator. Install component and known good insulators on heat sink as directed in paragraph 4-14*e*. Repeat insulation checks before proceeding to step 2.
	115-VAC INPUT RESISTANCE CHECKS	
2	Using DMM, perform the following checks. *(– lead)* / *(+ lead)* / *Normal indication*	
	P1-A1 / P1-A2 / Greater than 300 ohms	Check T1, A1C1, and CR3.
	P1-A2 / P1-A1 / Greater than 300 ohms	Check T1, A1C1, and CR1.
	P1-A1 / Chassis / Greater than 100K ohms	Check A1C2, CR1, and CR3.
	P1-A2 / Chassis / Greater than 100K ohms	Check A1C3, CR1, and CR3.

Table 4-6. DC Power Supply Circuits Troubleshooting Procedures—Continued

<table>
<tr><th>Step</th><th>Procedure/normal indication</th><th>If indication is abnormal</th></tr>
<tr><td colspan="3">HEAT SINK TRANSISTOR CHECKS</td></tr>
<tr><td colspan="3">CAUTION
Failure to remove all of the transistors in step 3 may cause additional equipment damage to power supply circuits when performing troubleshooting procedures.</td></tr>
<tr><td>3</td><td>One at a time, remove Q3 through Q8 from heat sink and perform resistance checks as directed in paragraph 4-14a.</td><td></td></tr>
<tr><td colspan="3">SETUP PROCEDURES FOR DYNAMIC CHECKS</td></tr>
<tr><td>4</td><td>Remove jumpers P2 (J6 to J7) and P3 (J8 to J9) on circuit card.</td><td></td></tr>
<tr><td>5</td><td>On power supply breakout box, set switches as follows:
AC POWER to OFF.
MONITOR TEST - 12V to ON.
MONITOR TEST + 12V to ON.
MONITOR TEST - 4.4V to ON.
+5V CROWBAR TEST to OFF.
45MA TEST LOAD to MIN.
VOLTAGE TEST +5V to MIN.
VOLTAGE TEST - 4.4V to MIN.
VOLTAGE TEST + 12 V to MIN.
VOLTAGE TEST - 12V to MIN.</td><td></td></tr>
<tr><td colspan="3">CAUTION
When performing step 6, the ground wire in test equipment power cords must be isolated from power source ground. Otherwise, the power supply under test and the test equipment may be damaged when performing the following steps in this table. Ensure that power supply under test and test equipment cases do not come in contact with anything such as work benches or test equipment stands that are connected to ground potential.</td></tr>
<tr><td>6</td><td>Connect test equipment and power supply as shown in figure 4-4.</td><td></td></tr>
<tr><td colspan="3">WARNINGS
• DEATH or SERIOUS INJURY may occur upon contact with components in the power supply. Up to 400 volts ac and dc are present in the power supply when AC POWER indicator on breakout box is lit.
• DDM, power supply, and oscilloscope are not connected to ground. Up to 500 volts may be present between test equipment and test points on the power supply. Use extreme caution when performing checks to prevent DEATH or serious injury.
CAUTION
A high voltage short caused by test equipment leads can cause extensive damage to components and may cause extensive damage to printed wiring on circuit board. Before setting AC POWER switch to ON, ensure that test leads are insulated and securely fastened to test points and there are no shorting conditions between components caused by test leads.
NOTE
All switches and test points called out in the procedures are on the power supply breakout box unless otherwise indicated.
Components mounted on the circuit card (fig. 4-1) in the power supply are prefixed by "A1" in the procedures. Components mounted on the heat sink (fig. 4-2) in the power supply are identified without a prefix in the procedures. For example, Q4 is on the heat sink and A1Q4 is on the circuit card.</td></tr>
<tr><td colspan="3">CONTROL VOLTAGE CHECKS</td></tr>
<tr><td>7</td><td>Set AC POWER switch to ON. AC POWER ON indicator is lit.</td><td>If indicator is out because of open AC POWER fuse, check:
a. A1C1, A1C2, and A1C3.
b. Primary of T1.
c. CR1, CR2, CR3, Q1, and Q2.</td></tr>
<tr><td>8</td><td>Set external power supply input to + 5.0 ± 0.05 volts.</td><td></td></tr>
<tr><td colspan="3">WARNINGS
Up to 500 volts dc and ac may be present between test equipment and test points on the power supply. Use extreme caution when performing checks to prevent DEATH or SERIOUS INJURY. Perform the following safety procedures when making connections in steps 9 through 22.
• Set AC POWER switch to OFF. AC POWER ON indicator must be out.
• Connect insulated test leads to desired points. Check that test leads are properly connected and not shorted to any adjacent parts.
• Set AC POWER switch to ON and observe safety procedures for working on high-voltage equipment.</td></tr>
<tr><td>9</td><td>Move DMM lead from A1J8 to A1TP4. DMM indicates + 15 ± 5.0 volts.</td><td>Check A1CR7 and A1CR8.</td></tr>
<tr><td>10</td><td>Move DMM lead from A1TP4 to A1TP5. DMM indicates - 15 ± 5.0 volts.</td><td>Check A1CR9 and A1CR10.</td></tr>
<tr><td>11</td><td>Move DMM lead from A1E14 to A1TP4. DMM indicates - 30 ± 5.0 volts.</td><td>Check A1VR7.</td></tr>
</table>

Table 4-6. DC Power Supply Circuits Troubleshooting Procedures—Continued

Step	Procedure/normal indication	If indication is abnormal
	CONTROL CIRCUITS CHECKS	
12	On oscilloscope, check 60 Hz, 2.0 to 5.0-volt peak-to-peak waveform (fig. 4-5, A).	Check T1, A1CR11, A1CR12, A1CR15, and A1CR16.
13	Move oscilloscope lead from A1TP6 to A1TP7. Observe same waveform as in step 12.	Check T1, A1CR13, A1CR14, A1CR17, and A1CR18.
14	Move oscilloscope lead from A1TP7 to A1J5. Connect DMM leads to A1J8(+) and A1E14(−).	
15	Rotate A1R34 fully counterclockwise (approximately eight turns).	
16	Set oscilloscope to display a negative dc trace line and set vertical gain for 5V/CM. Adjust external power supply until DMM indicates +5.0 ± 0.05 volts.	
17	Slowly rotate A1R34 clockwise until trace line displayed on oscilloscope starts to go positive. Observe external power supply output as indicated on DMM is +5.0 ±0.1 volts at the time that the dc voltage starts to rise. CAUTION After A1R34 is properly set in step 17, do not readjust A1R34 or external power supply unless directed to do so in the following procedures. If A1R34 is not properly set, faulty indications may occur for a given check.	Check A1U1 and A1R34 and associated components.
18	Install jumper P2 in A1J6 and A1J7.	
19	Move oscilloscope probe to A1TP10.	
20	On oscilloscope, observe 120 Hz, 25 to 35 volts peak-to-peak waveform (fig. 4-5, B). If waveform is missing, slowly adjust A1R34 clockwise (up to two turns) until proper waveform appears. Otherwise, circuit is faulty.	Check A1U2 and associated components.
21	Move oscilloscope probe from A1TP10 to A1CR22 anode. Observe 120 Hz, 1.2 to 3.0-volt peak-to-peak waveform (fig. 4-5, C).	Check A1Q4, A1CR22, and A1C18.
22	On oscilloscope, check waveform across A1R49 by connecting probe return to negative lead of A1C21 and holding probe to A1Q5 case. Observe 120 Hz, 3.0 to 7.0-volt waveform (fig. 4-5, D).	Check A1Q4, A1Q5, A1VR10, and associated components.
23	Set AC POWER switch to OFF. External 115 volts ac is not used in steps 24 through 44.	
24	Set external power supply output to zero. Then connect power supply leads to A1E7(+) and A1E10(−).	
	+5-VOLT CROWBAR OVERVOLTAGE CIRCUIT CHECKS	
25	Connect DMM leads to A1TP1(+) and A1E10(−).	
26	Slowly increase external power supply output (not to exceed 80 volts) until DMM indicates +1.5 volts or greater. External power supply output is +75 ± 5.0 volts.	*a.* If +1.5 volts or greater is obtained when external power supply output is less than +60 volts, check A1Q1 and associated circuits. *b.* If +1.5 volts or greater is not obtained, check A1Q3 and associated components.
27	Set external power supply output to zero.	
	CHOPPER CIRCUIT CHECKS	
28	Install Q5 and Q6 on heat sink. Refer to paragraph 4-14*b*.	
29	Using DMM, check insulation resistance between Q5 case to heat sink and Q6 case to heat sink. Observe that DMM indicates greater than 1 megohm for each check.	Remove transistor, check insulator for damage, install transistor, and repeat this step.
30	Remove jumper P5 from A1J15 and A1J16 and jumper P6 from A1J18 and A1J19. Connect P3 and P4 from breakout box in A1J15 and A1J18, respectively.	
31	Connect oscilloscope probe to A1E12(+) and probe ground to A1E10(−).	
32	Slowly increase external power supply output to +60 volts (dial accuracy). On oscilloscope, observe 20 +6.0 kHz, 120 ±5.0-volt peak-to-peak waveform. Any overshoot on square wave is less than 2.0 volts (fig. 4-5, E).	*a.* If overshoot is greater than 2.0 volts, check for open A1CR5 or A1CR6. *b.* If waveform is missing: (1) Check Q5 and Q6.

Table 4-6. DC Power Supply Circuit Troubleshooting Procedures—Continued

Step	Procedure/normal indication	If indication is abnormal
		(2) Check A1CR5 and A1CR6. (3) Check A1R18 and R7. (4) Check A1T1. (5) Check T2 as directed in *d* below. *c*. If waveform is distorted: (1) Check components in base circuit Q5 and Q6. (2) Check T2 as directed in *d* below. *d*. A distorted or missing square wave may be caused by a faulty T2 or excessive loading on one of the secondary outputs of T2. Troubleshoot T2 by disconnecting the secondary outputs of T2, one at a time, until waveform appears or all outputs are disconnected.
33	Set external power supply output to zero.	

ACTIVE FILTER CIRCUIT CHECKS

Step	Procedure/normal indication	If indication is abnormal
34	Install Q3 and Q4 on heat sink. Refer to paragraph 4-14*b*.	
35	Using DMM, check insulation resistance between Q3 case and heat sink. Check Q4 to heat sink. Observe that DMM indicates greater than 1 megohm.	Remove transistor, check insulator for damage, install transistor, and repeat this step.
36	Move external power supply (+) output from A1E7 to A1E5.	
37	Slowly increase external power supply output to +60 volts (dial accuracy). On oscilloscope, observe 20 ±6.0 kHz, 120 ± 5.0-volt peak-to-peak waveform (fig. 4-5, E).	Check components associated with Q3 and Q4.

FUNCTIONAL DC OUTPUT VOLTAGE CHECKS

Step	Procedure/normal indication	If indication is abnormal
38	Connect DMM leads to +5V and GND TEST POINTS. DMM indicates +5 ± 0.1 volts.	*a*. If voltage is +5.0 ±1.5 volts, adjust external power supply for DMM indication of +5.0 ± 0.1 volts. *b*. If +5 volts is missing, check A1L2, A1CR4, A1CR5, and T2.
39	Connect DMM leads to −4.4V and GND TEST POINTS. DMM indicates −4.4 ± 0.4 volts.	Check A1L1, A1CR26, A1CR27, A1T2, and T2.
40	Connect DMM leads to +12V and GND TEST POINTS. DMM indicates +12.0 ± 1.2 volts.	Check A1L2, A1CR28, A1CR29, and T2.
41	Connect DMM leads to −12V and GND TEST POINTS. DMM indicates −12.0 ± 1.2 volts.	Check A1L3, A1CR30, A1CR31, and T2.
42	Set external power supply output to zero and then remove external power supply leads from A1E5 and A1E10.	
43	Install jumper P3 in A1J8 and A1J9.	
44	Connect DMM leads to +5V and GND TEST POINTS.	

WARNING

Up to 500 volts dc and ac may be present between test equipment and test points on the power supply. Use extreme caution when performing checks to prevent DEATH or SERIOUS INJURY. Perform the following safety procedures when making connections in steps 45 through 56.

- Set AC POWER switch to OFF. AC POWER ON indicator must be out.
- Connect insulated test leads to desired points. Check that test leads are properly connected and not shorted to any adjacent parts.
- Set AC POWER switch to ON and observe safety procedures for working on high-voltage equipment.

NOTE

Proceed to step 48 when normal indication is obtained in step 45.

Step	Procedure/normal indication	If indication is abnormal
45	Set AC POWER switch to ON. DMM indicates +5.0 ±0.005 volts.	If +5 volts is missing, proceed to step 46. When voltage is out of tolerance, adjust A1R34 for normal indication.
46	Connect DMM leads to A1TP3 (+) and A1E10 (−). DMM indication is greater than +5 volts.	Check Q2 and associated components.
47	Connect oscilloscope leads across A1R49. Observe 120 Hz, 3.0 to 7.0-volt waveform (fig. 4-5, D).	*a*. If waveform is missing, check Q5, Q4, and associated components. *b*. If waveform is present, check components in diode/SCR bridge circuit (Q1, Q2, and associated components).

ACTIVE FILTER CIRCUIT RIPPLE CHECK

Step	Procedure/normal indication	If indication is abnormal
48	Connect oscilloscope probe to A1E7 and probe ground to E10. Ripple voltage is 120 Hz and less than 400 millivolts peak-to-peak.	*a*. If ripple voltage is 60 Hz, check Q1, Q3, and associated components in diode/SCR bridge circuit. *b*. If ripple voltage is high, check A1Q3, A1Q4, and associated components.

Table 4-6. DC Power Supply Circuits Troubleshooting Procedures—Continued

Step	Procedure/normal indication	If indication is abnormal
	+5 OUTPUT AND +5 VOLT CROWBAR CIRCUIT CHECKS	
49	Connect oscilloscope and DMM leads to +5V and GND TEST POINTS.	
50	Observe that indication on DMM is +5.0 ± 0.005 volts; ripple voltage is less than 300 millivolts. Set VOLTAGE TEST +5V switch to MAX; indication on DMM is +5.0 ±0.3 volts; ripple voltage is less than 300 millivolts.	Adjust A1R34 with VOLTAGE TEST +5V switch in MIN position. Repeat this step. If normal indication cannot be obtained, check A1L2, A1CR4, A1CR5, associated RC components in +5-volt output circuit, and T2.
51	Set four VOLTAGE TEST switches to MAX.	
52	Set +5V CROWBAR TEST switch to ON and then back to OFF. DMM indicates zero. Set AC POWER switch to OFF and then back to ON. DMM indicates +5.0 ± 0.3 volts.	Check A1Q1, A1Q2, and associated components.
	−4.4V OUTPUT CIRCUIT CHECK	
53	Connect DMM and oscilloscope leads to −4.4V and GND test points. DMM indicates −4.5 ±0.4 volts. Ripple voltage is less than 200 millivolts. Set four VOLTAGE TEST switches to MIN. Observe that indications are still within tolerances.	Check A1L1, A1CR26, A1CR27, associated components in −4.4V output circuit, and T2.
	+12V OUTPUT CIRCUIT CHECK	
54	Connect DMM and oscilloscope leads to +12V and GND TEST POINTS. DMM indicates +12.0 ±1.3 volts. Ripple voltage is less than 300 millivolts. Set four VOLTAGE TEST switches to MAX. Observe that indications are still within tolerances.	Check A1L2, A1CR28, A1CR29, T2, and associated RC components in +12-volt output circuit.
	−12V OUTPUT CIRCUIT CHECK	
55	Connect DMM and oscilloscope leads to −12V and GND TEST POINTS. DMM indicates −12.0 ±1.3 volts. Ripple voltage is less than 300 millivolts. Set four VOLTAGE TEST switches to MIN. Observe that indications are still within tolerances.	Check A1L3, A1CR30, A1CR31, T2, and associated RC components in −12-volt output circuit.
	DC MONITOR CIRCUIT CHECK	
56	Observe that DC POWER indicator is lit when three MONITOR TEST switches are set to ON. One at a time, set −4.4V, +12V, and −12V MONITOR TEST switches to OFF and then back to ON. Observe that DC POWER indicator is out when each switch is set to OFF.	Check A1U3, A1U4, and associated components.
	SHUTDOWN PROCEDURE	
57	Set AC POWER switch to OFF.	
58	Remove breakout box connectors P3 and P4 from power supply. Remove jumper P4 from A1J12 and A1J13.	
59	Install Q7 and Q8 on heat sink. Refer to paragraph 4-14*b*.	
60	Using DMM, measure isolation resistance between collector (case) of Q7 and heat sink assembly. Then measure between collector (case) of Q8 and heat sink assembly. In both measurements, DMM indicates greater than 1 megohm.	Remove Q7 or Q8, check insulator, install Q7 or Q8, and repeat this step.
61	Install jumper P4 in A1J12 and A1J13, P5 in A1J15 and A1J16, and P6 in A1J18 and A1J19.	
62	Check that jumpers P1 through P7 are installed as shown in figure 4-1. Shutdown procedure is complete.	
63	Disconnect test setup.	

Table 4-7. Cable Power Supply Circuits Troubleshooting Procedures

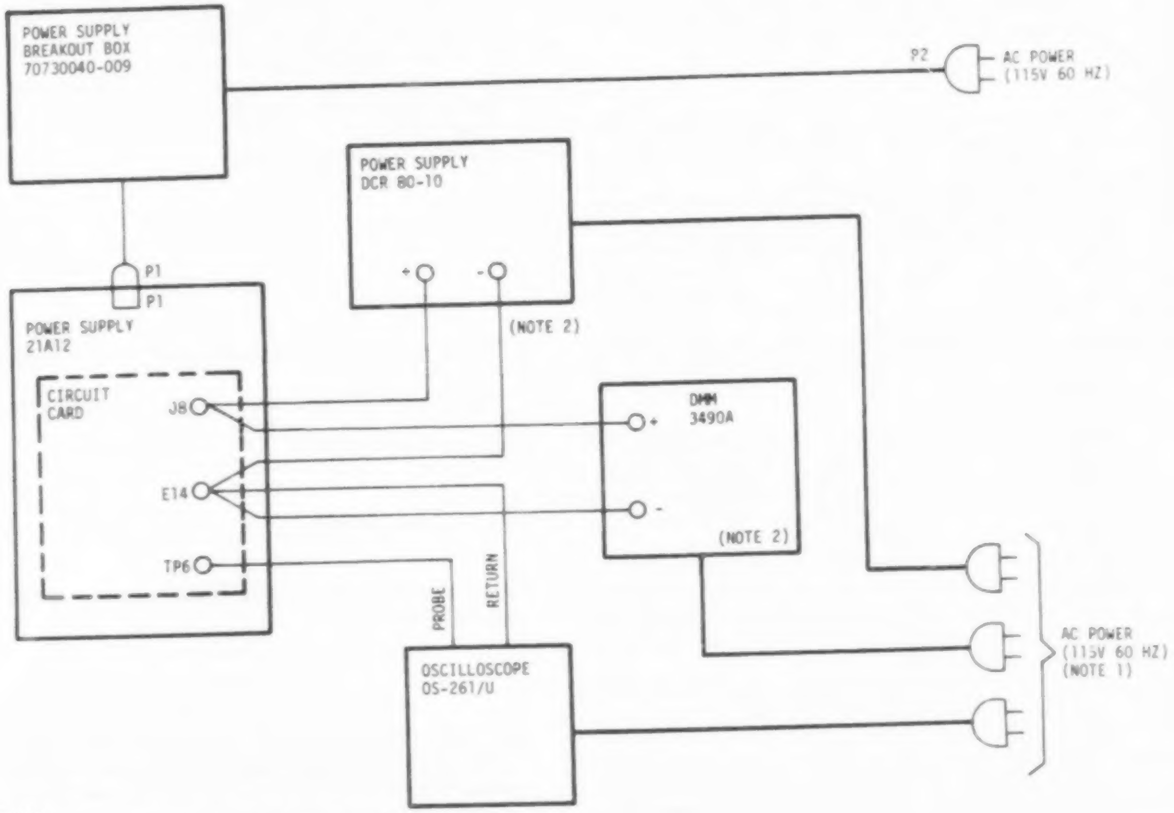
Step	Procedure/normal indication	If indication is abnormal
	WARNING • DEATH or SERIOUS INJURY may occur upon contact with components in the power supply. Up to 400 volts ac and dc are present on exposed electrical components when the cover is removed from an energized power supply. Do not perform any adjustments or circuit modifications or apply power until directed in the following procedures. • If cable current crowbar circuit is faulty, up to 300 volts dc may be present at +4.500V and RTN TEST POINTS when 45MA TEST LOAD switch is set to CROWBAR. DEATH or SERIOUS INJURY may occur upon contact with noninsulated probes in these test points. • DDM, power supply, and oscilloscope are not connected to ground. Up to 500 volts may be present between test equipment and test points on the power supply. Use extreme caution when performing checks to prevent DEATH or SERIOUS INJURY. Perform the following safety procedures when performing dynamic checks directly on the power supply components. • Set AC POWER switch on breakout box to OFF. AC POWER ON indicator must be out. • Connect insulated test leads to desired points. Check that test leads are properly connected and not shorted to any adjacent parts. • Set AC POWER switch to ON and observe safety procedures for working on high voltage equipment. **CAUTION** A high voltage short caused by test equipment leads can cause extensive damage to components and may cause extensive damage to printed wiring on circuit board. Before setting AC POWER switch to ON, ensure that test leads are insulated and securely fastened to test points and there are no shorting conditions between components caused by test leads. **NOTES** All switches and test points called out in the procedures are on the power supply breakout box unless otherwise indicated. Components mounted on the heat sink (fig. 4-2) in the power supply are identified without a prefix in the procedures. Components mounted on the circuit card (fig. 4-1) in the power supply are prefixed by "A1" in the procedures. For example, Q4 is on the heat sink and A1Q4 is on the circuit card.	
	ISOLATION CHECKS	
1	Remove jumper P4 from A1J12 and A1J13, jumper P5 from A1J15 and A1J16, and jumper P6 from A1J18 and A1J19.	
2	*a.* Using DMM, perform the following resistance checks between transistor collectors (case) and heat sink assembly (chassis). *(− lead)* *(+ lead)* *Normal indication* Chassis Q7 Greater than 1 megohm Chassis Q8 Greater than 1 megohm	Remove transistor(s) as directed in paragraph 4-14*a* and check for faulty insulator. Install transistor and known good insulator on heat sink as directed in paragraph 4-14*b*. Repeat insulation checks before proceeding to *b* below.
	b. Using DMM, check resistance between heat sink assembly (chassis) and cathodes of diodes listed below. *(− lead)* *(+ lead)* *Normal indication* Chassis CR4 Greater than 1 megohm Chassis CR5 Greater than 1 megohm	Remove diodes or SCR's as directed in paragraph 4-14*d* and check for faulty insulators. Install item and known good insulators on heat sink as directed in paragraph 4-14*e*. Repeat insulation checks before proceeding to step 3.
3	Install jumper P4 in A1J12 and A1J13, jumper P5 in A1J15 and A1J16, and jumper P6 in A1J18 and A1J19.	
	SETUP PROCEDURES FOR DYNAMIC TESTS	
4	On breakout box, set switches as follows: AC POWER to OFF. MONITOR TEST −12V to ON. MONITOR TEST +12V to ON. MONITOR TEST −4.4V to ON. +5V CROWBAR TEST to OFF. 45MA TEST LOAD to MIN. VOLTAGE TEST +5V to MIN. VOLTAGE TEST −4.4V to MIN. VOLTAGE TEST +12V to MIN. VOLTAGE TEST −12V to MIN.	
	CAUTION When performing step 5, the ground wire in test equipment power cords must be isolated from power source ground. Otherwise, the power supply under test and the test equipment may be damaged when performing the following steps in this table. Ensure that power supply under test and test equipment cases do not come in contact with anything such as work benches or test equipment stands that are connected to ground potential.	
5	Connect test equipment as shown in figure 4-6.	
6	Set AC POWER switch to ON. AC POWER ON and MONITOR TEST DC POWER indicators are lit.	When MONITOR TEST DC POWER indicator does not light and AC POWER ON indicator lights, perform the troubleshooting procedures in table 4-6 to determine fault before performing the procedures in this table.

Table 4-7. Cable Power Supply Circuits Troubleshooting Procedures—Continued

Step	Procedure/normal indication	If indication is abnormal
	45 MA CABLE CURRENT REGULATION CIRCUITS CHECKS	
7	**WARNING** When jumper P7 is removed from power supply and 45MA TEST LOAD switch is set to CROWBAR position, up to 300 volts dc is present at +4.500V and RTN TEST POINTS. DEATH or serious injury may occur upon contact with noninsulated probes in these test points. Set AC POWER switch to OFF and then remove jumper P7 from A1J21 and A1J22. Set AC POWER switch to ON.	
8	**NOTE** Proceed to step 19 when normal indication is obtained in step 8. Rotate 45MA TEST LOAD switch to MIN, NOM, and MAX. At each position, DMM indicates between −2.3 and −2.7 volts. In MIN position only, observe that 20 kHz voltage spikes are less than 1.0 volt peak-to-peak and ripple voltage is less than 50 millivolts peak-to-peak (fig. 4-5, F).	*a.* When DMM indication is out of tolerance: (1) Move DMM lead from −2.529V to +4.500V TEST POINTS and set 45MA TEST LOAD switch to ADJ. Adjust A1R72 for +4.5 ±0.01 volts on DMM. When adjustment cannot be performed, proceed to step 9. (2) Move DMM lead from +4.500V to −2.529V TEST POINTS and repeat this step. When normal indications are not obtained, check value of A1R80. If A1R80 is not faulty, proceed to step 9. *b.* When ripple voltage or voltage spikes are excessive, check A1CR32 thru A1CR35, A1CR38, A1C27, and A1C31.
9	Connect DMM leads across A1C27. DMM indicates +375 ± 25 volts. (Ensure that four VOLTAGE TEST switches are set to MIN.)	*a.* Check A1L4, A1L5, and A1C27. *b.* Check A1CR32 through A1CR35. *c.* Check secondary of T2.
10	Remove Q7 and Q8 from heat sink assembly and perform resistance checks as directed in paragraph 4-14*a* and *c*.	
11	Remove jumper P4 from A1J12 and A1J13, jumper P5 from A1J15 and A1J16, and jumper P6 from A1J18 and A1J19. Install connector P3 from breakout box in A1J15 and P4 in A1J18.	
12	Connect DMM leads to −2.529V and RTN TEST POINTS. Rotate RGLTR control for indication of −2.529 volts on DMM.	*a.* When normal indication is obtained, check A1U7 and associated components. *b.* When normal indication is not obtained, proceed to step 13.
13	Remove connectors P3 and P4 from A1J15 and A1J18. Using DMM, measure resistance between A1E41 and A1J15. DMM should indicate between 120 and 250 ohms.	Check A1R71 and A1R72.
14	Using DMM, measure resistance between A1E41 and A1J18. DMM should indicate between 90 and 110 ohms.	Check A1R79 and A1R80.
15	Install Q7 and Q8 on heat sink. Refer to paragraph 4-14*b*.	
16	Using DMM, check insulation resistance between Q7 case and heat sink. Check insulation resistance between Q8 case and heat sink. Observe that DMM indication is greater than 1 megohm for each check.	Remove transistor, check insulator, install transistor, and repeat this step.
17	Install jumper P4 in A1J12 and A1J13, jumper P5 in A1J15 and A1J16, and jumper P6 in A1J18 and A1J19.	
18	Connect DMM leads to +4.500V and RTN TEST POINTS. Set 45MA TEST LOAD switch to ADJ and observe that DMM indicates +4.5 ±0.01 volts. Then move DMM lead from +4.500V to −2.529V TEST POINTS. Rotate 45MA TEST LOAD switch to MIN, NOM, and MAX positions. Observe that DMM indicates between −2.36 and −2.7 volts at each position.	When DMM indication is out of tolerance, set 45MA TEST LOAD switch to ADJ and connect DMM leads to +4.500V and RTN TEST POINTS. Adjust A1R72 for indication of +4.5 ± 0.01 volts on DMM. Repeat this step.
	45 MA CABLE CURRENT CROWBAR CIRCUIT CHECKS	
19	Connect DMM leads to A1TP12 (+) and A1E14 (−). DMM indicates 0.000 ± 0.005 volts.	Adjust A1R67 for normal indication. When normal indication is not obtained, check A1VR13 and associated components.
20	Move DMM lead from A1TP12 to A1CR36 anode. DMM indicates −10 ± 2.0 volts.	Check A1U5 and A1CR36.

Table 4-7. Cable Power Supply Circuits Troubleshooting Procedures—Continued

Step	Procedure/normal indication	If indication is abnormal
21	Move DMM lead from A1CR36 to A1CR37 anode. DMM indicates − 10 ± 2.0 volts.	Check A1U6 and A1CR37.
22	Install jumper P7 in A1J21 and A1J22.	
23	Set 45MA TEST LOAD switch to ADJ. Connect DMM leads to +4.500V and RTN TEST POINTS. DMM indicates +5 ± 0.5 volts.	Check Q6 and associated components.
24	Set 45MA TEST LOAD switch on CROWBAR and then back to ADJ. DMM indicates less than 1.0 volt.	Using DMM, check for +10 ± 2.0 volts between A1TP16 (+) and RTN TEST POINTS. If voltage is missing, check A1U5, A1U6, and associated components. If voltage is present, check Q6 and associated components.
	SHUTDOWN PROCEDURE	
25	Set AC POWER switch to OFF.	
26	Check that jumpers P1 through P7 are all installed as shown in figure 4-1. Shutdown procedure is complete.	
27	Disconnect test setup.	

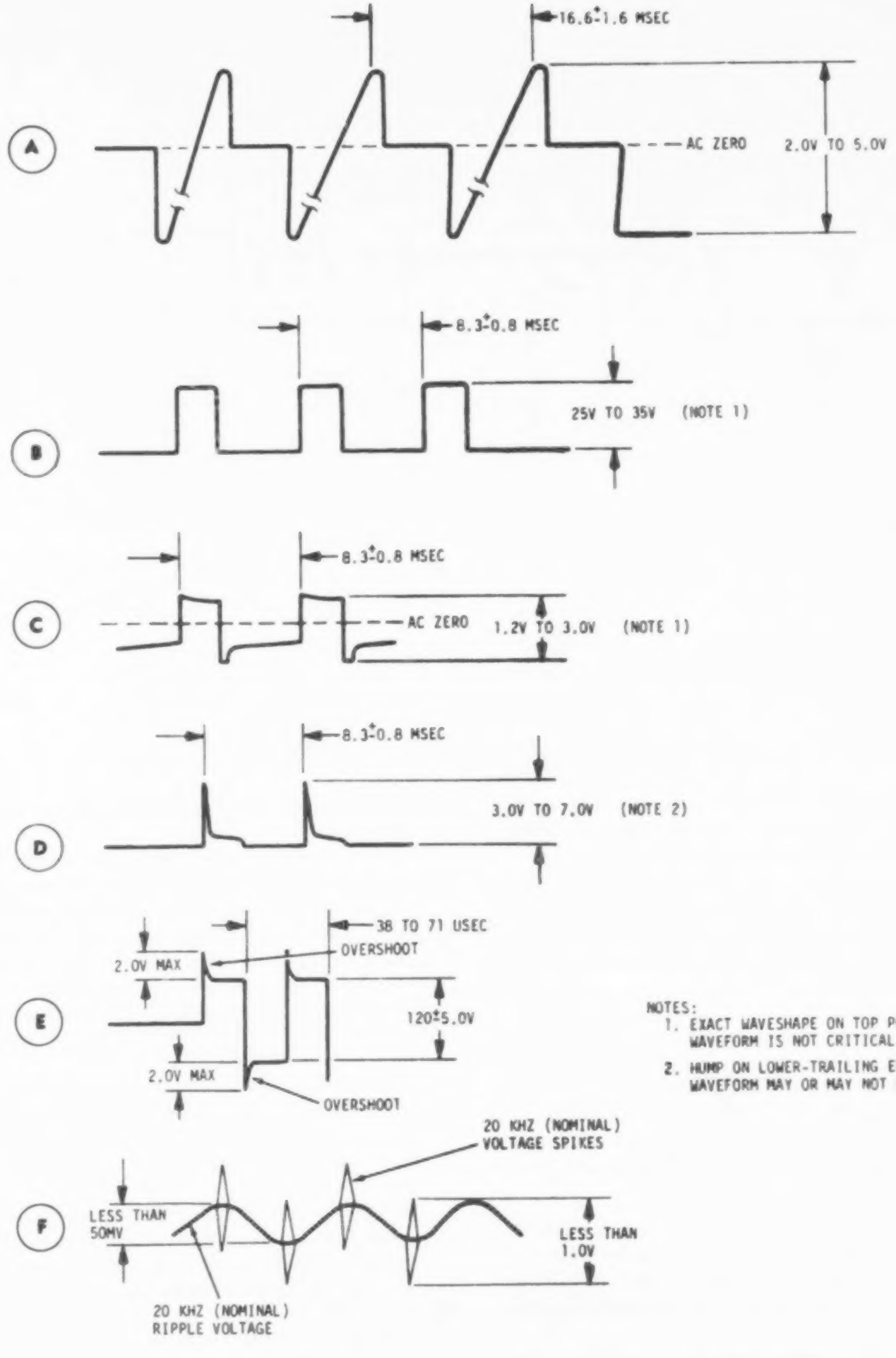

POWER SUPPLY
BREAKOUT BOX
70730040-009
P2
AC POWER
(115V 60 HZ)
POWER SUPPLY
DCR 80-10
+
-
(NOTE 2)
P1
P1
POWER SUPPLY
21A12
CIRCUIT
CARD
J8
E14
TP6
DMM
3490A
+
-
(NOTE 2)
PROBE
RETURN
OSCILLOSCOPE
OS-261/U
AC POWER
(115V 60 HZ)
(NOTE 1)

NOTES:

1. USE APPROPRIATE ADAPTER IN SERIES WITH AC POWER CORDS TO ISOLATE TEST EQUIPMENT GROUND WIRE FROM EXTERNAL AC NEUTRAL LINE (GROUND WIRE). CONNECT OSCILLOSCOPE, DMM, AND POWER SUPPLY DCR 80-10 TO 115V 60 HZ POWER SOURCE.
2. PHYSICALLY CONNECT DMM TEST LEADS TO J8 AND E14.
3. DO NOT APPLY DC POWER TO UNIT UNDER TEST UNTIL DIRECTED TO DO SO IN TEST PROCEDURES.

EL5NG146

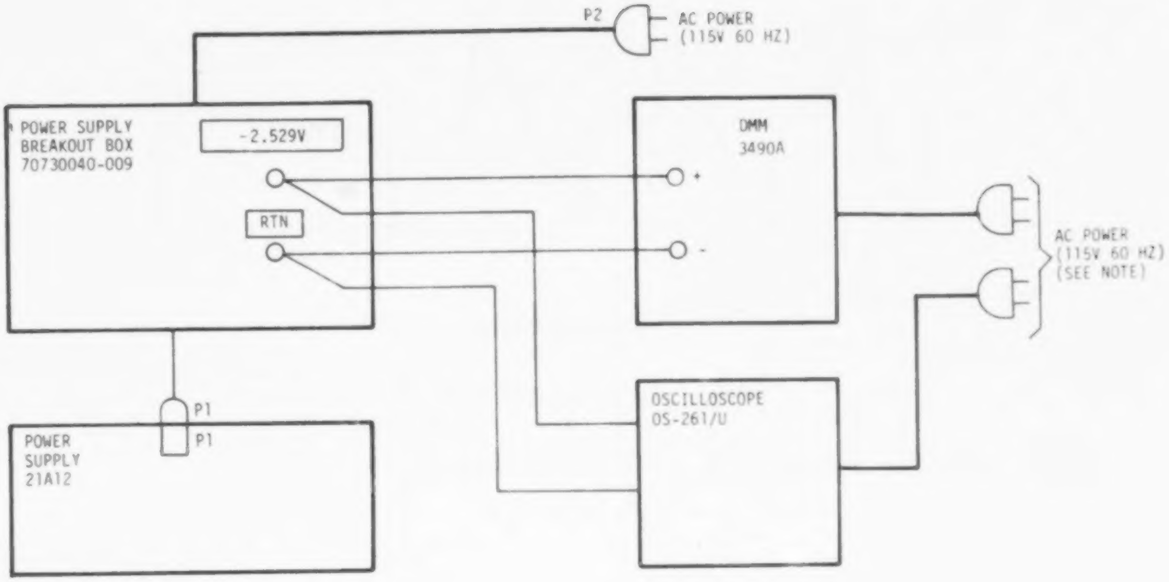
Figure 4-4. DC power supply circuits troubleshooting setup diagram.


16.6±1.6 MSEC
A
AC ZERO
2.0V TO 5.0V
8.3±0.8 MSEC
B
25V TO 35V (NOTE 1)
8.3±0.8 MSEC
C
AC ZERO
1.2V TO 3.0V (NOTE 1)
8.3±0.8 MSEC
D
3.0V TO 7.0V (NOTE 2)
38 TO 71 USEC
2.0V MAX
OVERSHOOT
E
120±5.0V
2.0V MAX
OVERSHOOT
20 KHZ (NOMINAL) VOLTAGE SPIKES
LESS THAN 50MV
F
LESS THAN 1.0V
20 KHZ (NOMINAL) RIPPLE VOLTAGE

NOTES:
1. EXACT WAVESHAPE ON TOP PORTION OF WAVEFORM IS NOT CRITICAL.
2. HUMP ON LOWER-TRAILING EDGE OF WAVEFORM MAY OR MAY NOT BE PRESENT.

EL5NG148

Figure 4-5. Power supply typical waveforms diagram.



NOTE:
USE APPROPRIATE ADAPTER IN SERIES WITH AC POWER CORDS TO ISOLATE TEST EQUIPMENT GROUND WIRE FROM EXTERNAL AC NEUTRAL LINE (GROUND WIRE). CONNECT DMM AND OSCILLOSCOPE TO 115V 60 HZ POWER SOURCE.

EL5NG149

Figure 4-6. Cable power supply circuits troubleshooting setup diagram.

4-14. Heat Sink Transistor, Diode, and SCR Removal, Installation, and Check Procedures

This paragraph contains the procedures for removing and installing the transistors, diodes, and SCR's mounted on the heat sink. These procedures will be performed when directed in the troubleshooting procedures in tables 4-6 and 4-7. The transistor removal procedures are in *a* below and the transistor installation procedures are in *b* below. Each time a transistor is removed, it must be checked (*c* below) to determine if it is faulty. Typical diode and SCR removal and installation procedures are described in *d* and *e* below.

a. Removal Procedures. Perform the following procedures to remove a transistor (Q3 through Q8) from heat sink.

(1) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(2) Remove two sets of screws and lockwashers (fig. 4-7, items 1 and 2) securing transistor to heat sink.

(3) Carefully remove transistor and insulator (fig. 4-7, items 3 and 4) from heat sink. Mark transistor to ensure that it is installed in same location during installation procedures.

(4) Check transistor as directed in *c* below. When transistor is faulty, refer to schematic diagram, figure FO-14, and check components and wiring associated with faulty transistor to determine cause of failure.

b. Installation Procedures. Perform the following procedures to install a transistor on heat sink.

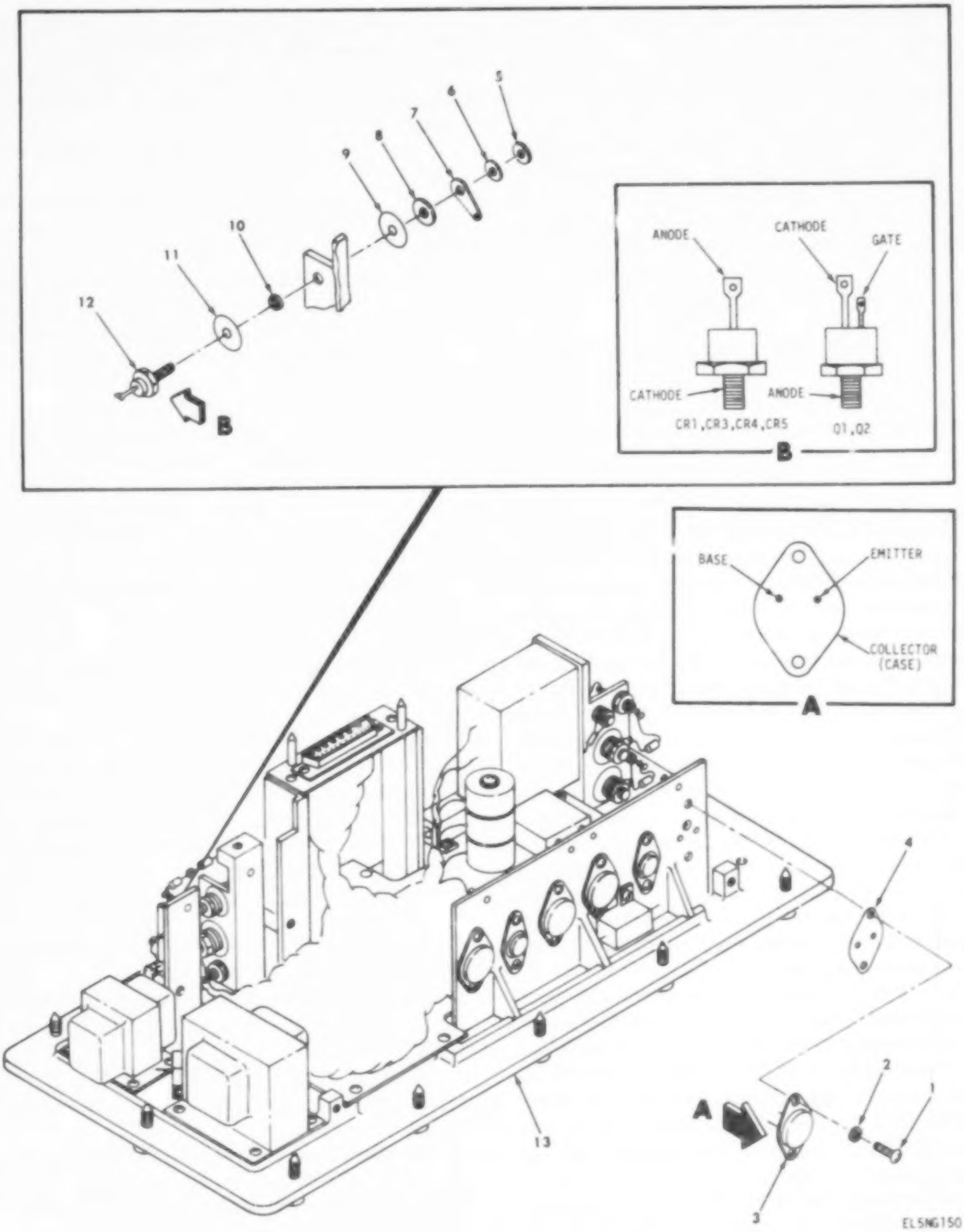
(1) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

CAUTION

> Faulty circuit operation may occur when insulator is not properly coated with thermal compound. Thermal compound is required for proper heat dissipation when power supply is energized.

(2) Check insulator (fig. 4-7, item 4) for damage and ensure that there is a thin and continuous coating of thermal compound on both sides of insulator. Thermal compound must meet the requirements of MIL-C-47009.

(3) Carefully install insulator and transistor (fig. 4-7, items 4 and 3) on heat sink, using two sets of screws and washers removed in *a*(2) above.


5
6
7
8
9
10
11
12
B
ANODE
CATHODE
GATE
CATHODE
ANODE
CR1,CR3,CR4,CR5
Q1,Q2
B
BASE
EMITTER
COLLECTOR
(CASE)
A
4
13
A
2
1
3
EL5NG150

1 Screw (2)
2 Lockwasher (2)
3 Transistor
4 Insulator
5 Nut
6 Lockwasher
7 Terminal lug
8 Washer
9 Insulator washer
10 Insulator disk
11 Insulator washer
12 Diode CR3
13 Heat sink

Figure 4-7. Typical heat sink transistor, diode, and SCR installation and removal diagram.

(4) Connect (−) lead of DMM to heat sink. Measure resistance between transistor case and heat sink to ensure that insulator is properly installed and is not faulty. Indication on DMM should be greater than 1 megohm.

c. Heat Sink Transistor Checks. The transistor checks consist of measuring the forward and back resistances between the base-to-collector, base-to-emitter, and collector-to-emitter leads on Q3 through Q8. The use of specific resistance values is not used for checks. In some applications, the resistance value measured between two leads of a given transistor will vary when different meters are used to measure the same points. In turn, the resistance values measured between two transistor leads can vary when the different resistance scales on one type of meter measure the same two leads. It is practical to use the resistance measurements to develop forward-to-back resistance ratios to determine that a transistor is good or faulty as described in (1) and (2) below.

(1) Transistors Q3 through Q8 have forward-to-back resistance ratios that are greater than 10 to 1 between the base-to-collector and base-to-emitter leads. A low resistance value is obtained when the meter voltage applied through the test leads forward biases the base to draw current through the base and the associated collector or emitter being checked. In turn, when the leads are reversed and the meter voltage applied through the test leads reverse biases the base to the off state, a high resistance value is measured between the base and the associated collector or emitter being checked. In a good transistor, the collector-to-emitter and emitter-to-collector checks will both be relatively high resistances since the two elements maintain an open circuit condition when the base lead is open. Table 4-8 shows the test connections to the transistor leads, bias condition, and the expected high or low resistance indication.

(2) In a faulty transistor, the base-to-emitter and base-to-collector forward and back resistance measurements can both be low (shorted condition) or both can be high (open circuit condition) resistance values. In turn, the normally high resistance between the collector and emitter becomes a low resistance when the two elements are shorted together. A typical short in one of the transistors is less than 5 ohms.

d. Typical Diode and SCR Removal Procedures. Diodes CR1, CR3, CR4, and CR5 and SCR's Q1 and Q2 are secured to the heat sink by mounting hardware. As a typical example, CR3 and its attaching hardware are shown in an exploded configuration in figure 4-7. A typical disassembly procedure, using CR3, is described in the following steps. With minor attaching hardware differences, this basic procedure can be followed to remove any of the other diodes or SCR's mounted on the heat sink.

(1) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(2) Remove nut (figure 4-7, item 5), lockwasher (6), terminal lug (7), and washer (8) from mounting lug of CR3 (12).

(3) Carefully remove insulator washer (9) from CR3.

(4) Carefully remove CR3 from heat sink and then remove insulator disk (10) and insulator washer (11) from CR3.

(5) Using DMM, measure forward and back resistance of diode. With + lead of DMM connected to anode, the resistance measured should be less than the resistance measured with + lead of DMM connected to cathode of CR3.

NOTE

SCR Q1 or Q2 can be checked by connecting − lead of DMM to cathode and + lead to anode. Then jumper + lead to SCR gate to turn on SCR. Observe resistance indication on DMM drops when SCR is turned on.

e. Typical Diode and SCR Installation Procedures. A typical installation procedure, using CR3, is described in the following steps. With minor hardware differences, this basic procedure can be followed to install any of the other diodes or SCR's mounted on the heat sink.

(1) On breakout box, set AC POWER switch to OFF. Observe that AC POWER ON indicator is out.

(2) Inspect insulator washers (fig. 4-7, items 9 and 11) and insulator disk (10) for damage. Ensure that insulator washer (11) has a thin and continuous coating of thermal compound on both sides of washer. Thermal compound must meet the requirements of MIL-C-47009.

(3) Install insulator washer (11) on CR3 (12). Then install insulator disk (10) on CR3.

(4) Carefully position CR3 to heat sink so that insulator disk is not jammed or damaged while positioning disk in hole in heat sink.

(5) Ensure that insulator disk (10) is properly positioned within heat sink and then mount insulator washer (9) on CR3.

(6) Place washer (8) on CR3 and then lightly press the anode of CR3 and washer (8) against heat sink. This results in positioning insulator washers (11) and (9) against heat sink.

(7) Install terminal lug (7), lockwasher (6), and nut (5) on CR3. Carefully tighten nut until CR3 and attaching hardware are secured to heat sink. Do not over-tighten nut to extent that washer (8) or CR3 cuts into insulator washers.

(8) Remove any access thermal compound squeezed out of hardware.

(9) Using DMM, measure resistance between cath-

ode of diode or anode of SCR and heat sink. DMM should indicate a resistance that is greater than 50K ohms for CR4 or CR5. DMM should indicate a resistance that is greater than one megohm for CR1, CR3, Q1, or Q2.

(10) Ensure that any external electrical component leads or wiring connected to the diode or SCR are properly connected.

4-15. Power Supply Wire Run List

The point-to-point wire runs between the components in the power supply are listed in table 4-9. The wire run list contains double-ended wiring entries so that each wire termination appears in the "From" column. This means that the user can select any terminal or pin location in the power supply and find that specific location in the "From" column in table 4-9. All the entries in the "From" column are listed in alphanumerical sequence.

Table 4-8. Heat Sink Transistor Resistance Checks

Transistor	Meter Leads		Condition	Resistance	
	(+)	(−)		Low	High
Q3 through Q8	Base	Collector	Forward biased	X	-
	Collector	Base	Reverse biased	-	X
	Base	Emitter	Forward biased	X	-
	Emitter	Base	Reverse biased	-	X
	Emitter	Collector	Open circuit	-	X
	Collector	Emitter	Open circuit	-	X

Section V. MAINTENANCE OF POWER SUPPLY

14-16. Introduction

This section contains the repair procedures for the power supply. The procedures are divided into the chassis repair (*a* below) and the electrical component and wiring repair procedures (*b* below).

a. Chassis Repair. The chassis repair procedures consist of replacing a damaged cover, tightening or replacing handle as necessary, and replacing one or more damaged locking inserts in the heat sink assembly. These procedures are in paragraph 4-18.

b. Electrical Component and Wiring Repair. Repair of the electrical components consists of replacing individual components on the heat sink or on the circuit card mounted on the heat sink, replacement of the circuit card, and repair of the wiring in the power supply. These procedures are in paragraph 4-19.

4-17. Tools Required for Power Supply Maintenance

The tools required for the repair of the power supply are listed in table 4-10. There are no requirements for test equipment in the following repair procedures.

4-18. Chassis Repair

a. General. The instructions for tightening or replacing the handle on the heat sink assembly are in *b* below. Subparagraph *c* below contains the repair procedures for replacing a faulty heat sink assembly locking insert. There are no special instructions required in the replacement of a damaged cover for the power supply.

b. Handle Maintenance. The power supply must be partially disassembled to reach the two self-locking nuts involved in the replacement of a handle or when tightening the handle.

(1) Remove cover from heat sink assembly, and then remove attaching hardware securing circuit card to heat sink assembly (para 4-20*b*).

(2) Lift circuit card to gain access to two self-locking nuts (fig 4-8, item 1).

(3) When handle is loose, tighten two self-locking nuts until handle is tight and then proceed to (7) below. When handle is damaged, remove two nuts and proceed to (4) below.

(4) Remove damaged handle from heat sink assembly.

(5) Install two flat washers AN9600XC616 and two packings NAS1523-6B on replacement handle SM-A-942148 as shown in figure 4-8 (items 2, 3, and 4).

(6) Insert handle (in folded position) in heat sink assembly and then secure handle in place, using two self-locking nuts MS21042-6. (Handle must set in indented area when in folded position.)

(7) Secure circuit card to heat sink assembly and then install cover on heat sink assembly as directed in paragraph 4-20*c*.

c. Locking Insert Repair. There are five types of replaceable locking inserts in the heat sink. There are 2 MS21209C0215, 25 MS21209C0415, 4 MS21209C0820, 1 MS21209F1-15, and 1 MS21209F1-20 locking inserts in the unit. To replace one of these locking inserts, perform the procedures in paragraph 3-35c. Locking insert sizes and tools required for each locking insert size are listed in (1) through (4) below:

(1) Locking insert MS21209C0215 (insert is 0.129 inch long with 0.86-56 UNC internal thread size; 2-56).

Table 4-9. Power Supply Wire Run List

From	To
A1E1	Q1 GATE
A1E2	Q2 GATE
A1E3	Q1 ANODE
A1E3	P1-A1
A1E4	Q2 ANODE
A1E4	P1-A2
A1E5	XQ3 COLL
A1E6	XQ3 BASE
A1E7	XQ4 EMTR
A1E8	XQ5 COLL
A1E8	T2-1
A1E9	XQ5 BASE
A1E10	XQ5 EMTR
A1E10	C1 NEG
A1E11	XQ6 BASE
A1E12	XQ6 COLL
A1E12	T2-3
A1E13	T1-5
A1E14	T1-4
A1E15	T1-3
A1E17	P1-9
A1E18	P1-7
A1E19	P1-17
A1E20	P1-15
A1E21	T2-9
A1E22	T2-11
A1E23	T2-4
A1E24	T2-5
A1E25	T2-6
A1E26	T2-7
A1E27	T2-8
A1E28	T2-2
A1E29	R3-1
A1E30	XQ8 BASE
A1E31	XQ8 EMTR
A1E32	XQ7 COLL
A1E33	P1-A7
A1E33	L2-1
A1E33	P1-10
A1E34	P1-A6
A1E34	T2-10
A1E35	P1-3
A1E35	P1-13
A1E36	P1-14
A1E37	P1-A3
A1E37	P1-8
A1E38	P1-A5
A1E39	P1-A4
A1E39	P1-16
A1E40	P1-6
A1E40	R4-2
A1E41	P1-4
A1E42	P1-1
A1E43	R7-1
A1E44	R7-2
C1 NEG	L1-1
C1 NEG	A1E10
C1 POS	Q1 CATH
C1 POS	CR2-2
C1 POS	XQ4 COLL
C2-1	Q1 GATE
C2-2	Q1 CATH
C3-1	Q2 CATH
C3-2	Q2 GATE
C4-1	R5-2[1]
C4-2	CR4 ANODE
C5-1	R6-2[1]
C5-2	CR5 ANODE
C6-1	R8-1[1]
C6-2	Q1 ANODE
C7-1	R9-1[1]
C7-2	Q2 ANODE
CR1 ANODE	CR3 ANODE
CR1 ANODE	CR2-1
CR1 CATH	Q1 ANODE
CR1 CATH	T1-2
CR2-1	CR1 ANODE
CR2-2	Q2 CATH
CR2-2	C1 POS
CR3 ANODE	CR1 ANODE
CR3 ANODE	L1-2
CR3 CATH	T1-1
CR3 CATH	Q2 ANODE
CR4 ANODE	T2-9
CR4 ANODE	C4-2
CR4 CATH	L2-2
CR4 CATH	R5-1
CR5 ANODE	T2-11
CR5 ANODE	C5-2
CR5 CATH	L2-2
CR5 CATH	R6-1
E1	P1-2
L1-1	C1 NEG
L1-2	CR3 ANODE
L2-1	A1E33
L2-2	CR4 CATH
L2-2	CR5 CATH
P1-1	A1E42
P1-2	E1
P1-3	A1E35
P1-4	A1E41
P1-6	A1E40
P1-7	A1E18
P1-8	A1E37
P1-9	A1E17
P1-10	A1E33
P1-13	A1E35
P1-14	A1E36
P1-15	A1E20
P1-16	A1E39
P1-17	A1E19
P1-A1	A1E3
P1-A2	A1E4
P1-A3	A1E37
P1-A4	A1E39
P1-A5	A1E38
P1-A6	A1E34
P1-A7	A1E33
Q1 ANODE	A1E3
Q1 ANODE	CR1 CATH
Q1 ANODE	C6-2
Q1 CATH	C1 POS
Q1 CATH	C2-2
Q1 CATH	R8-2
Q1 GATE	A1E1
Q1 GATE	C2-1
Q2 ANODE	A1E4
Q2 ANODE	C7-2
Q2 ANODE	CR3 CATH
Q2 CATH	C3-1
Q2 CATH	CR2-2
Q2 CATH	R9-2
Q2 GATE	A1E2
Q2 GATE	C3-2
R1-1	R2-2
R1-1	XQ7 BASE
R1-2	XQ7 COLL
R2-1	XQ8 EMTR
R2-2	R1-1
R3-1	A1E29
R3-2	R4-1
R4-1	R3-2
R4-2	A1E40
R5-1	CR4 CATH
R5-2	C4-1[1]
R6-1	CR5 CATH
R6-2	C5-1[1]
R7-1	A1E43
R7-2	A1E44
R8-1	C6-1[1]
R8-2	Q1 CATH
R9-1	C7-1[1]
R9-2	Q2 CATH
T1-1	CR3 CATH
T1-2	CR1 CATH
T1-3	A1E15
T1-4	A1E14
T1-5	A1E13
T2-1	A1E8
T2-2	A1E28
T2-3	A1E12
T2-4	A1E23
T2-5	A1E24
T2-6	A1E25
T2-7	A1E26
T2-8	A1E27
T2-9	A1E21
T2-9	CR4 ANODE
T2-10	A1E34
T2-11	A1E22
T2-11	CR5 ANODE
XQ3 BASE	A1E6
XQ3 COLL	XQ4 COLL
XQ3 COLL	A1E5
XQ3 EMTR	XQ4 BASE
XQ4 BASE	XQ3 EMTR
XQ4 COLL	C1 POS
XQ4 COLL	XQ3 COLL
XQ4 EMTR	A1E7
XQ5 BASE	A1E9
XQ5 COLL	A1E8
XQ5 EMTR	A1E10
XQ5 EMTR	XQ6 EMTR
XQ6 BASE	A1E11
XQ6 COLL	A1E12
XQ6 EMTR	XQ5 EMTR
XQ7 BASE	R1-1
XQ7 COLL	A1E32
XQ7 COLL	R1-2
XQ7 EMTR	XQ8 COLL
XQ8 BASE	A1E30
XQ8 COLL	XQ7 EMTR
XQ8 EMTR	A1E31
XQ8 EMTR	R2-1

[1] VIA FEEDTHRU TERMINAL

Tool	*Part No.*
Extraction tool	Heli-Coil 1227-02
Insertion tool	Heli-Coil 551-02
Tang breakoff tool	Heli-Coil 3695-02

(2) Locking insert MS21209C0415 (insert is 0.168 inch long with 0.112-40 UNC internal thread size; 4-40).

Tool	*Part No.*
Extraction tool	Heli-Coil 1227-06
Insertion tool	Heli-Coil 7551-04
Tang breakoff tool	Heli-Coil 3695-04

(3) Locking insert MS21209C0820 (insert is 0.328 inch long with 0.164-32 UNC internal thread size; 8-32).

Tool	*Part No.*
Extraction tool	Heli-Coil 1227-06
Insertion tool	Heli-Coil 7551-2
Tang breakoff tool	Heli-Coil 3695-2

(4) Locking insert MS21209F1-15 (insert is 0.285 inch long with 0.19-32 UNF internal thread size; 10-32). Locking insert MS21209F1-20 (insert is 0.38 inch long with 0.19-32 UNF internal thread size; 10-32).

Tool	*Part No.*
Extraction tool	Heli-Coil 1227-6
Insertion tool	Heli-Coil 7552-3
Tang breakoff tool	Heli-Coil 3695-3

Table 4-10. Tools Required for Power Supply Repair

Tool	Qty	NSN or part No.
Bench top repair center.	1	3439-00-445-5965
Locking insert tools consisting of:		
Extraction tool	1	5120-00-138-6803
Extraction tool	1	5120-00-245-9539
Extraction tool	1	5120-00-723-6833
Insertion tool	1	551-02 (Heli-Coil)
Insertion tool	1	5120-00-816-5703
Insertion tool	1	5120-00-237-4669
Insertion tool	1	5120-00-797-2404
Tang breakoff tool	1	5120-00-410-9156
Tang breakoff tool	1	5120-00-793-1073
Tang breakoff tool	1	5120-00-776-9519
Tang breakoff tool	1	5120-00-793-1076
Connector repair tool kit.	1	70730090-009 (Martin Marietta)
Electronic equipment tool kit TK-105/G.	1	5180-00-610-8177

4-19. Electrical Component Repair

a. General. This paragraph contains the procedures for replacing contacts in connector P1 (*b* below), replacing components on the circuit card (*c* below), and replacing the circuit card (*d* below). There are no special procedures required for removing and installing an electrical component mounted on the heat sink assembly. All the heat sink-mounted components are accessible when the cover is removed from the heat sink assembly.

b. Connector P1 Repair. Connector P1 contains seven replaceable contacts (A1 through A7). Perform the procedures in paragraph 3-44*b* (like connectors P2 and J3 on front panel) to replace one or more of contacts SM-B-942072-2 in connector P1.

c. Circuit Card Component Repair. To replace a component on the circuit card, the hardware securing the circuit card to the heat sink must be removed. When the hardware is removed, the circuit card can be lifted and tilted sufficiently to gain access to both sides of the card without unsoldering the wiring to the card. Perform the following procedures to replace a component on the circuit card.

(1) Remove cover from heat sink and then remove screws and washers securing circuit card to heat sink as directed in paragraph 4-20*b*.

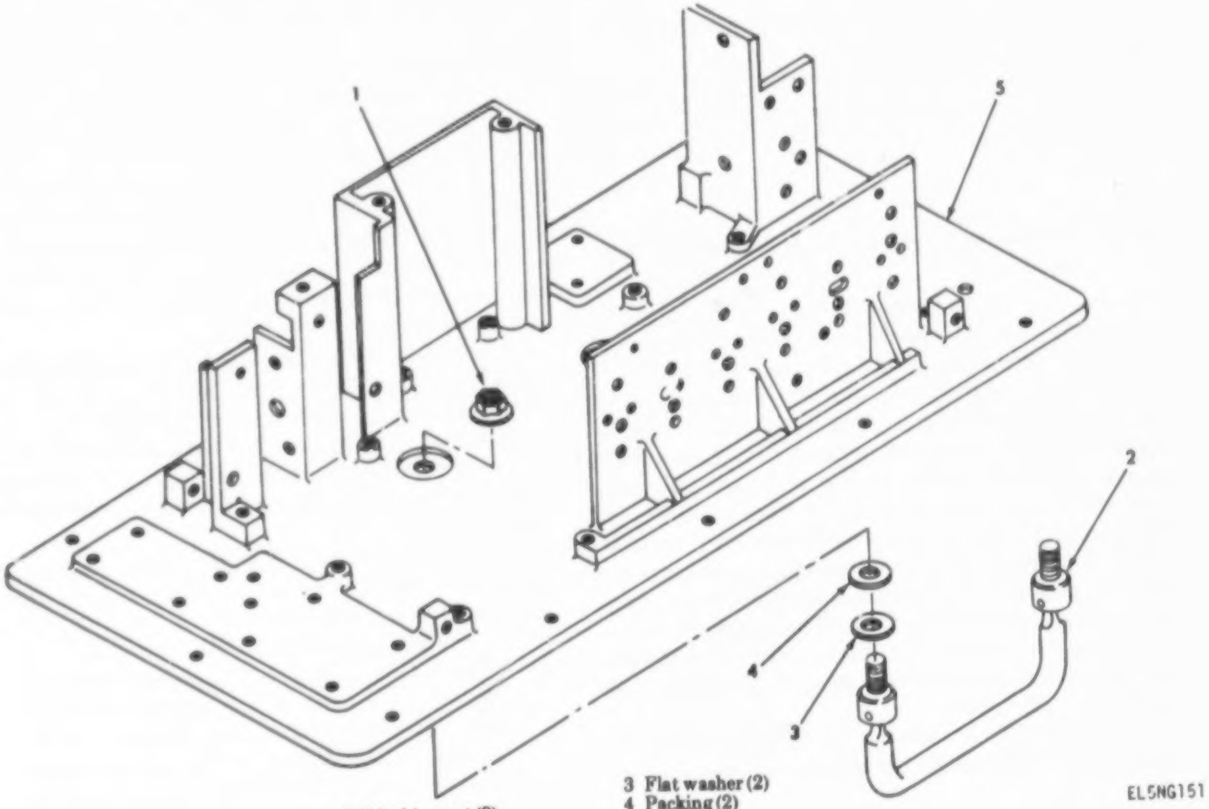
(2) There are no special procedures required to unsolder and solder components on the circuit card. Use the circuit card repair procedures as directed in paragraph 3-46 and *(a)* and *(b)* below when replacing a faulty component on the circuit card.

(a) The following resistors are high temperature components. When replacing any of these resistors, position body of resistor at least 0.06 inch above surface of printed circuit card.

R7
R8
R12
R14
R18
R22
R44
R48
R60
R61
R71
R79

(b) Do not apply conformal coating to the following items on the circuit card.

E1-E15
E17-E44
J1-J22
TP1-TP6
Adjustment screws of R34, R67, and R72



1 Self-locking nut (2)
2 Handle
3 Flat washer (2)
4 Packing (2)
5 Heat sink

Figure 4-8. Handle mounting diagram.

(3) Secure the circuit card and cover to heat sink as directed in paragraph 4-20*c*.

(4) Perform test procedures in table 4-4 to ensure that power supply is repaired and ready to be returned to the user or stock.

d. Circuit Card Replacement. Perform the following procedures to replace the circuit card in the power supply.

(1) Remove cover from heat sink and then remove screws and washers securing circuit card to heat sink as directed in paragraph 4-20*b*.

(2) Unsolder each wire connected to terminals on circuit card. Tag each wire with its corresponding terminal number to ensure that wire will be reconnected to the correct terminal on replacement card.

(3) After all wires to circuit card are unsoldered from terminals, lift card from heat sink. Position replacement card on heat sink.

(4) Ensure that terminals on replacement card are clean and dry. Solder each wire removed in (2) above to its associated terminal on card.

(5) After all wires are installed, remove all solder splashes and loose wire ends from power supply. Ensure that wires are positioned so they are not pinched when card is attached to heat sink in (6) below.

(6) Secure circuit card and cover to heat sink as directed in paragraph 4-20*c*.

(7) Perform test procedures in table 4-4 to ensure that power supply is repaired and ready to be returned to the user or stock.

4-20. Disassembly and Assembly Procedures

a. General. The electrical components in the power supply are mounted directly on the heat sink or on the circuit card that is mounted on the heat sink. A protective cover is installed over the electrical components on the heat sink as shown in figure 4-9. There are no special tools or procedures required to replace a component mounted directly on the heat sink assembly. The circuit card must be partially disconnected from the heat sink before a faulty component on the circuit card can be replaced. The disassembly procedures for gaining access to card-mounted components are in *b* below. The procedures for assembling a repaired power supply are in *c* below. The disassembly and assembly procedures can be performed using the common tools in Tool Kit TK-105/G.

b. Disassembly Procedures. Perform the following procedures to disconnect the circuit card from the heat sink.

WARNING

Ensure that connector P1 on power supply is disconnected from power supply breakout box. Otherwise, dangerous voltages may be accidentally generated in the power supply that could cause DEATH or serious injury to personnel.

NOTE

The key numbers on figure 4-9 are shown in parentheses after the components called out in the following procedures to aid in locating the components.

(1) If installed, remove cover from heat sink by removing four sets of screws (1) and washers (2) and then lifting cover (3) from heat sink (4).

(2) Remove screw (5) and washer (6) from center of coils on circuit card.

(3) Remove four sets of screws (7) and washers (8 and 9) securing transformer T2 (10) to heat sink. Remove pad (11) under transformer and retain for use in assembly procedure.

(4) Remove three sets of screws (12) and washers (13) securing three loop clamps (14) to heat sink. Lift capacitor C1 (15) upwards and position it off end of heat sink.

(5) Remove two sets of screws (16) and washers (17) securing connector P1 (18) to heat sink. Lift connector P1 up and away from heat sink (over circuit card).

(6) Remove 11 sets of screws (19) and washers (20) securing circuit card (21) to heat sink.

(7) Remove two sets of screws (24) and washers (25) securing resistor R7 (26) to heat sink.

(8) Lift connector-side of circuit card upward. Service loops in wiring should allow circuit card to be lifted sufficiently to permit access to underside of circuit card. If there is insufficient work space under the circuit card to permit unsoldering of faulty components, perform (9) below.

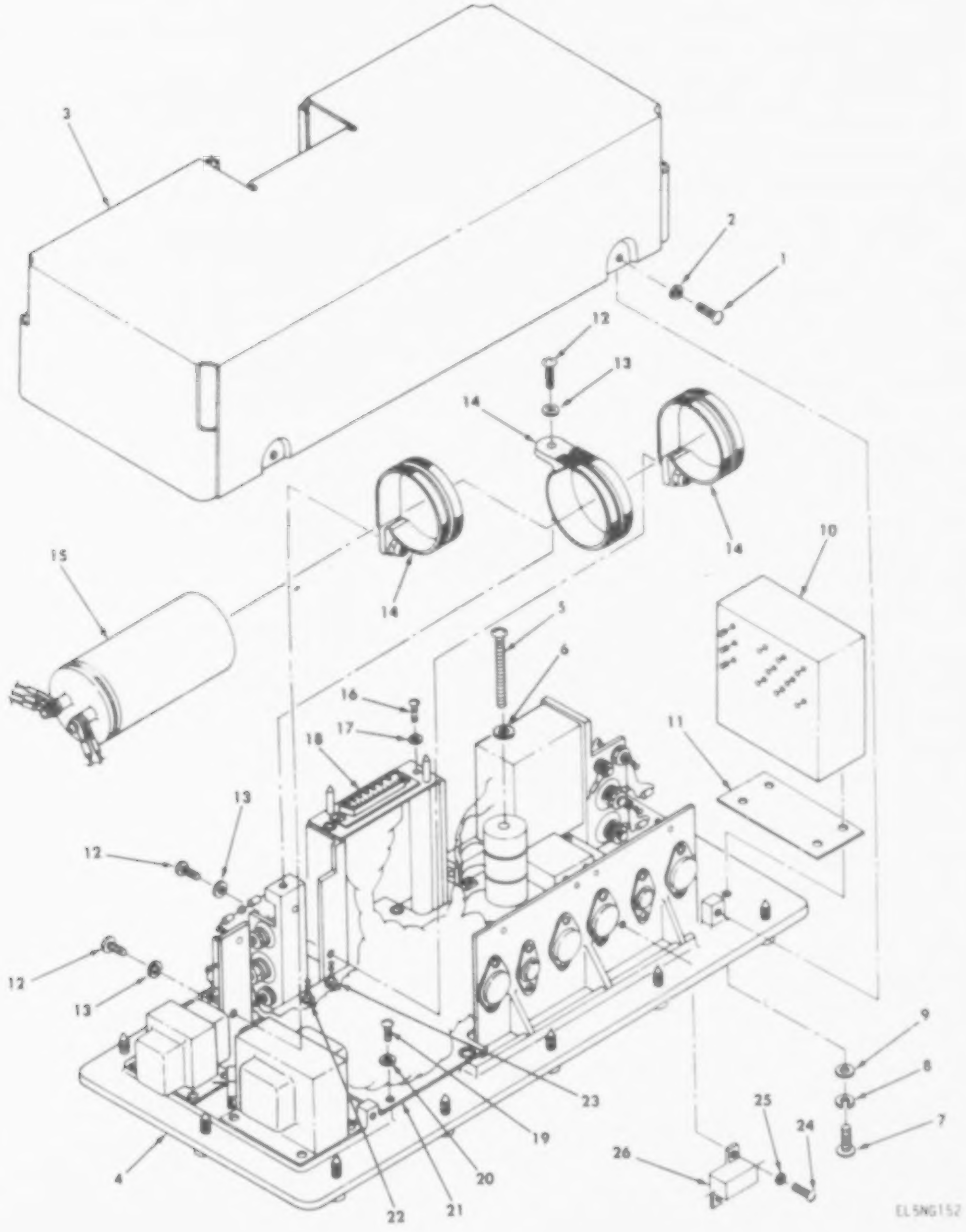
(9) Unsolder wire No. 3 from terminal E3 (22) and wire No. 5 from terminal E4 (23). Tag each wire with its respective terminal number to ensure that wires will be properly connected in the assembly procedures.

(10) Perform the appropriate repair procedures and then assemble repaired circuit card as directed in c below.

c. Assembly Procedures. Perform the following procedures to assemble a repaired power supply into the normal operating configuration.

WARNING

Ensure that connector P1 on power supply is disconnected from power supply breakout box. Otherwise, dangerous voltages may be accidentally generated in the power supply that could cause DEATH or serious injury to personnel. Ensure that AC POWER switch on breakout box is set to OFF before disconnecting P1.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EL5NG152

1 Screw (4)
2 Washer (4)
3 Cover
4 Heat sink
5 Screw
6 Washer
7 Screw (4)
8 Washer (4)
9 Washer (4)
10 Transformer T2
11 Pad
12 Screw (3)
13 Washer (3)
14 Loop clamp (3)
15 Capacitor C1
16 Screw (2)
17 Washer (2)
18 Connector P1
19 Screw (11)
20 Washer (11)
21 Circuit card
22 Terminal E3
23 Terminal E4
24 Screw (2)
25 Washer (2)
26 Resistor R7

Figure 4-9. Power supply disassembly diagram.

NOTE

The key numbers on figure 4-9 are shown in parentheses after the components called out in the following procedures to aid in locating the components.

(1) If not connected, solder wire No. 3 to terminal E3 (22) and wire No. 5 to terminal E4 (23).

(2) Inspect heat sink (4) and circuit card (21) for loose washers and screws and presence of solder splashes or other foreign material that could cause a short circuit or damage to components and wiring.

(3) Carefully align wiring and circuit card (21) on heat sink (4). Attach circuit card to heat sink, using 11 sets of screws (19) and washers (20). Ensure that wiring is not pinched between circuit card and heat sink.

(4) Install screw (5) and washer (6) through center of coils to heat sink.

(5) Secure connector P1 (18) to heat sink, using two sets of screws (16) and washers (17).

(6) Hold capacitor C1 (15) to heat sink and loosely secure center loop clamp (14) to heat sink, using screw (12) and washer (13).

CAUTION

Ensure that wiring is clear of securing screws and loop clamp when performing (7) below to prevent damaging wires when tightening clamps.

(7) Loosely secure other two loop clamps to heat sink assembly.

(8) Position capacitor C1 so that + and – terminals on C1 are parallel to heat sink and do not contact other components.

(9) Tighten screws and washers on three loop clamps to secure C1 in place.

(10) Install resistor R7 (26) to heat sink, using two sets of screws (24) and washers (25).

(11) Place pad (11) between transformer T2 (10) and heat sink. Secure transformer to heat sink, using four sets of screws (7) and washers (8 and 9).

(12) Ensure that wire terminations are secure and there are no loose components on power supply.

NOTE

When fault was detected during visual inspection (table 4-2), proceed to (13) below. When fault was detected during troubleshooting (table 4-6 or 4-7), proceed to (14) below.

(13) Secure cover (3) to heat sink (4), using four sets of screws (1) and washers (2). Perform procedures in table 4-4.

(14) Return to the appropriate troubleshooting table (4-6 or 4-7) in which the fault was detected and complete the remaining test procedures to ensure that there are no more faults in the power supply.

APPENDIX A

REFERENCES

DA PAM 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (Types 7, 8, and 9), Supply Bulletins, and Lubrication Order.
TM 11-5805-382-12	Operator's and Organizational Maintenance Manual: Multiplexers TD-660/G (NSN 5820-00-930-8079), TD-660A/G (NSN 5820-00-928-3382) and TD-660B/G (NSN 5820-00-928-3382).
TM 11-5805-382-35	Direct Support, General Support, and Depot Maintenance Manual: Multiplexers TD-660/G (NSN 5805-00-930-8079), TD-660A/G and TD-660B/G (NSN 5820-00-928-3382).
TM 11-5805-383-12	Operator's and Organizational Maintenance Manual: Multiplexer TD-754/G (NSN 5820-00-930-8078).
TM 11-5805-383-35	Direct Support, General Support, and Depot Maintenance Manual Including Repair Parts and Special Tool Lists: Multiplexer TD-754/G.
TM 11-5805-585-14-2	Operator's, Organizational, Direct Support, General Support and Depot Maintenance Manual : Terminal Set, Telephone AN/TCC-73(V)1 and AN/TCC-73(V)2 (NSN 5805-00-134-5404).
TM 11-5820-695-12	Operator's and Organizational Maintenance Manual (Including Repair Parts List and Special Tools Lists): Radio Set AN/GRC-144 (NSN 5820-00-926-7356).
TM 11-5820-695-35	Direct Support, General Support and Depot Maintenance Manual: Radio Set AN/GRC-144 (NSN 5820-00-926-7356).
TM 11-7025-202-12	Operator's and Organizational Maintenance Manual for Multiplexer TD-976/G (NSN 7025-01-048-9678) and Pulse Form Restorer TD-982/G (NSN 7025-01-061-1245).
TM 11-7025-202-20P	Organizational Maintenance Repair Parts and Special Tools Lists for Multiplexer TD-976/G (NSN 7025-00-048-9678) and Pulse Form Restorer TD-982/G (7025-00-061-1254).
TM 11-7025-202-34P	Direct Support and General Support Maintenance Repair Parts List and Special Tools List's (Including Depot Maintenance Repair Parts and Special Tools): Multiplexer TD-976/G (NSN 7025-01-048-9678) and Pulse Form Restorer TD-982/G (NSN 7025-00-061-1254).
TM 38-750	The Army Maintenance Management System (TAMMS).
TM 740-90-1	Administrative Storage of Equipment.
TM 750-244-2	Procedures for Destruction of Electronics Materiel To Prevent Enemy Use (Electronics Command).

GLOSSARY

Activity pattern—

A unique repetitive 7-bit pattern (1011000, last bit in time shown on left) generated within the TD-976/G. This pattern is automatically inserted into the SG in place of user data when a group is not active (on).

Asynchronous—

Signals or events that are not synchronous or not of a common period and phase (frequency) relationship one to another.

Bipolar—

Refers to TD-976/G SG format. Bipolar data format consists of alternate positive and negative ½-baud pulses for digital 1's and an ac zero level for digital 0's. Pulse amplitudes are positive or negative 0.9 ± 0.1 volt peak with reference to ac zero.

Channel—

Refers to one digitally encoded voice signal as contained within the multichannel output of a user equipment such as a TD-660/G. Within the TD-976/G, one channel represents a rate of 48 kbps.

Destuffing—

A rate adjustment function performed by the demultiplexer section in response to a stuffing function performed by far-end multiplexer section. Destuffing consists of deleting the group write clock associated with the data bit time during which the multiplexer section performed a stuffing operation. This action equalizes group output rate with initial group rate as applied to the far-end multiplexer input.

Dummy pattern—

A unique repetitive 7-bit pattern (0100111, last bit in time shown on left) generated by the TD-976/G. This dummy pattern is inserted into the SG in place of user data when an active user group input is missing.

Frame—

A grouping of 20 minor frames.

Group—

Data associated with a quantity of channels (usually 6 or 12) as exchanged between the TD-976/G and an interfacing user equipment on a single line.

Major frame—

Largest organized grouping within SG message format. A major frame is divided into frames, which, in turn, are divided into minor frames.

Minor frame—

Smallest organized grouping within SG message format. A minor frame consists of data bits and O/H bits arranged in a predetermined sequence.

NRZ—

Nonreturn to zero. Refers to a type of data format wherein the signal level does not return to zero for successive digital 1's.

Overhead (O/H)—

Data interleaved among group data within an SG for purposes of exchanging orderwire, synchronization, and status information between a multiplexer and a demultiplexer.

Stuffing—

A rate adjustment function performed by a multiplexer section. Results in an instantaneous 1-bit slowing of a group's read clock (deletion of a read clock) for purposes of equalizing read rate to group input rate.

Supergroup (SG)—

A serial data stream containing two or more time-division interleaved groups of user data. An SG also contains overhead bits.

Synchronous—

Signals or events occurring at the same time or having the same period and phase relationship.

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  - SHAD (3)
  - TOAD (14)
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  - Sig Sec USA Dep (1)
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NG: None
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For explanation of abbreviations used, see AR 310-50.

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PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of [illegible] knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		FO3		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. + 24 VDC is the input voltage.

SAMPLE

TYPED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER	SIGN HERE:
SSG I. M. DeSpiritof 999-1776	SSG. I.M. DeSpiritof.

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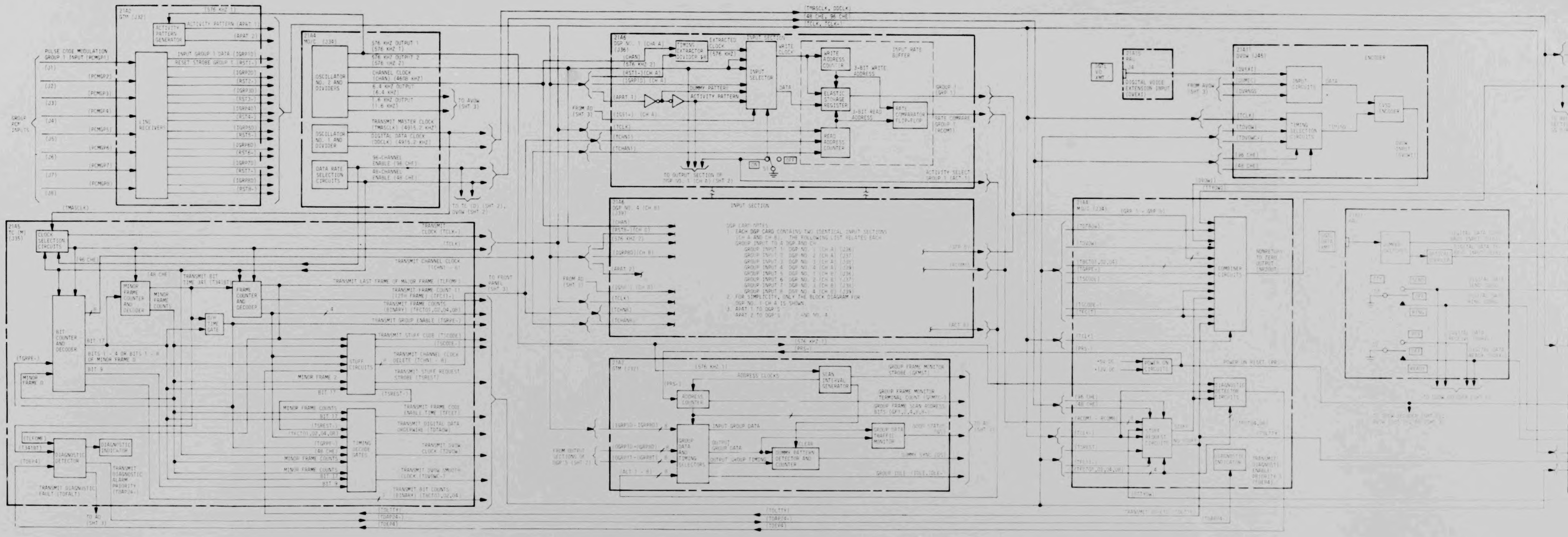
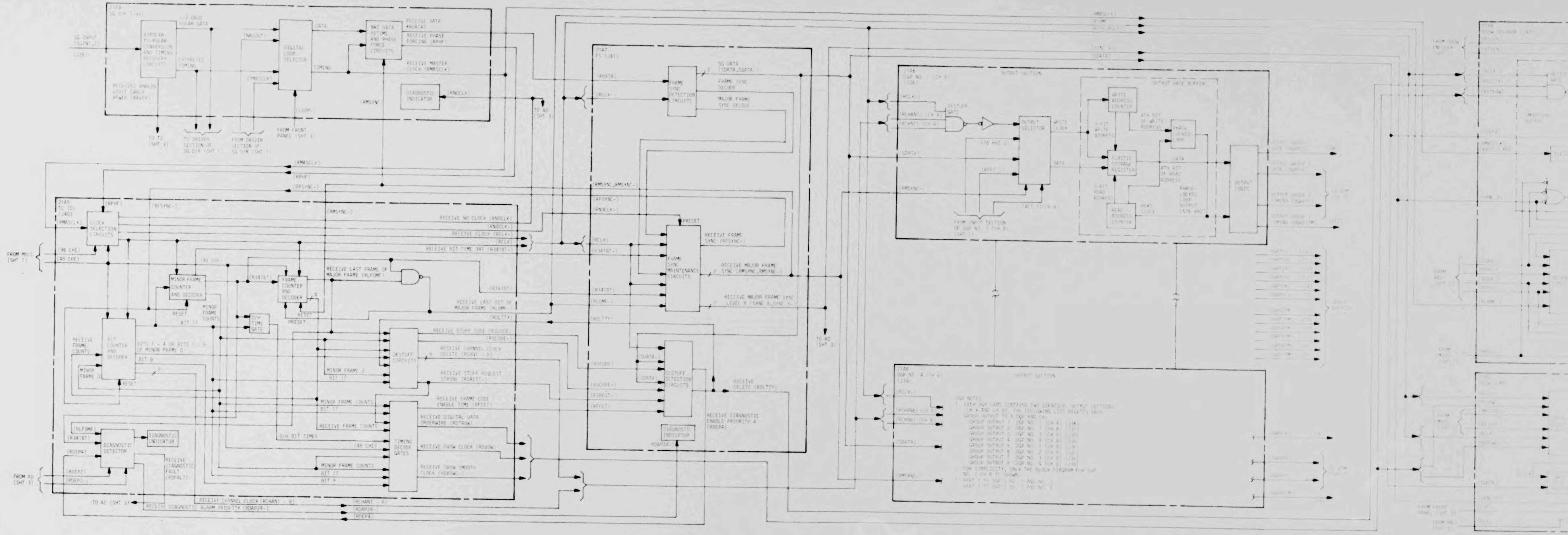

21A2
GTM (J32)
ACTIVITY PATTERN GENERATOR
(576 KHZ 1)
ACTIVITY PATTERN (APAT 1)
(APAT 2)
PULSE CODE MODULATION GROUP 1 INPUT (PCMGP1)
(J1)
(PCMGP2)
(J2)
(PCMGP3)
(J3)
(PCMGP4)
(J4)
(PCMGP5)
(J5)
(PCMGP6)
(J6)
(PCMGP7)
(J7)
(PCMGP8)
(J8)
GROUP PCM INPUTS
LINE RECEIVERS
INPUT GROUP 1 DATA (IGRP1D)
RESET STROBE GROUP 1 (RST1-)
(IGRP2D)
(RST2-)
(IGRP3D)
(RST3-)
(IGRP4D)
(RST4-)
(IGRP5D)
(RST5-)
(IGRP6D)
(RST6-)
(IGRP7D)
(RST7-)
(IGRP8D)
(RST8-)
21A4
MD/C (J34)
OSCILLATOR NO. 2 AND DIVIDERS
576 KHZ OUTPUT 1 (576 KHZ 1)
576 KHZ OUTPUT 2 (576 KHZ 2)
CHANNEL CLOCK (CHAN) (4608 KHZ)
6.4 KHZ OUTPUT (6.4 KHZ)
1.6 KHZ OUTPUT (1.6 KHZ)
TO AVOW (SHT 3)
OSCILLATOR NO. 1 AND DIVIDER
TRANSMIT MASTER CLOCK (TMASCLK) (4915.2 KHZ)
DIGITAL DATA CLOCK (DDCLK) (4915.2 KHZ)
DATA RATE SELECTION CIRCUITS
96-CHANNEL ENABLE (96 CHE)
48-CHANNEL ENABLE (48 CHE)
TO TC (D) (SHT 2), DVOW (SHT 2)
(TMASCLK)
21A5
TC (M)
(J35)
CLOCK SELECTION CIRCUITS
(96 CHE)
(48 CHE)
TRANSMIT CLOCK (TCLK-)
(TCLK)
TRANSMIT CHANNEL CLOCK (TCHN1 - 8)
MINOR FRAME COUNTER AND DECODER
MINOR FRAME COUNTS
TRANSMIT BIT TIME 341 (T341BT)
FRAME COUNTER AND DECODER
O/H TIME GATE
BIT COUNTER AND DECODER
BIT 17
BITS 1 - 4 OR BITS 1 - 8 OF MINOR FRAME 0
BIT 9
(TGRPE-)
MINOR FRAME 0
TRANSMIT LAST FRAME OF MAJOR FRAME (TLFOMF)
TRANSMIT FRAME COUNT 11 (12TH FRAME) (TFC11-)
TRANSMIT FRAME COUNTS (BINARY) (TFCT01,02,04,08)
TRANSMIT GROUP ENABLE (TGRPE-)
TO FRONT PANEL (SHT 3)
STUFF CIRCUITS
MINOR FRAME 2
BIT 17
TRANSMIT STUFF CODE (TSCODE)
(TSCODE-)
TRANSMIT CHANNEL CLOCK DELETE (TCHN1 - 8)
TRANSMIT STUFF REQUEST STROBE (TSREST)
(TSREST-)
MINOR FRAME COUNTS
BIT 17
(TSREST-)
(TFCT01,02,04,08)
(TGRPE-)
(48 CHE)
MINOR FRAME COUNTS
MINOR FRAME COUNTS
BIT 17
BIT 9
TIMING DECODE GATES
TRANSMIT FRAME CODE ENABLE TIME (TFEET)
TRANSMIT DIGITAL DATA ORDERWIRE (TDTAOW)
TRANSMIT DVOW CLOCK (TDVOW)
TRANSMIT DVOW SMOOTH CLOCK (TDVOWC-)
TRANSMIT BIT COUNTS (BINARY) (TBCT01,02,04)
(TLFOMF)
(T341BT)
(TDEP4)
DIAGNOSTIC DETECTOR
DIAGNOSTIC INDICATOR
TRANSMIT DIAGNOSTIC FAULT (TDFALT)
TRANSMIT DIAGNOSTIC ALARM PRIORITY (TDAP24-)
TO AD (SHT 3)
(TOLTTY)
(TDAP24-)
(TDEP4)
(TMASCLK, DDCLK)
(48 CHE, 96 CHE)
(TCLK, TCLK-)
21A6
DGP NO. 1 (CH A)
(J36)
(CHAN)
(576 KHZ 2)
(RST1-)(CH A)
(IGRP1D) (CH A)
(APAT 1)
FROM AD (SHT 3)
(IGS1-) (CH A)
(TCLK)
(TCHN1)
(TCHAN1)
TIMING EXTRACTOR DIVIDER ÷8
EXTRACTED CLOCK (576 KHZ)
INPUT SECTION
INPUT SELECTOR
DUMMY PATTERN
ACTIVITY PATTERN
WRITE CLOCK
DATA
TO OUTPUT SECTION OF DGP NO. 1 (CH A) (SHT 2)
ON
S1
OFF
INPUT RATE BUFFER
WRITE ADDRESS COUNTER
3-BIT WRITE ADDRESS
ELASTIC STORAGE REGISTER
3-BIT READ ADDRESS
READ ADDRESS COUNTER
RATE COMPARATOR FLIP-FLOP
GROUP 1 (GRP 1)
RATE COMPARE GROUP 1 (RCOM1)
ACTIVITY SELECT GROUP 1 (ACT 1)
21A6
DGP NO. 4 (CH B)
(J39)
(CHAN)
(RST8-)(CH B)
(576 KHZ 2)
(IGRP8D)(CH B)
(APAT 2)
FROM AD (SHT 3)
(IGS8-) (CH B)
(TCLK)
(TCHN8)
(TCHAN8)
INPUT SECTION
(GRP 8)
(RCOM8)
(ACT 8)
(576 KHZ 1)
(PRS-)
21A2
GTM (J32)
(576 KHZ 1)
ADDRESS CLOCKS
(PRS-)
ADDRESS COUNTER
SCAN INTERVAL GENERATOR
GROUP FRAME MONITOR STROBE (GFMST)
GROUP FRAME MONITOR TERMINAL COUNT (GFMTC-)
GROUP FRAME SCAN ADDRESS BITS (GF1,2,4,8,R-)
(IGRP1D - IGRP8D)
INPUT GROUP DATA
GROUP DATA AND TIMING SELECTORS
FROM OUTPUT SECTIONS OF DGP'S (SHT 2)
(OGRP1D - OGRP8D)
(OGRP1T - OGRP8T)
(ACT 1 - 8)
OUTPUT GROUP DATA
OUTPUT GROUP TIMING
CLEAR
DUMMY PATTERN DETECTOR AND COUNTER
GROUP DATA TRAFFIC MONITOR
GOOD STATUS (GS)
DUMMY SYNC (DS)
GROUP IDLE (IDLE, IDLE-)
TO AD (SHT 3)
DGTL VO XMT
21A15
RAL
J4
DIGITAL VOICE EXTENSION INPUT (DVEXI)
21A11
DVOW (J45)
ENCODER
(DVEXI)
FROM AVOW (SHT 3)
(DVMIC)
(DVRNGS)
INPUT CIRCUITS
DATA
CVSD ENCODER
(TCLK)
(TDVOW)
(TDVOWC-)
TIMING SELECTION CIRCUITS
TIMING
(96 CHE)
(48 CHE)
DVOW INPUT (DVOWI)
(DVOWI)
(TTYOWI)
21A4
MD/C (J34)
(GRP 1 - GRP 8)
(TDTAOW)
(TDVOW)
(TBCT01,02,04)
(TGRPE-)
(TSCODE)
(TSCODE-)
(TFEET)
COMBINER CIRCUITS
NONRETURN TO ZERO OUTPUT (NRZOUT)
(TCLK)
(PRS-)
+5V DC
+12V DC
POWER ON CIRCUITS
POWER ON RESET (PRS-)
DIAGNOSTIC DETECTOR CIRCUITS
(96 CHE)
(48 CHE)
(RCOM1 - RCOM8)
(TCLK-)
(TSREST)
(TFC11-)
(TFCT01,02,04,08)
STUFF REQUEST CIRCUITS
STUFF
NO STUFF
(TFCT04,08)
(TOLTTY)
DIAGNOSTIC INDICATOR
TRANSMIT DIAGNOSTIC ENABLE PRIORITY 4 (TDEP4)
(TTTYOW)
TRANSMIT DIRECT TTY (TOLTTY)
(TDAP24-)
21A1
RAL
DGTL DATA XMT
JUMPER SWITCHES
OPTICAL COUPLER
DIGITAL DATA SEND INPUT
DIGITAL DATA TX INPUT
TTY
SEND
OFF
RING
DIGITAL DATA SEND
DIGITAL DATA RING
DIGITAL DATA RECEIVE
DIGITAL DATA READY
RCV
OFF
READY
TO DDOW ENCODER (SHT 4)
TO DDOW ENCODER (SHT 4), AVOW (SHT 3)

DGP CARD NOTES:

1. EACH DGP CARD CONTAINS TWO IDENTICAL INPUT SECTIONS (CH A AND CH B). THE FOLLOWING LIST RELATES EACH GROUP INPUT TO A DGP AND CH.
   GROUP INPUT 1 DGP NO. 1 (CH A) (J36)
   GROUP INPUT 2 DGP NO. 2 (CH A) (J37)
   GROUP INPUT 3 DGP NO. 3 (CH A) (J38)
   GROUP INPUT 4 DGP NO. 4 (CH A) (J39)
   GROUP INPUT 5 DGP NO. 1 (CH B) (J36)
   GROUP INPUT 6 DGP NO. 2 (CH B) (J37)
   GROUP INPUT 7 DGP NO. 3 (CH B) (J38)
   GROUP INPUT 8 DGP NO. 4 (CH B) (J39)
2. FOR SIMPLICITY, ONLY THE BLOCK DIAGRAM FOR DGP NO. 1 CH A IS SHOWN.
3. APAT 1 TO DGP'S [illegible]
   APAT 2 TO DGP'S [illegible] AND NO. 4


21A8
SG O/R (J41)
SG INPUT (SGIN1,2)
(J20)
BIPOLAR-TO-POLAR CONVERSION AND TIMING RECOVERY CIRCUITS
1/2-BAUD POLAR DATA
EXTRACTED TIMING
RECEIVED ANALOG VOICE CABLE POWER (RAVCP)
(NRZOUT)
(TMASCLK)
DIGITAL LOOP SELECTOR
DATA
TIMING
(LOOP-)
NRZ DATA RETIME AND PHASE FORCE CIRCUITS
RECEIVE DATA (RDATA)
RECEIVE PHASE FORCING (RPHF)
RECEIVE MASTER CLOCK (RMASCLK)
DIAGNOSTIC INDICATOR
(RNOCLK)
(RMSYNC)
TO T2 (SHT 3)
TO DRIVER SECTION OF SG O/R (SHT 1)
FROM DRIVER SECTION OF SG O/R (SHT 1)
FROM FRONT PANEL (SHT 1)
TO AD (SHT 3)
(RMASCLK)
(RPHF)
(RFSYNC-)
21A5
TC (D)
(J40)
(RMASCLK)
CLOCK SELECTION CIRCUITS
(RMSYNC-)
RECEIVE NO CLOCK (RNOCLK)
(RNOCLK-)
RECEIVE CLOCK (RCLK-)
(RCLK)
RECEIVE BIT TIME 341 (R341BT-)
FROM MO/C (SHT 1)
(96 CHE)
(48 CHE)
MINOR FRAME COUNTER AND DECODER
(R341BT)
FRAME COUNTER AND DECODER
RECEIVE LAST FRAME OF MAJOR FRAME (RLFOMF)
RECEIVE LAST BIT OF MAJOR FRAME (RLBMF-)
(RDLTTY)
RESET
PRESET
BIT 17
MINOR FRAME COUNTS
O/H TIME GATE
RECEIVE FRAME COUNTS
BIT COUNTER AND DECODER
BITS 1 - 4 OR BITS 1 - 8 OF MINOR FRAME 0
BIT 9
MINOR FRAME 0
DESTUFF CIRCUITS
RECEIVE STUFF CODE (RSCODE)
(RSCODE+)
RECEIVE CHANNEL CLOCK DELETE (RCHN1 - 8)
MINOR FRAME 2
RECEIVE STUFF REQUEST STROBE (RSREST-)
MINOR FRAME COUNTS
RECEIVE FRAME CODE ENABLE TIME (RFCET)
RECEIVE DIGITAL DATA ORDERWIRE (RDTAOW)
RECEIVE FRAME COUNTS
O/H BIT TIMES
(48 CHE)
TIMING DECODE GATES
RECEIVE OVOW CLOCK (ROVOW)
RECEIVE OVOW SMOOTH-CLOCK (ROVOWC-)
BIT 9
(RLFOMF)
(R341BT)
(RDEP4)
DIAGNOSTIC DETECTOR
DIAGNOSTIC INDICATOR
RECEIVE DIAGNOSTIC FAULT (RDFALT)
FROM AD (SHT 3)
(RDEP2)
(RDEP2-)
TO AD (SHT 3)
RECEIVE CHANNEL CLOCK (RCHAN1 - 8)
RECEIVE DIAGNOSTIC ALARM PRIORITY (RDAP24-)
(RCHAN1 - 8)
(RDAP24-)
(RDEP4)
21A7
FS (J41)
(RDATA)
(RCLK-)
FRAME SYNC DETECTION CIRCUITS
SG DATA (SDATA,SDATA-)
FRAME SYNC DECODE
MAJOR FRAME SYNC DECODE
(RMSYNC,RMSYNC-)
(RFSYNC-)
(RNOCLK-)
PRESET
(RCLK)
(R341BT-)
FRAME SYNC MAINTENANCE CIRCUITS
RECEIVE FRAME SYNC (RFSYNC-)
RECEIVE MAJOR FRAME SYNC (RMSYNC,RMSYNC-)
(R341BT)
(RLBMF-)
RECEIVE MAJOR FRAME SYNC LEVEL 8 (SYNC 8,SYNC 8-)
TO AD (SHT 3)
(RDLTTY)
(SDATA-)
(RSCODE)
(SDATA)
DESTUFF DETECTION CIRCUITS
(RSCODE-)
(RSREST-)
(RFCET)
RECEIVE DELETE (RDLTTY)
RECEIVE DIAGNOSTIC ENABLE PRIORITY 4 (RDEP4)
DIAGNOSTIC INDICATOR
RDAP24-
21A8
DGP NO. 1 (CH A)
(J38)
OUTPUT SECTION
(RCLK-)
(RCHAN1) (CH A)
(RCHN1) (CH A)
DESTUFF GATE
OUTPUT SELECTOR
(576 KHZ 2)
(SDATA)
(ARAT 1)
(RMSYNC-)
(ACT 1) (CH A)
FROM INPUT SECTION OF DGP NO. 1 (CH A) (SHT 1)
WRITE CLOCK
DATA
OUTPUT RATE BUFFER
WRITE ADDRESS COUNTER
3-BIT WRITE ADDRESS
4TH BIT OF WRITE ADDRESS
PHASE-LOCKED-LOOP
ELASTIC STORAGE REGISTER
DATA
4TH BIT OF READ ADDRESS
3-BIT READ ADDRESS
READ ADDRESS COUNTER
READ CLOCK
PHASE-LOCKED LOOP OUTPUT (576 KHZ)
OUTPUT LOGIC
21A8
DGP NO. 4 (CH B)
(J39)
OUTPUT SECTION
(RCLK-)
(RCHAN8) (CH B)
(RCHN8) (CH B)
(SDATA)
(RMSYNC-)
DGP NOTES:
1. EACH DGP CARD CONTAINS TWO IDENTICAL OUTPUT SECTIONS (CH A AND CH B). THE FOLLOWING LIST RELATES EACH GROUP OUTPUT TO A DGP AND CH.
GROUP OUTPUT 1 DGP NO. 1 (CH A)
GROUP OUTPUT 2 DGP NO. 2 (CH A)
GROUP OUTPUT 3 DGP NO. 3 (CH A)
GROUP OUTPUT 4 DGP NO. 4 (CH A)
GROUP OUTPUT 5 DGP NO. 1 (CH B)
GROUP OUTPUT 6 DGP NO. 2 (CH B)
GROUP OUTPUT 7 DGP NO. 3 (CH B)
GROUP OUTPUT 8 DGP NO. 4 (CH B)
2. FOR SIMPLICITY, ONLY THE BLOCK DIAGRAM FOR DGP NO. 1 CH A IS SHOWN.
FROM FRONT PANEL (SHT 3)

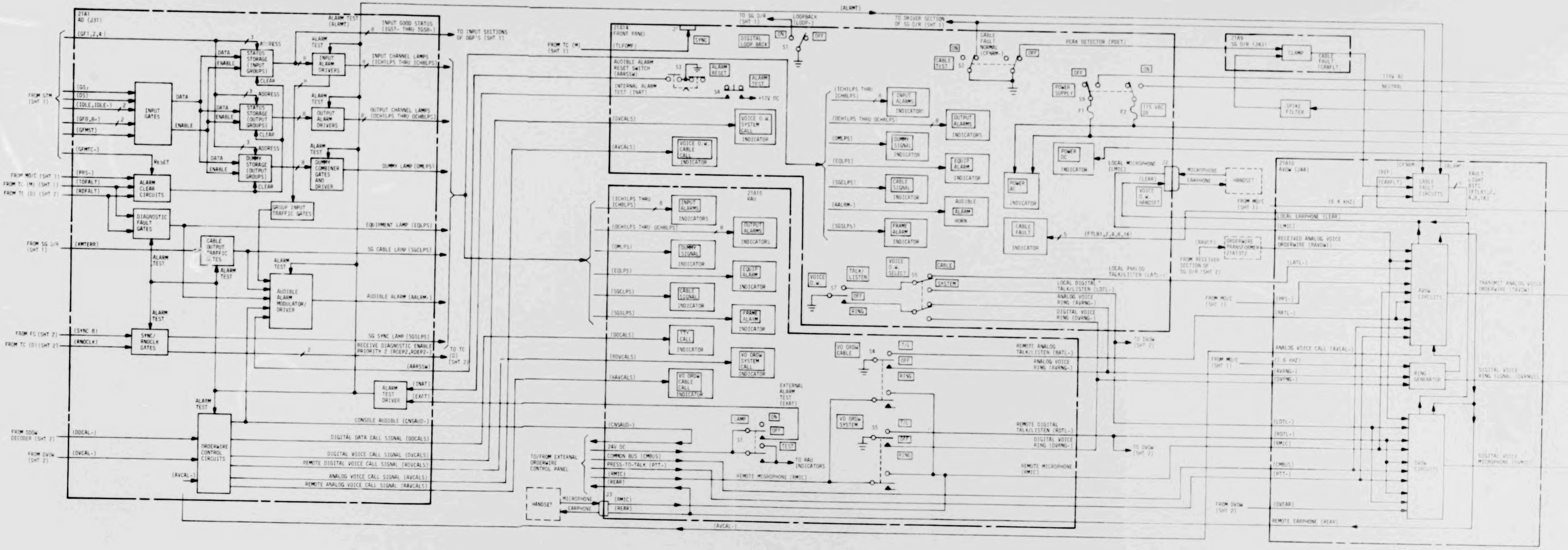
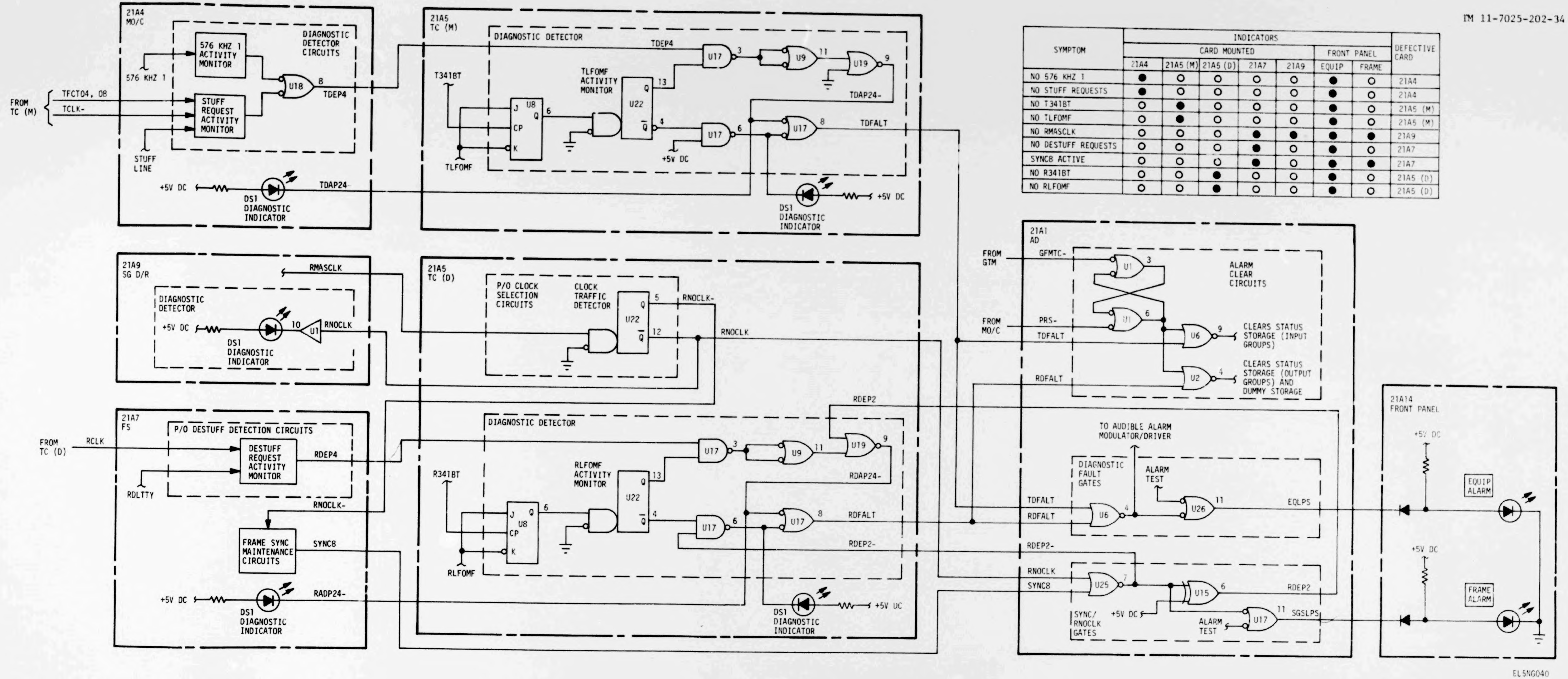
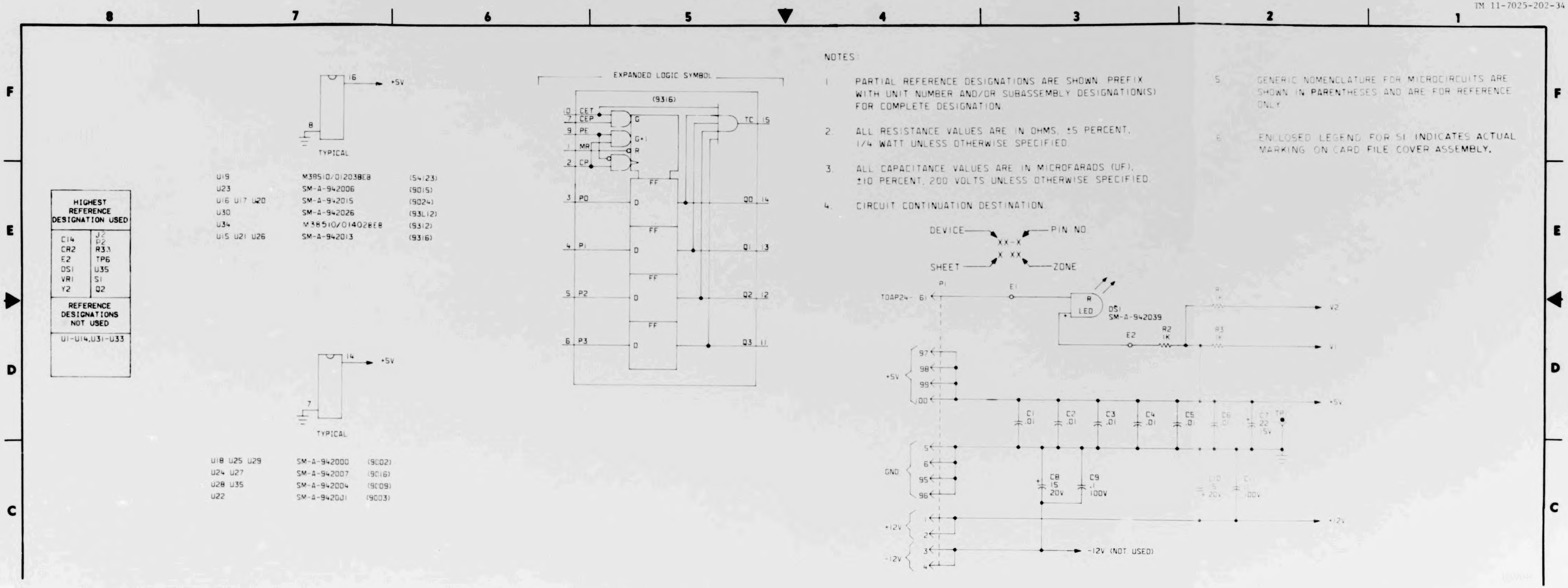

21A1
AD (J31)
(GF1,2,4)
FROM GTM (SHT 1)
(GS)
(DS)
(IDLE,IDLE-)
(GF8,8-)
(GFMST)
(GFMTC-)
INPUT GATES
DATA
ENABLE
ADDRESS
STATUS STORAGE (INPUT GROUPS)
STATUS STORAGE (OUTPUT GROUPS)
DUMMY STORAGE (OUTPUT GROUPS)
CLEAR
RESET
FROM MD/C (SHT 1)
FROM TC (M) (SHT 1)
FROM TC (D) (SHT 2)
(PRS-)
(TDFALT)
(RDFALT)
ALARM CLEAR CIRCUITS
DIAGNOSTIC FAULT GATES
FROM SG D/R (SHT 1)
(XMTERR)
CABLE OUTPUT TRAFFIC GATES
GROUP INPUT TRAFFIC GATES
ALARM TEST
INPUT ALARM DRIVERS
OUTPUT ALARM DRIVERS
DUMMY COMBINER GATES AND DRIVER
AUDIBLE ALARM MODULATOR/DRIVER
FROM FS (SHT 2)
FROM TC (D) (SHT 2)
(SYNC 8)
(RNOCLK)
SYNC/RNOCLK GATES
ALARM TEST DRIVER
FROM DDOW DECODER (SHT 2)
FROM DVOW (SHT 2)
(DDCAL-)
(DVCAL-)
(AVCAL-)
ORDERWIRE CONTROL CIRCUITS
ALARM TEST (ALRMT)
INPUT GOOD STATUS (IGS1- THRU IGS8-)
TO INPUT SECTIONS OF DGP'S (SHT 1)
INPUT CHANNEL LAMPS (ICH1LPS THRU ICH8LPS)
OUTPUT CHANNEL LAMPS (OCH1LPS THRU OCH8LPS)
DUMMY LAMP (DMLPS)
EQUIPMENT LAMP (EQLPS)
SG CABLE LAMP (SGCLPS)
AUDIBLE ALARM (AALRM-)
SG SYNC LAMP (SGSLPS)
RECEIVE DIAGNOSTIC ENABLE PRIORITY 2 (RDEP2,RDEP2-)
TO TC (D) (SHT 2)
(AARSSW)
(INAT)
(EXAT)
CONSOLE AUDIBLE (CNSAUD-)
DIGITAL DATA CALL SIGNAL (DDCALS)
DIGITAL VOICE CALL SIGNAL (DVCALS)
REMOTE DIGITAL VOICE CALL SIGNAL (RDVCALS)
ANALOG VOICE CALL SIGNAL (AVCALS)
REMOTE ANALOG VOICE CALL SIGNAL (RAVCALS)
(ALRMT)
TO SG D/R (SHT 1)
LOOPBACK (LOOP-)
TO DRIVER SECTION OF SG D/R (SHT 1)
21A14
FRONT PANEL
J1
SYNC
FROM TC (M) (SHT 1)
(TLFOMF)
DIGITAL LOOP BACK
ON
OFF
S1
AUDIBLE ALARM RESET SWITCH (AARSSW)
S3
ALARM RESET
INTERNAL ALARM TEST (INAT)
S4
ALARM TEST
+12V DC
(DVCALS)
VOICE O.W. SYSTEM CALL INDICATOR
(AVCALS)
VOICE O.W. CABLE CALL INDICATOR
CABLE FAULT NORMAL (CFNRM-)
CABLE TEST
S2
PEAK DETECTOR (PDET)
POWER SUPPLY
S9
F1
F2
115 VAC 2A
(ICH1LPS THRU ICH8LPS)
INPUT ALARMS INDICATORS
(OCH1LPS THRU OCH8LPS)
OUTPUT ALARMS INDICATORS
(DMLPS)
DUMMY SIGNAL INDICATOR
(EQLPS)
EQUIP ALARM INDICATOR
(SGCLPS)
CABLE SIGNAL INDICATOR
(AALRM-)
AUDIBLE ALARM HORN
(SGSLPS)
FRAME ALARM INDICATOR
POWER DC INDICATOR
POWER AC INDICATOR
CABLE FAULT INDICATOR
(FTLB1,2,4,8,16)
LOCAL MICROPHONE (LMIC)
J2
(LEAR)
VOICE O.W. HANDSET
MICROPHONE
EARPHONE
HANDSET
VOICE O.W.
TALK/LISTEN
VOICE O.W. SELECT
CABLE
SYSTEM
S5
S7
RING
LOCAL ANALOG TALK/LISTEN (LATL-)
LOCAL DIGITAL TALK/LISTEN (LDTL-)
ANALOG VOICE RING (AVRNG-)
DIGITAL VOICE RING (DVRNG-)
21A15
RAU
(DDCALS)
TTY CALL INDICATOR
(RDVCALS)
VO ORDW SYSTEM CALL INDICATOR
(RAVCALS)
VO ORDW CABLE CALL INDICATOR
EXTERNAL ALARM TEST (EXAT)
LAMP
TEST
TO RAU INDICATORS
VO ORDW CABLE
VO ORDW SYSTEM
T/L
TO DVOW (SHT 2)
REMOTE ANALOG TALK/LISTEN (RATL-)
REMOTE DIGITAL TALK/LISTEN (RDTL-)
DIGITAL VOICE RING (DVRNG-)
REMOTE MICROPHONE (RMIC)
(CNSAUD-)
TO/FROM EXTERNAL ORDERWIRE CONTROL PANEL
24V DC
COMMON BUS (CMBUS)
PRESS-TO-TALK (PTT-)
(RMIC)
(REAR)
J3
(AVCAL-)
21A9
SG D/R (J43)
CLAMP
CABLE FAULT (CABFLT)
SPIKE FILTER
115V AC
NEUTRAL
21A10
AVOW (J44)
(CFNRM-)
(ALRMT)
(REF)
(CABFLT)
CABLE FAULT CIRCUITS
FAULT LIGHT BITS (FTLB1,2,4,8,16)
FROM MD/C (SHT 1)
(6.4 KHZ)
LOCAL EARPHONE (LEAR)
(LMIC)
(RAVCP)
ORDERWIRE TRANSFORMER 21A13T2
FROM RECEIVER SECTION OF SG D/R (SHT 2)
RECEIVED ANALOG VOICE ORDERWIRE (RAVOW)
(LATL-)
(PRS-)
(RATL-)
AVOW CIRCUITS
TRANSMIT ANALOG VOICE ORDERWIRE (TAVOW)
ANALOG VOICE CALL (AVCAL-)
(1.6 KHZ)
(AVRNG-)
(DVRNG-)
RING GENERATOR
DIGITAL VOICE RING SIGNAL (DVRNGS)
(LDTL-)
(RDTL-)
(CMBUS)
(PTT-)
FROM DVOW (SHT 2)
(DVEAR)
DVOW CIRCUITS
DIGITAL VOICE MICROPHONE (DVMIC)
REMOTE EARPHONE (REAR)

Figure FO-1. TD-976/
diagram (sheet 1


21A4
MO/C
576 KHZ 1 ACTIVITY MONITOR
DIAGNOSTIC DETECTOR CIRCUITS
576 KHZ 1
FROM TC (M)
TFCT04, 08
TCLK-
STUFF REQUEST ACTIVITY MONITOR
U18
8
TDEP4
STUFF LINE
+5V DC
DS1 DIAGNOSTIC INDICATOR
TDAP24
21A5
TC (M)
DIAGNOSTIC DETECTOR
TDEP4
T341BT
TLFOMF ACTIVITY MONITOR
J
U8
Q
CP
K
6
U22
Q
13
4
TLFOMF
U17
3
U9
11
U19
9
TDAP24-
U17
6
+5V DC
U17
8
TDFALT
DS1 DIAGNOSTIC INDICATOR
+5V DC
21A9
SG D/R
RMASCLK
DIAGNOSTIC DETECTOR
+5V DC
DS1 DIAGNOSTIC INDICATOR
10
U1
RNOCLK
21A5
TC (D)
P/O CLOCK SELECTION CIRCUITS
CLOCK TRAFFIC DETECTOR
U22
5
12
RNOCLK-
RNOCLK
21A7
FS
FROM TC (D)
RCLK
P/O DESTUFF DETECTION CIRCUITS
DESTUFF REQUEST ACTIVITY MONITOR
RDEP4
RDLTTY
RNOCLK-
FRAME SYNC MAINTENANCE CIRCUITS
SYNC8
+5V DC
DS1 DIAGNOSTIC INDICATOR
RADP24-
DIAGNOSTIC DETECTOR
R341BT
RLFOMF ACTIVITY MONITOR
U8
U22
13
4
RLFOMF
U17
3
U9
11
U19
9
RDEP2
RDAP24-
U17
6
U17
8
RDFALT
RDEP2-
DS1 DIAGNOSTIC INDICATOR
+5V DC
21A1
AD
FROM GTM
GFMTC-
U1
3
ALARM CLEAR CIRCUITS
FROM MO/C
PRS-
U1
6
TDFALT
U6
9
CLEARS STATUS STORAGE (INPUT GROUPS)
RDFALT
U2
4
CLEARS STATUS STORAGE (OUTPUT GROUPS) AND DUMMY STORAGE
TO AUDIBLE ALARM MODULATOR/DRIVER
DIAGNOSTIC FAULT GATES
ALARM TEST
TDFALT
RDFALT
U6
4
U26
11
EQLPS
RDEP2-
RNOCLK
SYNC8
U25
7
U15
6
RDEP2
SYNC/RNOCLK GATES
+5V DC
ALARM TEST
U17
11
SGSLPS
21A14
FRONT PANEL
+5V DC
EQUIP ALARM
+5V DC
FRAME ALARM
EL5NG040

SYMPTOM	INDICATORS							DEFECTIVE CARD
	CARD MOUNTED					FRONT PANEL		
	21A4	21A5 (M)	21A5 (D)	21A7	21A9	EQUIP	FRAME	
NO 576 KHZ 1	●	○	○	○	○	●	○	21A4
NO STUFF REQUESTS	●	○	○	○	○	●	○	21A4
NO T341BT	○	●	○	○	○	●	○	21A5 (M)
NO TLFOMF	○	●	○	○	○	●	○	21A5 (M)
NO RMASCLK	○	○	○	●	●	●	●	21A9
NO DESTUFF REQUESTS	○	○	○	●	○	●	○	21A7
SYNC8 ACTIVE	○	○	○	●	○	●	●	21A7
NO R341BT	○	○	●	○	○	●	○	21A5 (D)
NO RLFOMF	○	○	●	○	○	●	○	21A5 (D)

Figure FO-2. EQUIP ALARM and FRAME ALARM circuits, simplified diagram.


8
7
6
5
4
3
2
1
F
E
D
C
16
+5V
8
TYPICAL
14
+5V
7
TYPICAL
EXPANDED LOGIC SYMBOL
(9316)
10 CET
7 CEP
9 PE
1 MR
2 CP
G
G+1
R
TC 15
FF
D
3 P0
4 P1
5 P2
6 P3
Q0 14
Q1 13
Q2 12
Q3 11
DEVICE
PIN NO.
XX-X
X XX
SHEET
ZONE
P1
TOAP24- 61
E1
R
LED
DS1
SM-A-942039
E2
R2
1K
R1
1K
R3
1K
V2
V1
+5V
97
98
99
100
C1 .01
C2 .01
C3 .01
C4 .01
C5 .01
C6 .01
C7 22 15V
TP1
GND
5
6
95
96
C8 15 20V
C9 .1 100V
C10 15 20V
C11 .1 100V
+12V
1
2
-12V
3
4
-12V (NOT USED)

HIGHEST REFERENCE DESIGNATION USED	
C14	J2 P2
CR2	R33
E2	TP6
DS1	U35
VR1	S1
Y2	Q2

REFERENCE DESIGNATIONS NOT USED
U1-U14,U31-U33

U19	M38510/01203BEB	(54123)
U23	SM-A-942006	(9015)
U16 U17 U20	SM-A-942015	(9024)
U30	SM-A-942026	(93L12)
U34	M38510/01402BEB	(9312)
U15 U21 U26	SM-A-942013	(9316)

U18 U25 U29	SM-A-942000	(9002)
U24 U27	SM-A-942007	(9016)
U28 U35	SM-A-942004	(9009)
U22	SM-A-942001	(9003)

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.
4. CIRCUIT CONTINUATION DESTINATION.
5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.
6. ENCLOSED LEGEND FOR S1 INDICATES ACTUAL MARKING ON CARD FILE COVER ASSEMBLY.

Figure FO-3. MO/C card 21A4, schematic diagram (sheet 1 of 4).

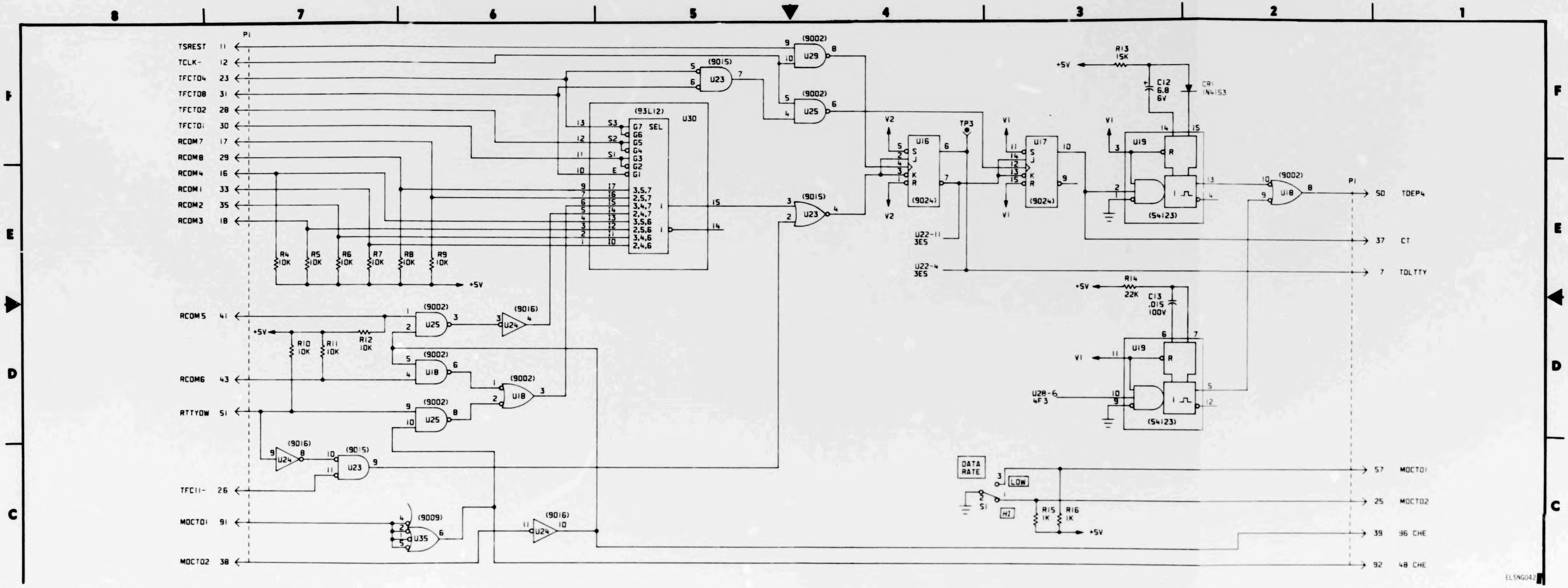

8
7
6
5
4
3
2
1
F
E
D
C
P1
TSREST 11
TCLK- 12
TFCT04 23
TFCT08 31
TFCT02 28
TFCT01 30
RCOM7 17
RCOM8 29
RCOM4 16
RCOM1 33
RCOM2 35
RCOM3 18
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
+5V
(93L12)
U30
G7 SEL
S3
S2
S1
E
(9002)
U29
(9015)
U23
U25
TP3
V2
V1
U16
(9024)
U17
U22-11 3E5
U22-4 3E5
R13 15K
C12 6.8 6V
CR1 1N4153
U19
(54123)
U18
TDEP4
CT
TDLTTY
R14 22K
C13 .015 100V
U28-6 4F3
RCOM5 41
RCOM6 43
RTTYOW 51
TFC11- 26
MOCTO1 91
MOCTO2 38
R10 10K
R11 10K
R12 10K
(9016)
U24
(9009)
U35
DATA RATE
LOW
HI
S1
R15 1K
R16 1K
50
37
7
57 MOCTO1
25 MOCTO2
39 96 CHE
92 48 CHE
EL5NG042

Figure FO-3. MO/C card 21A4, schematic diagram (sheet 2 of 4).

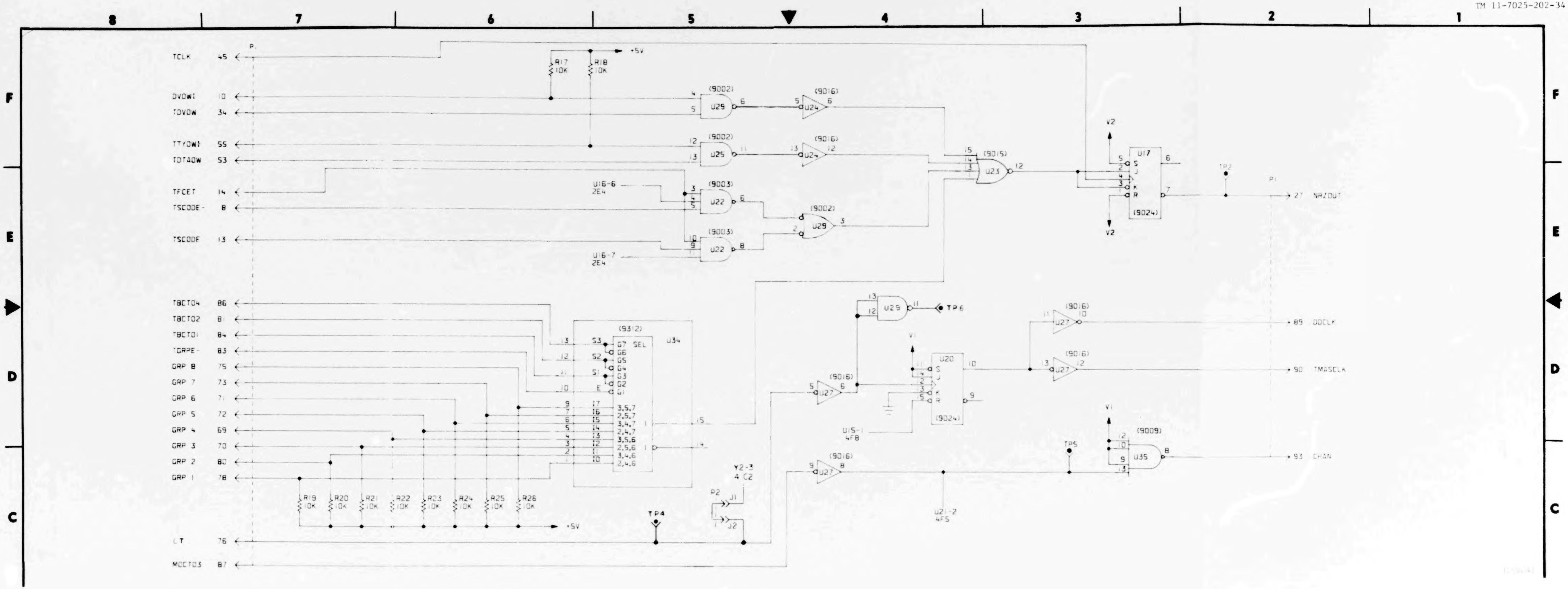

8
7
6
5
4
3
2
1
F
E
D
C
P1
TCLK 45
DVDWI 10
TDVDW 34
TTYDWI 55
TDTADW 53
TFCET 14
TSCODE- 8
TSCODF 13
TBCT04 86
TBCT02 81
TBCT01 84
TGRPE- 83
GRP 8 75
GRP 7 73
GRP 6 71
GRP 5 72
GRP 4 69
GRP 3 70
GRP 2 80
GRP 1 78
CT 76
MOCT03 87
+5V
R17 10K
R18 10K
(9002) U25
(9016) U24
U16-6 2E4
U16-7 2E4
(9003) U22
(9002) U29
(9015) U23
V2
U17 (9024)
S
J
K
R
TP2
P1
27 NRZOUT
(9312) U34 SEL
S3 S2 S1 E
G7 G6 G5 G4 G3 G2 G1
3,5,7
2,5,7
3,4,7
2,4,7
3,5,6
2,5,6
3,4,6
2,4,6
R19 10K
R20 10K
R21 10K
R22 10K
R23 10K
R24 10K
R25 10K
R26 10K
TP4
Y2-3 4 C2
P2
J1
J2
U29
TP6
V1
U20 (9024)
(9016) U27
U15-1 4F8
89 DDCLK
90 TMASCLK
TP5
(9009) U35
U21-2 4F5
93 CHAN

Figure FO-3. MO/C card 21A4, schematic diagram (sheet 3 of 4).

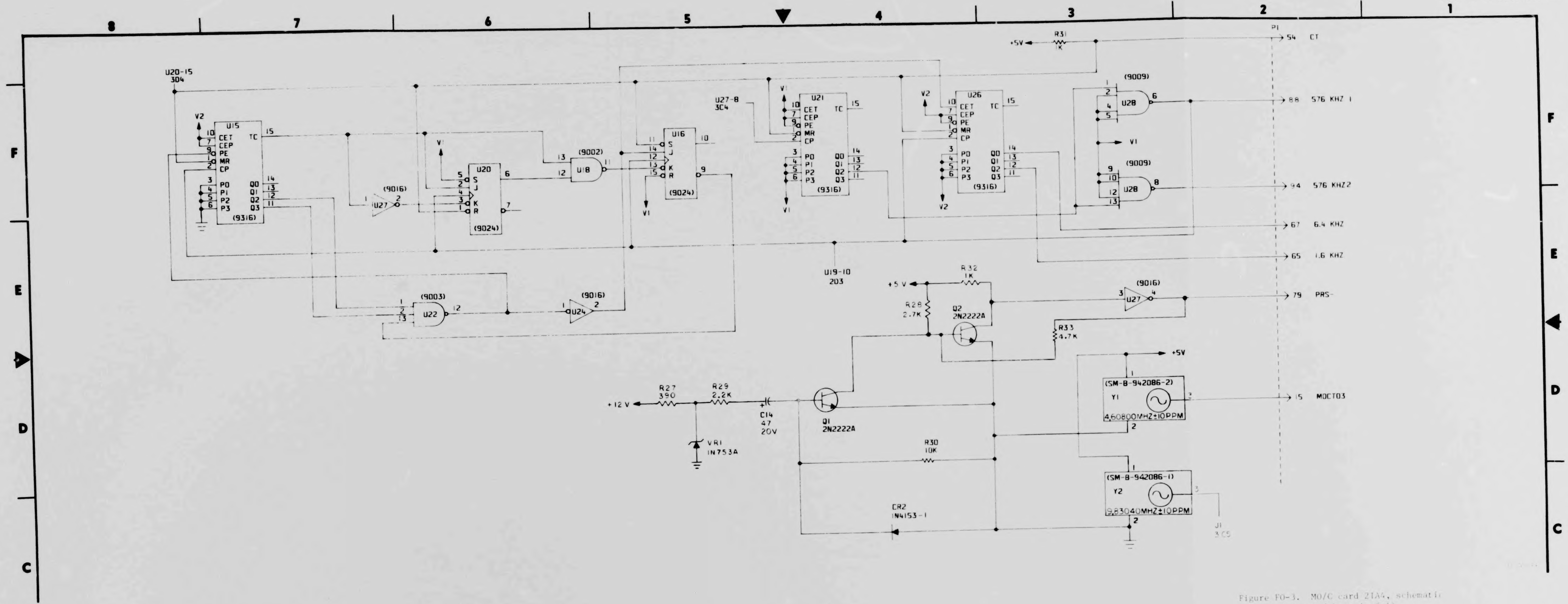

8
7
6
5
4
3
2
1
F
E
D
C
U20-15
3D4
V2
U15
CET
CEP
PE
MR
CP
TC
P0
P1
P2
P3
Q0
Q1
Q2
Q3
(9316)
(9016)
U27
(9024)
U20
S
J
K
R
(9002)
U18
U16
(9024)
(9003)
U22
(9016)
U24
V1
U27-8
3C4
U21
(9316)
U19-10
2D3
U26
(9316)
(9009)
U28
(9009)
U28
+5V
R31
1K
P1
54 CT
88 576 KHZ 1
94 576 KHZ 2
67 6.4 KHZ
65 1.6 KHZ
79 PRS-
15 MOCT03
R32
1K
+5 V
R28
2.7K
Q2
2N2222A
R33
4.7K
(9016)
U27
+12 V
R27
390
R29
2.2K
C14
47
20V
Q1
2N2222A
VR1
1N753A
R30
10K
CR2
1N4153-1
(SM-B-942086-2)
Y1
4.60800MHZ±10PPM
(SM-B-942086-1)
Y2
9.83040MHZ±10PPM
J1
3C5

Figure FO-3. MO/C card 2IA4, schematic diagram (sheet 4 of 4).

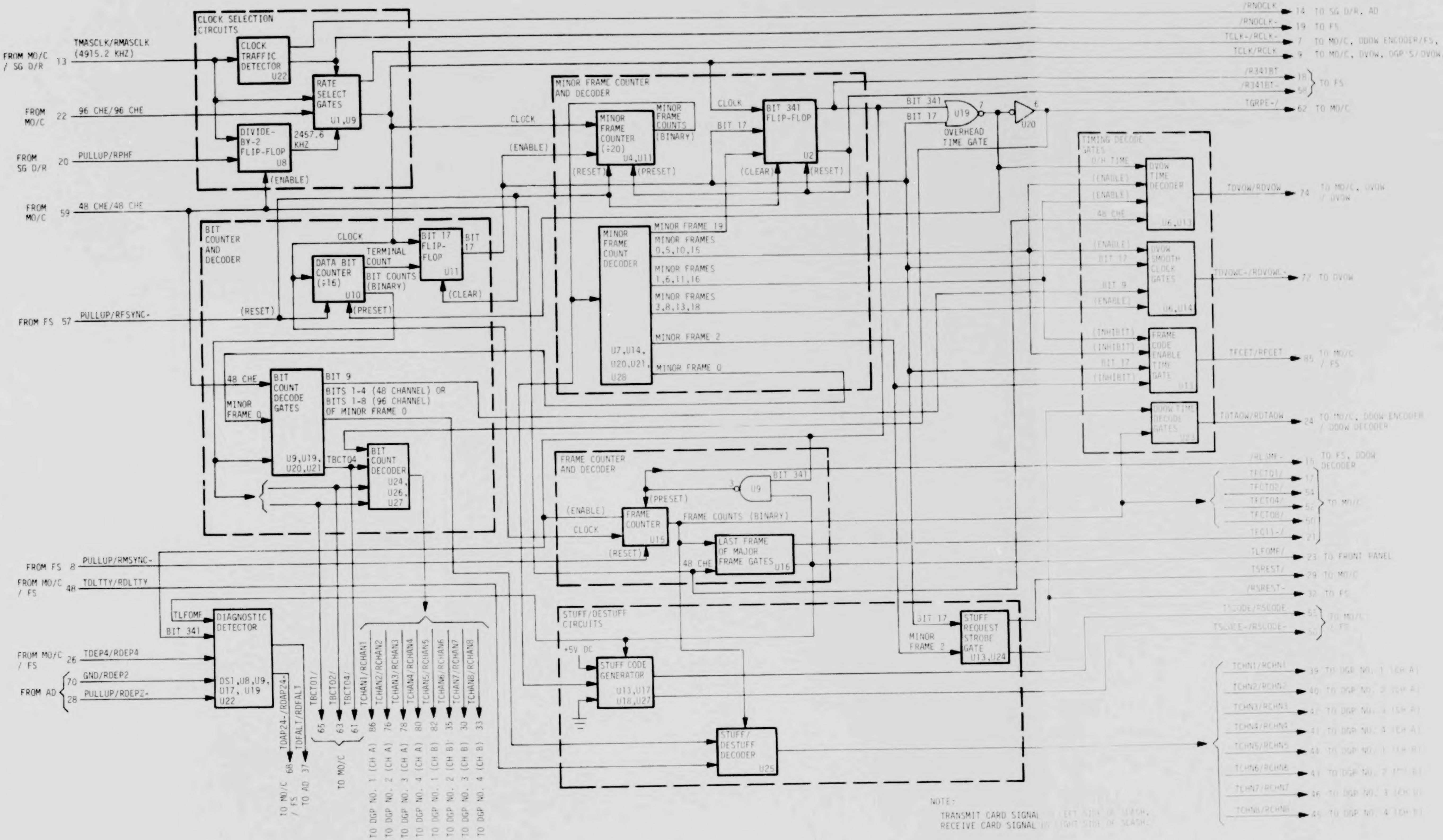
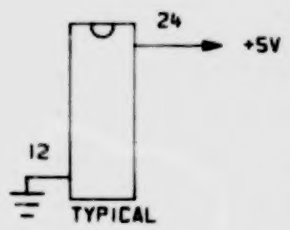
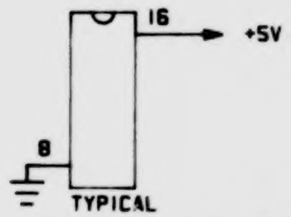

CLOCK SELECTION CIRCUITS
CLOCK TRAFFIC DETECTOR U22
RATE SELECT GATES U1,U9
DIVIDE-BY-2 FLIP-FLOP U8
2457.6 KHZ
(ENABLE)
FROM MO/C / SG D/R 13 TMASCLK/RMASCLK (4915.2 KHZ)
FROM MO/C 22 96 CHE/96 CHE
FROM SG D/R 20 PULLUP/RPHF
FROM MO/C 59 48 CHE/48 CHE
FROM FS 57 PULLUP/RFSYNC-
FROM FS 8 PULLUP/RMSYNC-
FROM MO/C / FS 48 TDLTTY/RDLTTY
FROM MO/C / FS 26 TDEP4/RDEP4
FROM AD 70 GND/RDEP2
28 PULLUP/RDEP2-
BIT COUNTER AND DECODER
DATA BIT COUNTER (÷16) U10
TERMINAL COUNT
BIT COUNTS (BINARY)
BIT 17 FLIP-FLOP U11
CLOCK
(RESET)
(PRESET)
(CLEAR)
BIT COUNT DECODE GATES U9,U19, U20,U21
48 CHE
MINOR FRAME 0
BIT 9
BITS 1-4 (48 CHANNEL) OR BITS 1-8 (96 CHANNEL) OF MINOR FRAME 0
TBCT04
BIT COUNT DECODER U24, U26, U27
DIAGNOSTIC DETECTOR DS1,U8,U9, U17, U19 U22
TLFOMF
BIT 341
TDAP24-/RDAP24-
TDFALT/RDFALT
TO MO/C / FS 68
TO AD 37
TBCT01/ 65
TBCT02/ 63
TBCT04/ 61
TO MO/C
TCHAN1/RCHAN1 86 TO DGP NO. 1 (CH A)
TCHAN2/RCHAN2 76 TO DGP NO. 2 (CH A)
TCHAN3/RCHAN3 78 TO DGP NO. 3 (CH A)
TCHAN4/RCHAN4 80 TO DGP NO. 4 (CH A)
TCHAN5/RCHAN5 82 TO DGP NO. 1 (CH B)
TCHAN6/RCHAN6 35 TO DGP NO. 2 (CH B)
TCHAN7/RCHAN7 30 TO DGP NO. 3 (CH B)
TCHAN8/RCHAN8 33 TO DGP NO. 4 (CH B)
MINOR FRAME COUNTER AND DECODER
MINOR FRAME COUNTER (÷20) U4,U11
MINOR FRAME COUNTS (BINARY)
(ENABLE)
(RESET)
(PRESET)
CLOCK
BIT 17
BIT 341 FLIP-FLOP U2
(CLEAR)
(RESET)
MINOR FRAME COUNT DECODER U7,U14, U20,U21, U28
MINOR FRAME 19
MINOR FRAMES 0,5,10,15
MINOR FRAMES 1,6,11,16
MINOR FRAMES 3,8,13,18
MINOR FRAME 2
MINOR FRAME 0
BIT 341
BIT 17
U19
U20
OVERHEAD TIME GATE
FRAME COUNTER AND DECODER
FRAME COUNTER U15
(ENABLE)
CLOCK
(RESET)
(PRESET)
U9
BIT 341
FRAME COUNTS (BINARY)
LAST FRAME OF MAJOR FRAME GATES U16
48 CHE
STUFF/DESTUFF CIRCUITS
+5V DC
STUFF CODE GENERATOR U13,U17 U18,U27
STUFF/DESTUFF DECODER U25
STUFF REQUEST STROBE GATE U13,U24
BIT 17
MINOR FRAME 2
TIMING DECODE GATES
O/H TIME
(ENABLE)
48 CHE
DVOW TIME DECODER U6,U13
DVOW SMOOTH CLOCK GATES U6,U14
BIT 17
BIT 9
FRAME CODE ENABLE TIME GATE U13
(INHIBIT)
DDOW TIME DECODE GATES U27
/RNOCLK 14 TO SG D/R, AD
/RNOCLK- 19 TO FS
TCLK-/RCLK- 7 TO MO/C, DDOW ENCODER/FS,
TCLK/RCLK 9 TO MO/C, DVOW, DGP'S/DVOW
/R341BT 18 TO FS
/R341BT- 58
TGRPE-/ 62 TO MO/C
TDVOW/RDVOW 74 TO MO/C, DVOW / DVOW
TDVOWC-/RDVOWC- 72 TO DVOW
TFCET/RFCET 85 TO MO/C / FS
TDTAOW/RDTAOW 24 TO MO/C, DDOW ENCODER / DDOW DECODER
/RLOMF- 15 TO FS, DDOW DECODER
TFCT01/ 17
TFCT02/ 54
TFCT04/ 52
TFCT08/ 50
TFCT1-/ 21
TO MO/C
TLFOMF/ 23 TO FRONT PANEL
TSREST/ 29 TO MO/C
/RSREST- 32 TO FS
TSCODE/RSCODE 55
TSCODE-/RSCODE- 57
TO MO/C / FS
TCHN1/RCHN1 39 TO DGP NO. 1 (CH A)
TCHN2/RCHN2 40 TO DGP NO. 2 (CH A)
TCHN3/RCHN3 42 TO DGP NO. 3 (CH A)
TCHN4/RCHN4 41 TO DGP NO. 4 (CH A)
TCHN5/RCHN5 44 TO DGP NO. 1 (CH B)
TCHN6/RCHN6 43 TO DGP NO. 2 (CH B)
TCHN7/RCHN7 46 TO DGP NO. 3 (CH B)
TCHN8/RCHN8 45 TO DGP NO. 4 (CH B)
NOTE:
TRANSMIT CARD SIGNAL TO LEFT SIDE OF SLASH.
RECEIVE CARD SIGNAL TO RIGHT SIDE OF SLASH.

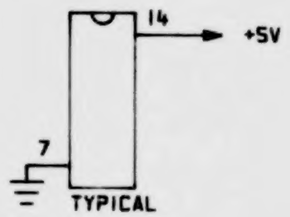
Figure FO-4. TC card 21A5, block diagram


24
+5V
12
TYPICAL

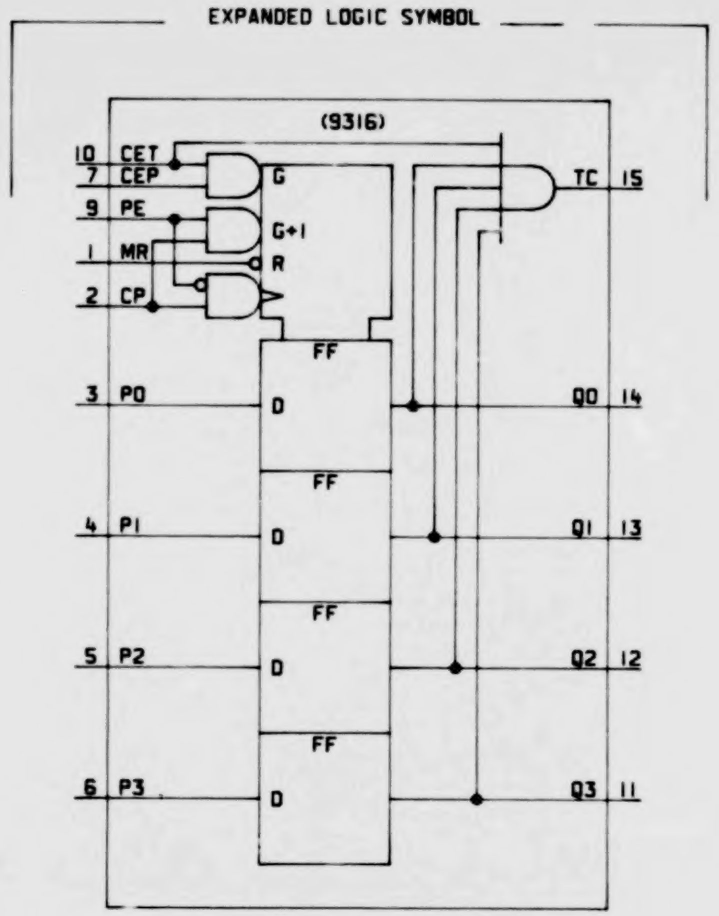
U25,U28	M38510/15201BJB	(9311)


16
+5V
8
TYPICAL

U22	M38510/01203BEB	(54123)
U4,U10,U15	SM-A-942013	(9316)
U8,U11	SM-A-942015	(9024)
U18	M38510/01402BEB	(9312)
U13,U19,U23	SM-A-942006	(9015)
U7,U26	M38510/15206BEB	(9301)


14
+5V
7
TYPICAL

U9,U17	SM-A-942000	(9002)
U2	SM-A-942016	(9001)
U16	SM-A-942001	(9003)
U14,U21	SM-A-942002	(9004)
U20,U24,U27	SM-A-942007	(9016)
U6	SM-A-942008	(9005)
U1	SM-A-942004	(9009)


EXPANDED LOGIC SYMBOL
(9316)
10 CET
7 CEP
9 PE
1 MR
2 CP
G
G+1
R
FF
3 P0
D
4 P1
5 P2
6 P3
TC 15
Q0 14
Q1 13
Q2 12
Q3 11

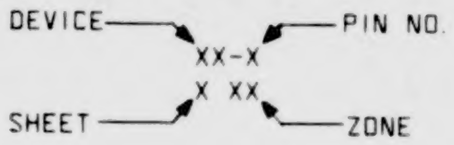
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

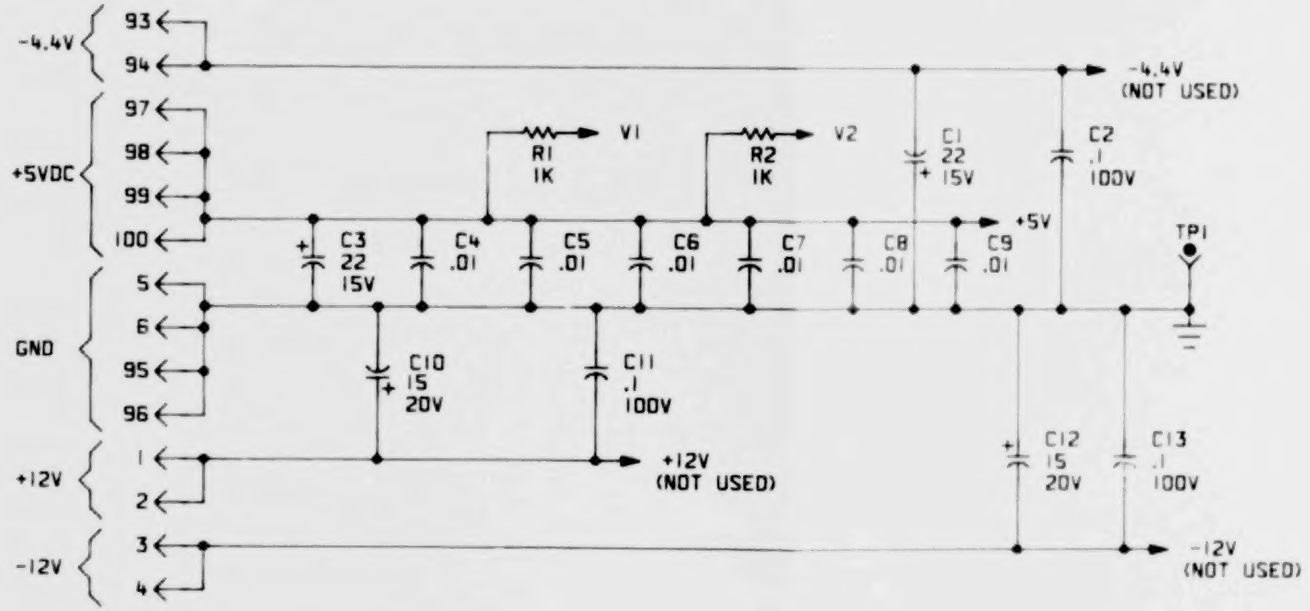
4. CIRCUIT CONTINUATION DESTINATION.


DEVICE
PIN NO.
XX-X
X XX
SHEET
ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

6. SIGNAL NAME CONVENTION:
TRANSMIT CARD SIGNAL/RECEIVE CARD SIGNAL

HIGHEST REFERENCE DESIGNATION USED	
C15 CR1 E2 DS1	P1 R5 TP7 U28
REFERENCE DESIGNATIONS NOT USED	
U3,U5,U12	


-4.4V
93
94
+5VDC
97
98
99
100
GND
5
6
95
96
+12V
1
2
-12V
3
4
R1
1K
V1
R2
1K
V2
C1
22
15V
C2
.1
100V
-4.4V
(NOT USED)
+5V
C3
22
15V
C4
.01
C5
.01
C6
.01
C7
.01
C8
.01
C9
.01
TP1
C10
15
20V
C11
.1
100V
+12V
(NOT USED)
C12
15
20V
C13
.1
100V
-12V
(NOT USED)

EL5NG046

Figure FO-5. TC card 21A5, schematic diagram (sheet 1 of 6).

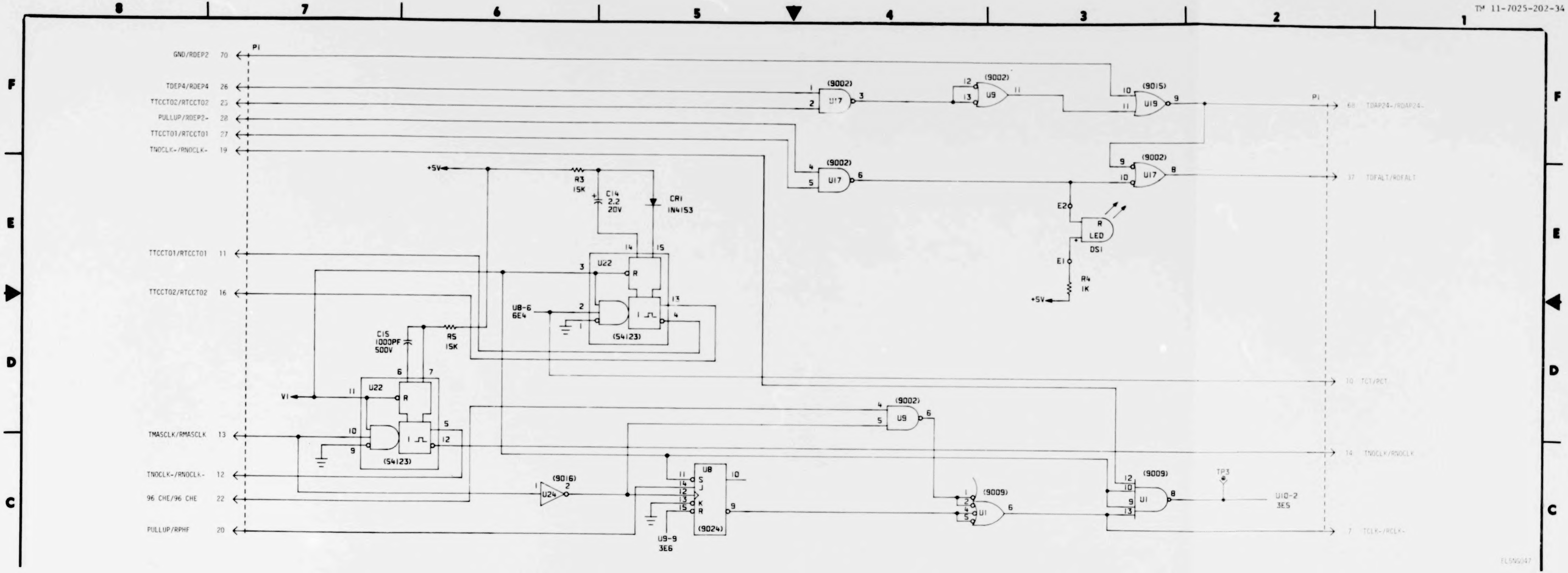

8
7
6
5
4
3
2
1
F
E
D
C
P1
GND/RDEP2 70
TDEP4/RDEP4 26
TTCCT02/RTCCT02 25
PULLUP/RDEP2- 28
TTCCT01/RTCCT01 27
TNOCLK-/RNOCLK- 19
+5V
R3
15K
C14
2.2
20V
CR1
1N4153
TTCCT01/RTCCT01 11
TTCCT02/RTCCT02 16
U22
R
U8-6
6E4
(54123)
C15
1000PF
500V
R5
15K
V1
U22
(54123)
TMASCLK/RMASCLK 13
TNOCLK-/RNOCLK- 12
96 CHE/96 CHE 22
PULLUP/RPHF 20
(9002)
U17
(9002)
U9
(9015)
U19
(9002)
U17
E2
R
LED
DS1
E1
R4
1K
+5V
(9016)
U24
U8
S
J
K
R
(9024)
U9-9
3E6
(9002)
U9
(9009)
U1
(9009)
U1
TP3
U10-2
3E5
68 TDAP24-/RDAP24-
37 TDFALT/RDFALT
10 TCT/RCT
14 TNOCLK/RNOCLK
7 TCLK-/RCLK-
EL5NG047

Figure FO-5. TC card 21A5, schematic diagram (sheet 2 of 6).

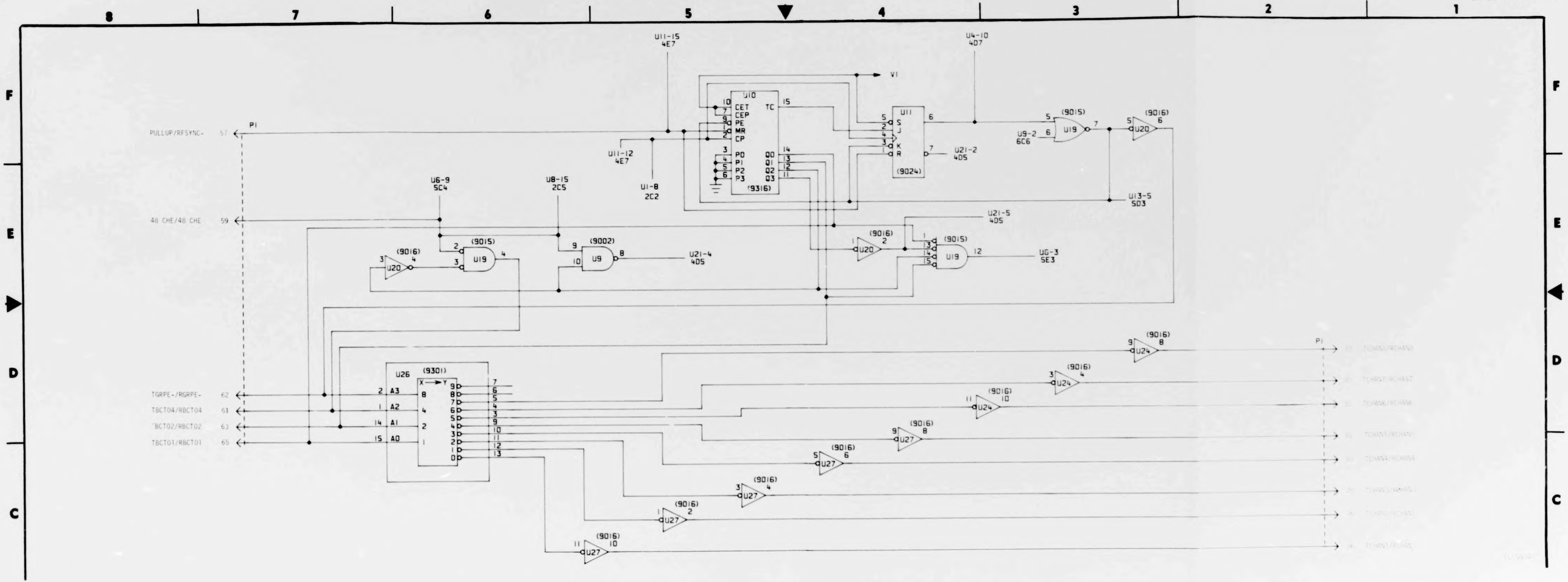

8
7
6
5
4
3
2
1
F
E
D
C
U11-15
4E7
U4-10
4D7
V1
U10
CET
CEP
PE
MR
CP
TC
P0
P1
P2
P3
Q0
Q1
Q2
Q3
(9316)
U11
S
J
K
R
(9024)
U21-2
4D5
(9015)
U19
U9-2
6C6
(9016)
U20
U13-5
5D3
U11-12
4E7
U1-8
2C2
U6-9
5C4
U8-15
2C5
U21-5
4D5
(9002)
U9
U21-4
4D5
U6-3
5E3
P1
PULLUP/RFSYNC- 57
48 CHE/48 CHE 59
TGRPE-/RGRPE- 62
TBCT04/RBCT04 61
TBCT02/RBCT02 63
TBCT01/RBCT01 65
U26
(9301)
A3
A2
A1
A0
X → Y
U24
U27
TCHAN8/RCHAN8
TCHAN7/RCHAN7
TCHAN6/RCHAN6
TCHAN5/RCHAN5
TCHAN4/RCHAN4
TCHAN3/RCHAN3
TCHAN2/RCHAN2
TCHAN1/RCHAN1

Figure FO-5. TC card 21A5, schematic diagram (sheet 3 of 6).

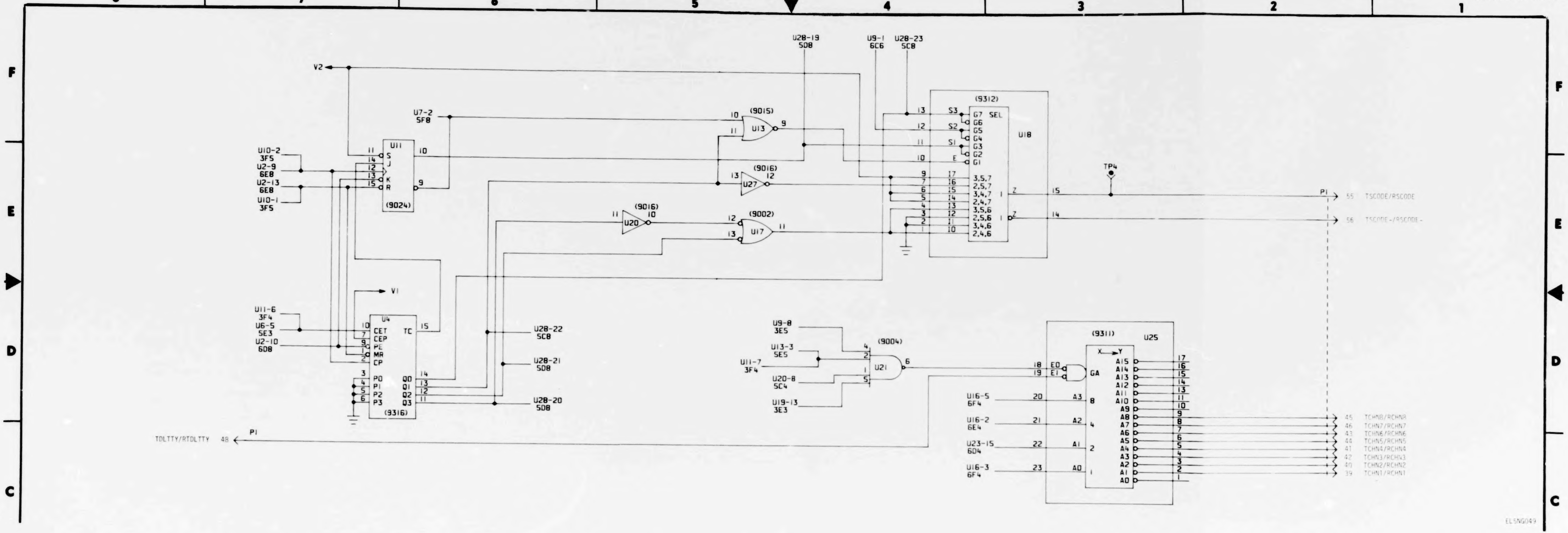

8
7
6
5
4
3
2
1
F
E
D
C
V2
U28-19
5D8
U9-1
6C6
U28-23
5C8
(9312)
U18
13
12
11
10
S3
S2
S1
E
G7
G6
G5
G4
G3
G2
G1
SEL
U7-2
5F8
(9015)
U13
9
(9016)
U27
U10-2
3F5
U2-9
6E8
U2-13
6E8
U10-1
3F5
U11
(9024)
S
J
K
R
TP4
3,5,7
2,5,7
3,4,7
2,4,7
3,5,6
2,5,6
3,4,6
2,4,6
Z
15
14
P1
55
TSCODE/RSCODE
56
TSCODE-/RSCODE-
(9016)
U20
(9002)
U17
V1
U11-6
3F4
U6-5
5E3
U2-10
6D8
U4
CET
CEP
PE
MR
CP
TC
P0
P1
P2
P3
Q0
Q1
Q2
Q3
(9316)
U28-22
5C8
U28-21
5D8
U28-20
5D8
U9-8
3E5
U13-3
5E5
U11-7
3F4
U20-8
5C4
U19-13
3E3
(9004)
U21
6
(9311)
U25
X
Y
E0
E1
GA
U16-5
6F4
U16-2
6E4
U23-15
6D4
U16-3
6F4
A3
A2
A1
A0
8
4
2
1
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
45
TCHN8/RCHN8
46
TCHN7/RCHN7
43
TCHN6/RCHN6
44
TCHN5/RCHN5
41
TCHN4/RCHN4
42
TCHN3/RCHN3
40
TCHN2/RCHN2
39
TCHN1/RCHN1
TDLTTY/RTDLTTY
48
P1
EL5NG049

Figure FO-5. TC card 21A5, schematic diagram (sheet 4 of 6).

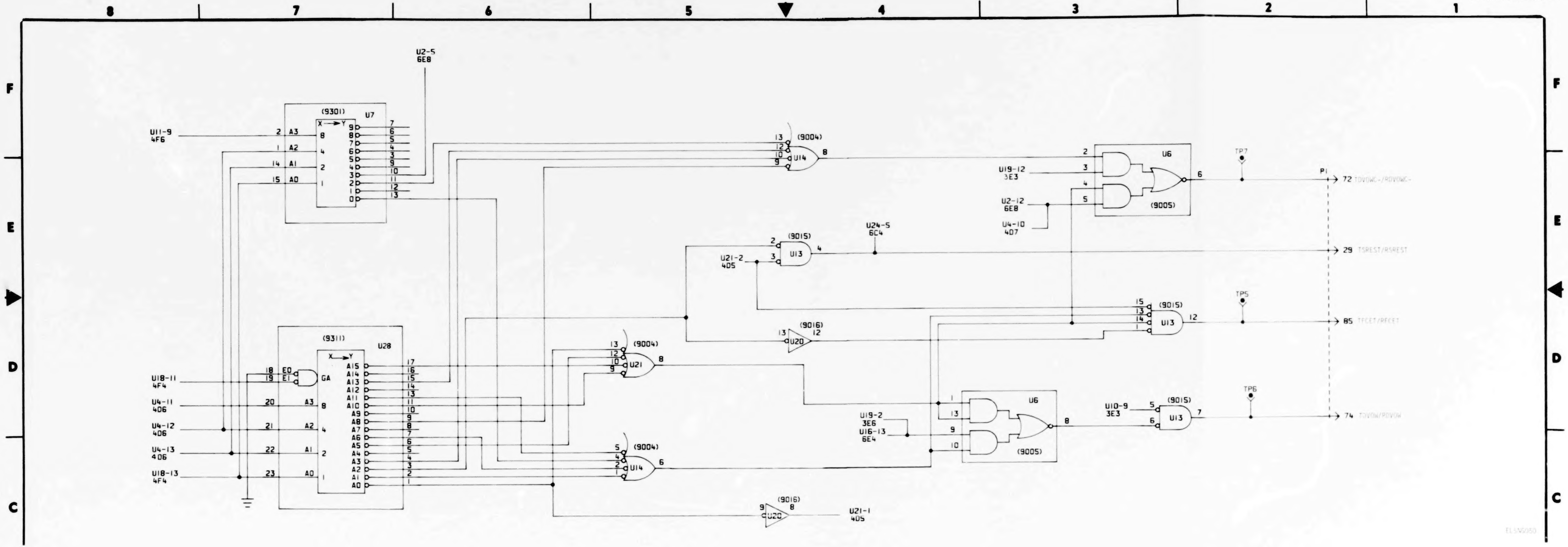

8
7
6
5
4
3
2
1
F
E
D
C
U2-5
6E8
(9301)
U7
X→Y
U11-9
4F6
2 A3 8
1 A2 4
14 A1 2
15 A0 1
9 7
8 6
7 5
6 4
5 3
4 9
3 10
2 11
1 12
0 13
(9004)
U14
13
12
10
9
8
U6
2
3
4
5
6
(9005)
U19-12
3E3
U2-12
6E8
U4-10
4D7
TP7
P1
72 TDVOWC-/RDVOWC-
(9015)
U13
2
3
4
U24-5
6C4
U21-2
4D5
29 TSREST/RSREST
TP5
(9015)
U13
15
13
14
1
12
85 TFCET/RFCET
(9016)
U20
13
12
(9311)
U28
X→Y
U18-11
4F4
18 E0
19 E1
GA
U4-11
4D6
20 A3 8
U4-12
4D6
21 A2 4
U4-13
4D6
22 A1 2
U18-13
4F4
23 A0 1
A15 17
A14 16
A13 15
A12 14
A11 13
A10 11
A9 10
A8 9
A7 8
A6 7
A5 6
A4 5
A3 4
A2 3
A1 2
A0 1
(9004)
U21
13
12
10
9
8
(9004)
U14
5
4
2
1
6
U6
1
13
9
10
8
(9005)
U19-2
3E6
U16-13
6E4
U10-9
3E3
(9015)
U13
5
6
7
TP6
74 TDVOW/RDVOW
(9016)
U20
9
8
U21-1
4D5

Figure FO-5. TC card 21A5, schematic diagram (sheet 5 of 6).

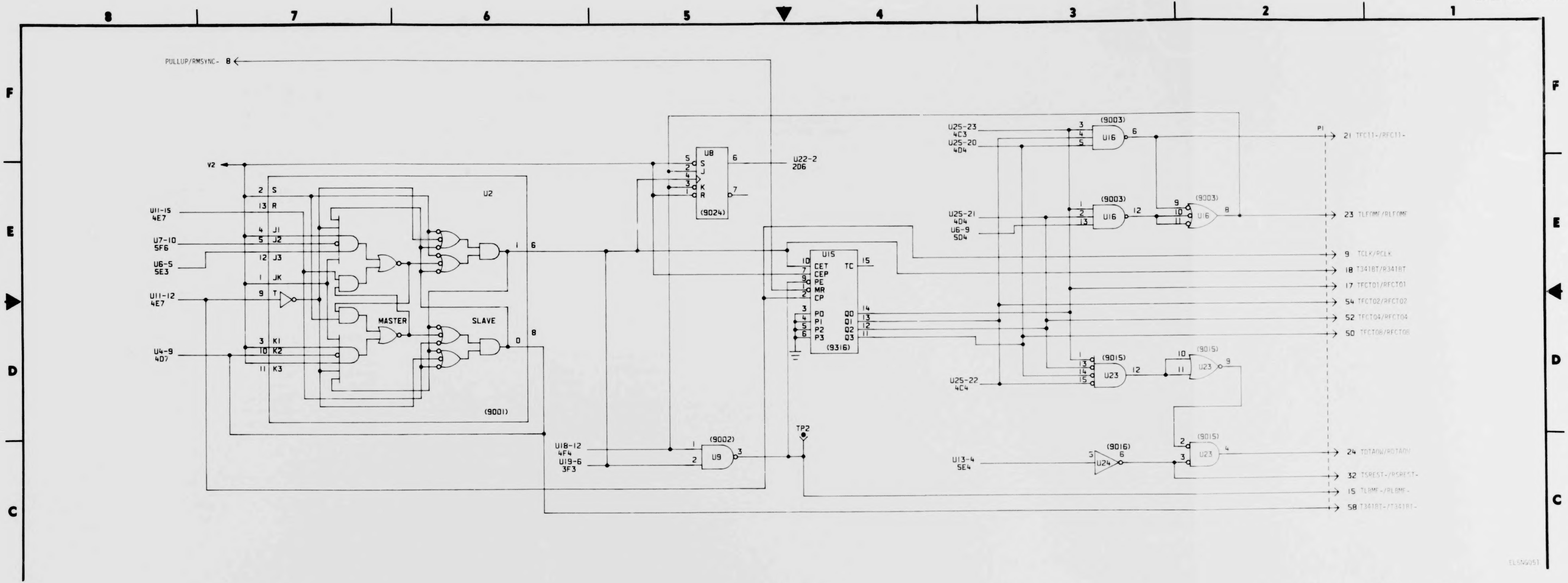
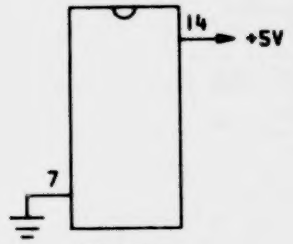
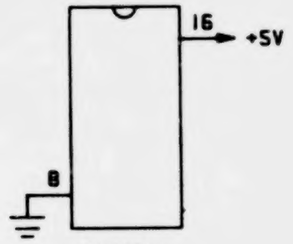

8
7
6
5
4
3
2
1
F
E
D
C
PULLUP/RMSYNC- 8
V2
U11-15
4E7
U7-10
5F6
U6-5
5E3
U11-12
4E7
U4-9
4D7
2 S
13 R
4 J1
5 J2
12 J3
1 JK
9 T
3 K1
10 K2
11 K3
U2
MASTER
SLAVE
1 6
0 8
(9001)
U8
S
J
K
R
(9024)
U22-2
2D6
U15
CET
CEP
PE
MR
CP
TC
P0
P1
P2
P3
Q0
Q1
Q2
Q3
(9316)
U18-12
4F4
U19-6
3F3
U9
(9002)
TP2
U25-23
4C3
U25-20
4D4
U16
(9003)
U25-21
4D4
U6-9
5D4
U25-22
4C4
U23
(9015)
U13-4
5E4
U24
(9016)
P1
21 TFC11-/RFC11-
23 TLFOMF/RLFOMF
9 TCLK/PCLK
18 T341BT/R341BT
17 TFCT01/RFCT01
54 TFCT02/RFCT02
52 TFCT04/RFCT04
50 TFCT08/RFCT08
24 TDTA0W/RDTA0W
32 TSREST-/RSREST-
15 TLBMF-/RLBMF-
58 T341BT-/T341BT-
EL5N6051

Figure FO-5. TC card 21A5, schematic diagram (sheet 6 of 6).



TYPICAL

U16,U18,U35	SM-A-942007	(9016)
U29	SM-A-942001	(9003)
U10,U26,U31	SM-A-942042	(54LS393)



TYPICAL

U15,U22	SM-A-942027	(93L16)
U2,U17,U24,U32	M38510/01404BED	(9309)
U27	M38510/01203BEB	(54123)
U8,U30	SM-A-942028	(93L38)
U9,U25	SM-A-942031	(9338)
U23	SM-A-942018	(9L24)
U34	SM-A-942015	(9024)
U1,U33	SM-A-942013	(9316)

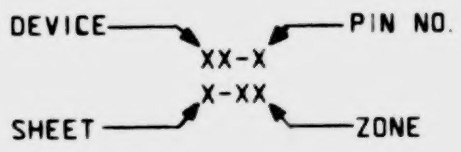
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

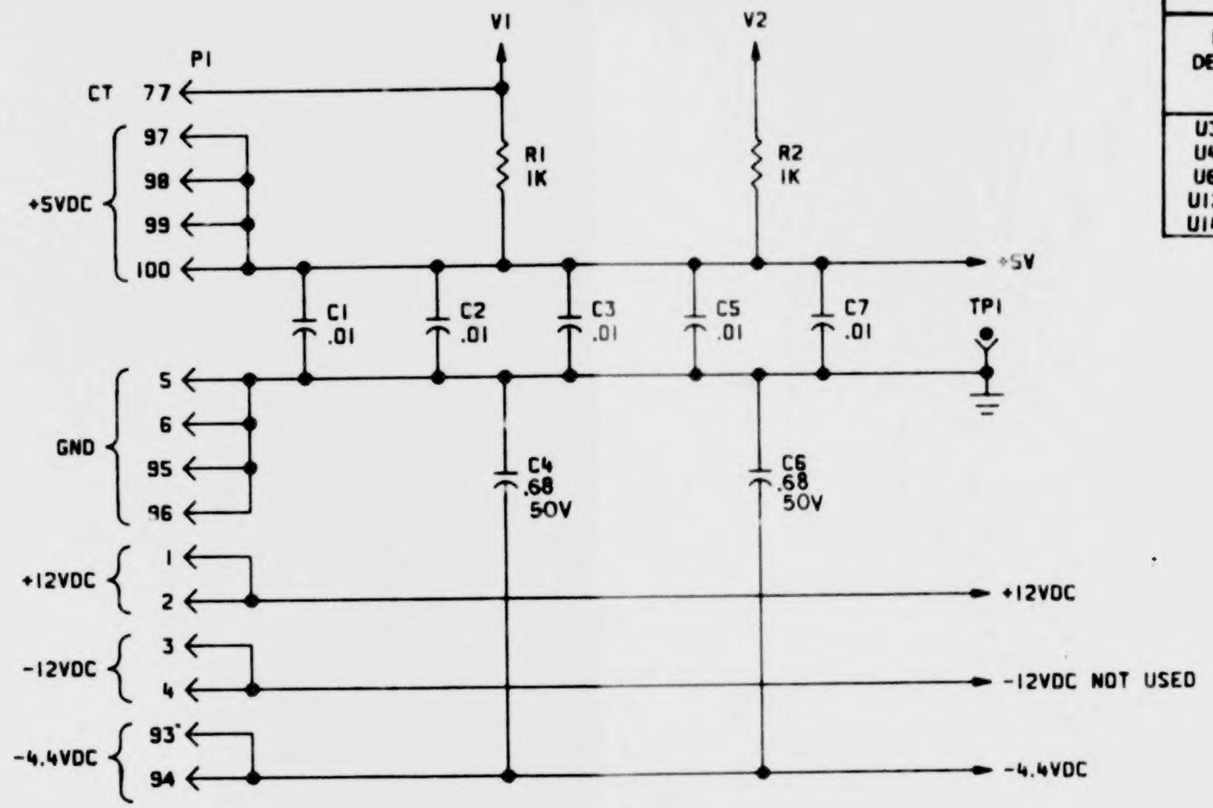
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

4. CIRCUIT CONTINUATION DESTINATION.


DEVICE
PIN NO.
XX-X
X-XX
SHEET
ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

6. VALUE OF RESISTORS R5 AND R12 MAY BE EITHER 5110 OR 3320 OHMS. VALUE SELECTED DURING CARD TEST.


V1
V2
P1
CT 77
+5VDC
97
98
99
100
R1
1K
R2
1K
+5V
C1
.01
C2
.01
C3
.01
C5
.01
C7
.01
TP1
GND
5
6
95
96
C4
.68
50V
C6
.68
50V
+12VDC
1
2
+12VDC
-12VDC
3
4
-12VDC NOT USED
-4.4VDC
93
94
-4.4VDC

HIGHEST REFERENCE DESIGNATION USED	
R48 C30 VR4 U35 TP7	CR5 S2 P1 Q10
REFERENCE DESIGNATIONS NOT USED	
U3 U4 U6 U12 U14	U20 U28

ELSNG052

Figure FO-6. DGP card 21A6, schematic diagram (sheet 1 of 5).

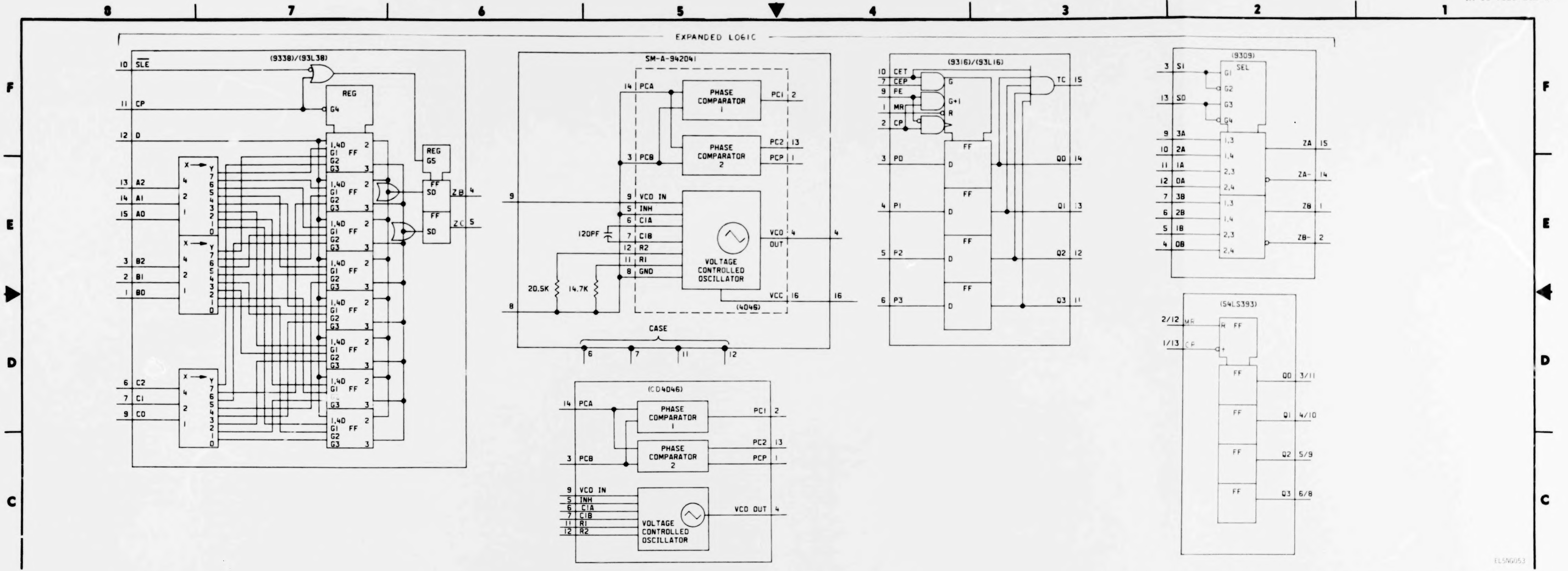

8
7
6
5
4
3
2
1
F
E
D
C
EXPANDED LOGIC
(9338)/(93L38)
10 SLE
11 CP
12 D
REG
G4
13 A2
14 A1
15 A0
3 B2
2 B1
1 B0
6 C2
7 C1
9 C0
X → Y
1,4D
G1 FF
G2
G3
REG
G5
FF
SD
ZB 4
ZC 5
SM-A-942041
14 PCA
3 PCB
PHASE COMPARATOR 1
PHASE COMPARATOR 2
PC1 2
PC2 13
PCP 1
9 VCO IN
5 INH
6 C1A
7 C1B
12 R2
11 R1
8 GND
120PF
20.5K
14.7K
VOLTAGE CONTROLLED OSCILLATOR
VCO OUT 4
VCC 16
(4046)
CASE
6
7
11
12
(CD4046)
(9316)/(93L16)
10 CET
7 CEP
9 PE
1 MR
2 CP
G
G+1
R
TC 15
3 P0
4 P1
5 P2
6 P3
FF
D
Q0 14
Q1 13
Q2 12
Q3 11
(9309)
SEL
3 S1
13 S0
G1
G2
G3
G4
9 3A
10 2A
11 1A
12 0A
7 3B
6 2B
5 1B
4 0B
1,3
1,4
2,3
2,4
ZA 15
ZA- 14
ZB 1
ZB- 2
(54LS393)
2/12 MR
1/13 CP
R FF
Q0 3/11
Q1 4/10
Q2 5/9
Q3 6/8
EL5NG053

Figure FO-6. DGP card 21A6, schematic diagram (sheet 2 of 5).

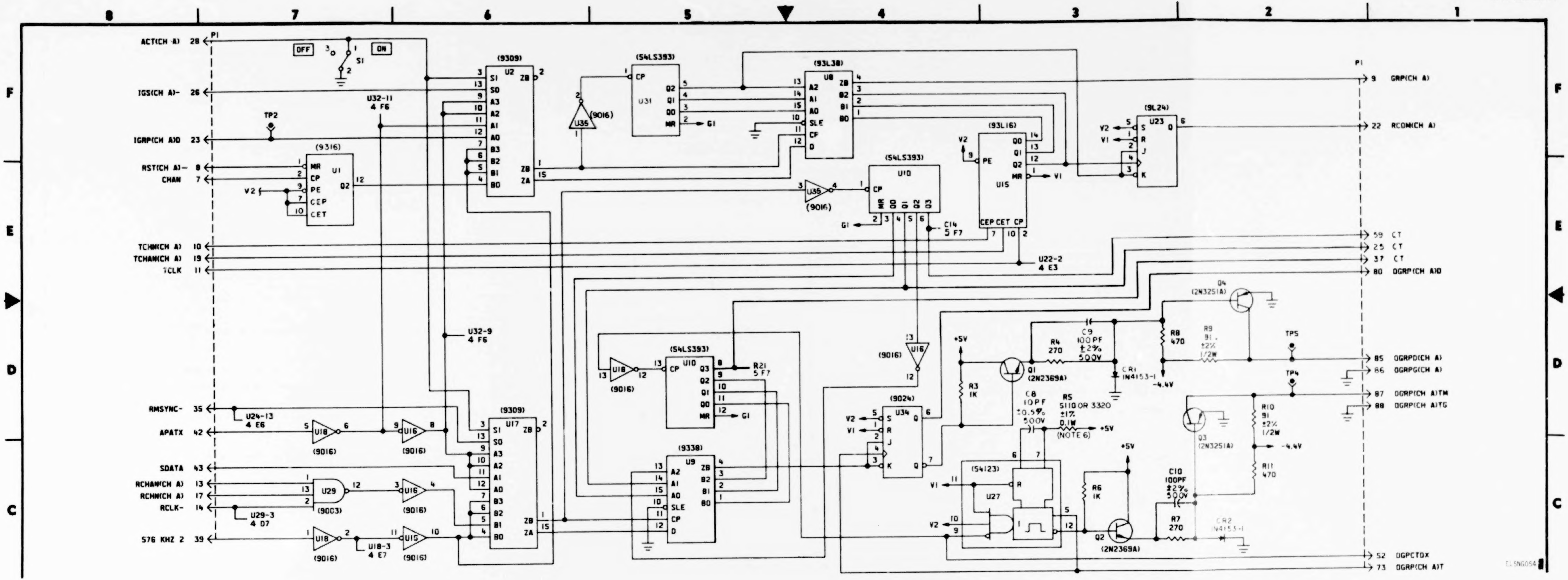

8
7
6
5
4
3
2
1
F
E
D
C
P1
ACT(CH A) 28
IGS(CH A)- 26
IGRP(CH A)O 23
RST(CH A)- 8
CHAN 7
TP2
OFF
ON
S1
(9316)
U1
MR
CP
PE
CEP
CET
Q2
V2
U32-11
4 F6
(9309)
U2
S1
S0
A3
A2
A1
A0
B3
B2
B1
B0
ZB
ZA
U35
(9016)
(54LS393)
U31
CP
Q2
Q1
Q0
MR
G1
(93L38)
U8
A2
A1
A0
SLE
CF
D
ZB
B2
B1
B0
(54LS393)
U10
CP
MR
Q0
Q1
Q2
Q3
C14
5 F7
(93L16)
U15
PE
Q0
Q1
Q2
MR
CEP CET CP
V1
U22-2
4 E3
(9L24)
U23
S
R
J
K
Q
P1
9 GRP(CH A)
22 RCOM(CH A)
59 CT
25 CT
37 CT
80 OGRP(CH A)O
TCHN(CH A) 10
TCHAN(CH A) 19
TCLK 11
U32-9
4 F6
U18
(9016)
(54LS393)
U10
Q3
Q2
Q1
Q0
MR
R21
5 F7
U16
(9016)
(9024)
U34
+5V
Q1
(2N2369A)
R3
1K
R4
270
C9
100PF
±2%
500V
CR1
1N4153-1
-4.4V
R8
470
R9
91
±2%
1/2W
Q4
(2N3251A)
TP5
TP4
85 OGRPD(CH A)
86 OGRPG(CH A)
87 OGRP(CH A)TM
88 OGRP(CH A)TG
C8
10PF
±0.5%
500V
R5
5110 OR 3320
±1%
0.1W
(NOTE 6)
R10
91
±2%
1/2W
Q3
(2N3251A)
R11
470
RMSYNC- 35
U24-13
4 E6
APATX 42
SDATA 43
RCHAN(CH A) 13
RCHN(CH A) 17
RCLK- 14
U29-3
4 D7
576 KHZ 2 39
U18-3
4 E7
U29
(9003)
U16
U18
(9016)
(9309)
U17
(9338)
U9
(54123)
U27
R6
1K
C10
100PF
±2%
500V
R7
270
CR2
1N4153-1
Q2
(2N2369A)
52 DGPCTOX
73 OGRP(CH A)T
EL5NG054

Figure FO-6. DGP card 21A6, schematic diagram (sheet 3 of 5).

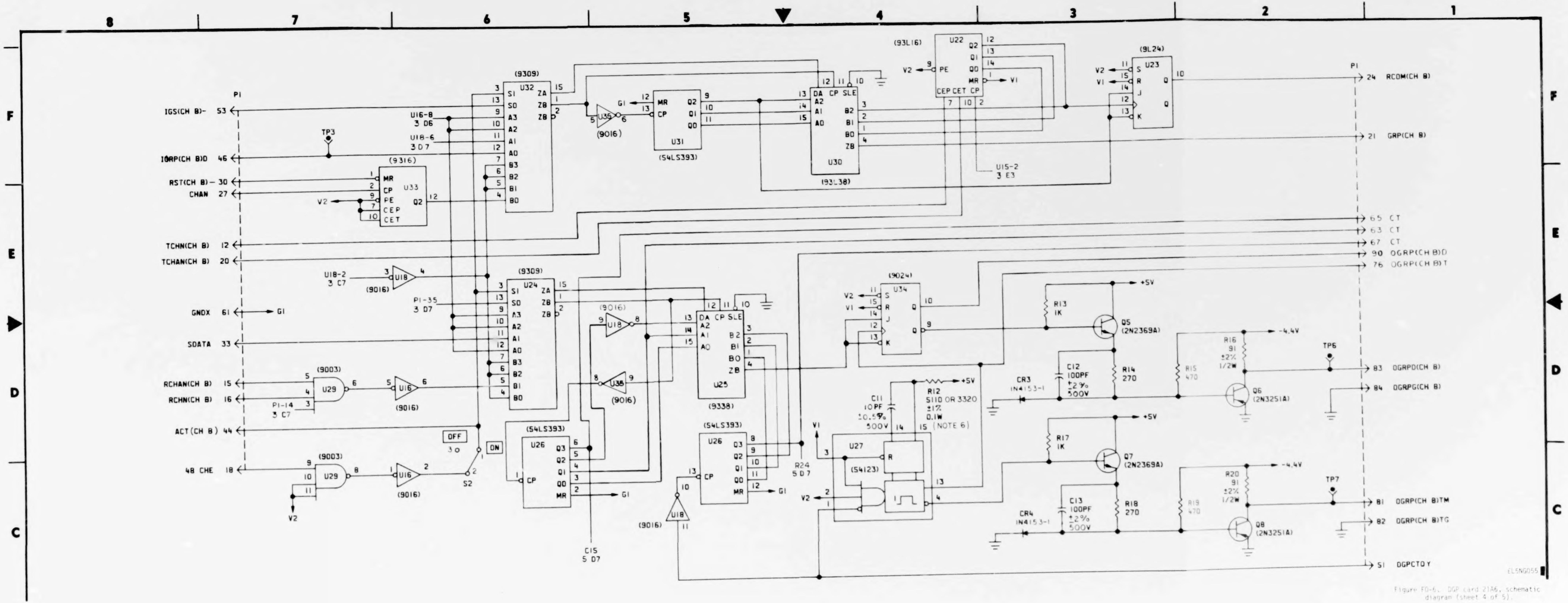

8
7
6
5
4
3
2
1
F
E
D
C
P1
IGS(CH B)- 53
IGRP(CH B)D 46
RST(CH B) - 30
CHAN 27
TCHN(CH B) 12
TCHAN(CH B) 20
GNDX 61
SDATA 33
RCHAN(CH B) 15
RCHN(CH B) 16
ACT(CH B) 44
48 CHE 18
TP3
U16-8
3 D6
U18-6
3 D7
U18-2
3 C7
P1-35
3 D7
P1-14
3 C7
(9316)
U33
MR
CP
PE
CEP
CET
Q2
V2
(9309)
U32
S1
S0
A3
A2
A1
A0
B3
B2
B1
B0
ZA
ZB
U24
(9016)
U35
U18
U16
G1
MR
CP
Q2
Q1
Q0
U31
(54LS393)
DA
CP
SLE
U30
(93L38)
U25
(9338)
(93L16)
U22
PE
CEP CET CP
Q3
Q2
Q1
Q0
MR
V1
U15-2
3 E3
(9L24)
U23
S
R
J
K
Q
24 RCOM(CH B)
21 GRP(CH B)
65 CT
63 CT
67 CT
90 OGRP(CH B)D
76 OGRP(CH B)T
(9024)
U34
+5V
-4.4V
R13
1K
Q5
(2N2369A)
C12
100PF
±2%
500V
CR3
1N4153-1
R14
270
R15
470
R16
91
±2%
1/2W
Q6
(2N3251A)
TP6
83 OGRPD(CH B)
84 OGRPG(CH B)
R17
1K
Q7
(2N2369A)
C13
100PF
±2%
500V
CR4
1N4153-1
R18
270
R19
470
R20
91
±2%
1/2W
Q8
(2N3251A)
TP7
81 OGRP(CH B)TM
82 OGRP(CH B)TG
51 DGPCTOY
(9003)
U29
OFF
3 0
ON
S2
(54LS393)
U26
C15
5 D7
R24
5 D7
C11
10PF
±0.5%
500V
R12
5110 OR 3320
±1%
0.1W
(NOTE 6)
U27
(54123)
EL5NG055

Figure FO-6. DGP card 21A6, schematic diagram (sheet 4 of 5).

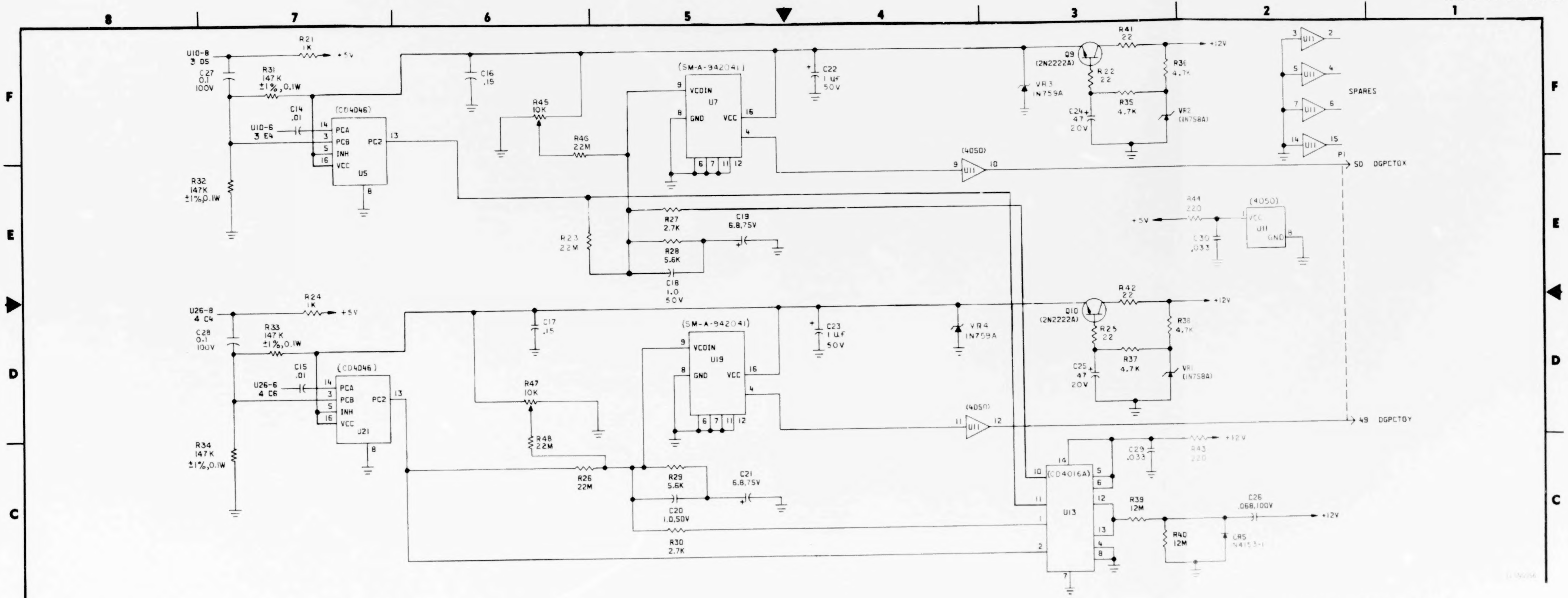

8
7
6
5
4
3
2
1
F
E
D
C
U10-8
3 D5
R21
1K
+5V
C27
0.1
100V
R31
147K
±1%,0.1W
C14
.01
U10-6
3 E4
(CD4046)
PCA
PCB
INH
VCC
PC2
U5
14
3
5
16
13
8
R32
147K
±1%,0.1W
C16
.15
R45
10K
R46
22M
(SM-A-942041)
VCOIN
U7
GND
VCC
9
8
16
4
6
7
11
12
C22
1 uf
50V
VR3
1N759A
Q9
(2N2222A)
R41
22
+12V
R36
4.7K
R22
22
R35
4.7K
C24
47
20V
VR2
(1N758A)
(4050)
U11
9
10
P1
50 DGPCTOX
SPARES
3
2
5
4
7
6
14
15
R23
22M
R27
2.7K
R28
5.6K
C19
6.8,75V
C18
1.0
50V
R44
220
+5V
C30
.033
(4050)
VCC
U11
GND
1
8
U26-8
4 C4
R24
1K
+5V
C28
0.1
100V
R33
147K
±1%,0.1W
C15
.01
U26-6
4 C6
(CD4046)
PCA
PCB
INH
VCC
PC2
U21
R34
147K
±1%,0.1W
C17
.15
R47
10K
R48
22M
(SM-A-942041)
VCOIN
U19
GND
VCC
C23
1 uf
50V
VR4
1N759A
Q10
(2N2222A)
R42
22
+12V
R38
4.7K
R25
22
R37
4.7K
C25
47
20V
VR1
(1N758A)
(4050)
U11
11
12
49 DGPCTOY
R26
22M
R29
5.6K
C21
6.8,75V
C20
1.0,50V
R30
2.7K
C29
.033
R43
220
+12V
(CD4016A)
U13
10
11
1
2
14
5
6
12
13
4
8
7
R39
12M
C26
.068,100V
+12V
R40
12M
CR5
1N4153-1

Figure FO-6. DGP card 21A6, schematic diagram (sheet 5 of 5).

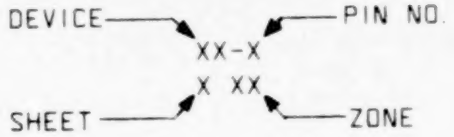
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

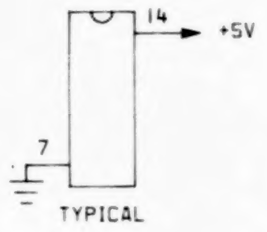
4. CIRCUIT CONTINUATION DESTINATION.


DEVICE
PIN NO.
XX-X
X XX
SHEET
ZONE

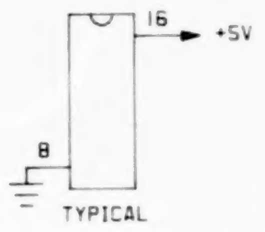
5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

HIGHEST REFERENCE DESIGNATION USED	
C36	P1
CR1	R64
Q1	TP7
VR2	U35
L1	T2

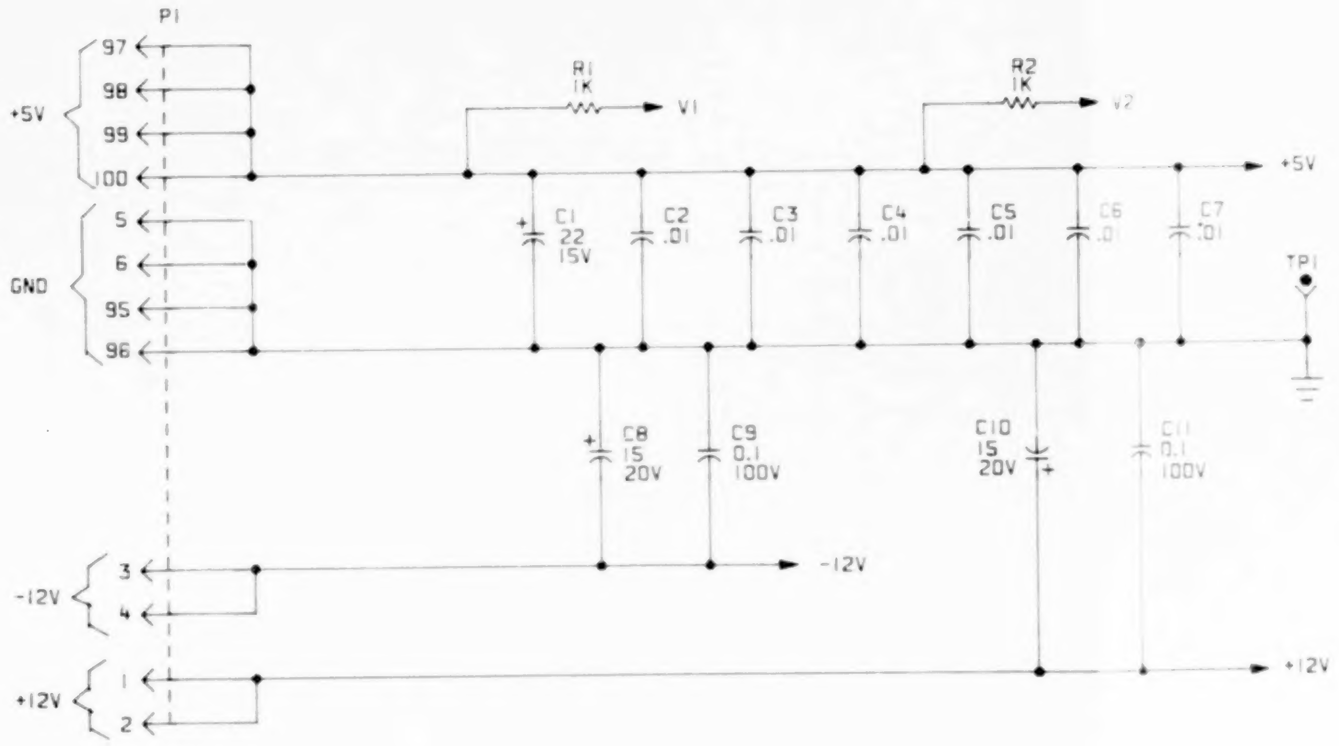
REFERENCE DESIGNATIONS NOT USED
U1,U2,U3,U4,U9 U10,U11,U13,U16 U18,U23,U25,U29 U30,U31,U32


14
+5V
7
TYPICAL

U6,U21	SM-A-942001	(9003)
U5,U19	M38510/00805BCB	(5426)
U34	SM-A-942000	(9002)
U28	SM-A-942007	(9016)
U33	SM-A-942008	(9005)


16
+5V
8
TYPICAL

U7,U14,U20,U27	SM-A-942015	(9024)
U35	SM-A-942006	(9015)


P1
+5V
97
98
99
100
GND
5
6
95
96
-12V
3
4
+12V
1
2
R1
1K
V1
R2
1K
V2
+5V
C1
22
15V
C2
.01
C3
.01
C4
.01
C5
.01
C6
.01
C7
.01
TP1
C8
15
20V
C9
0.1
100V
C10
15
20V
C11
0.1
100V
-12V
+12V

EL5NG057

Figure FO-7. DVOW card 21A11, schematic diagram (sheet 1 of 5).

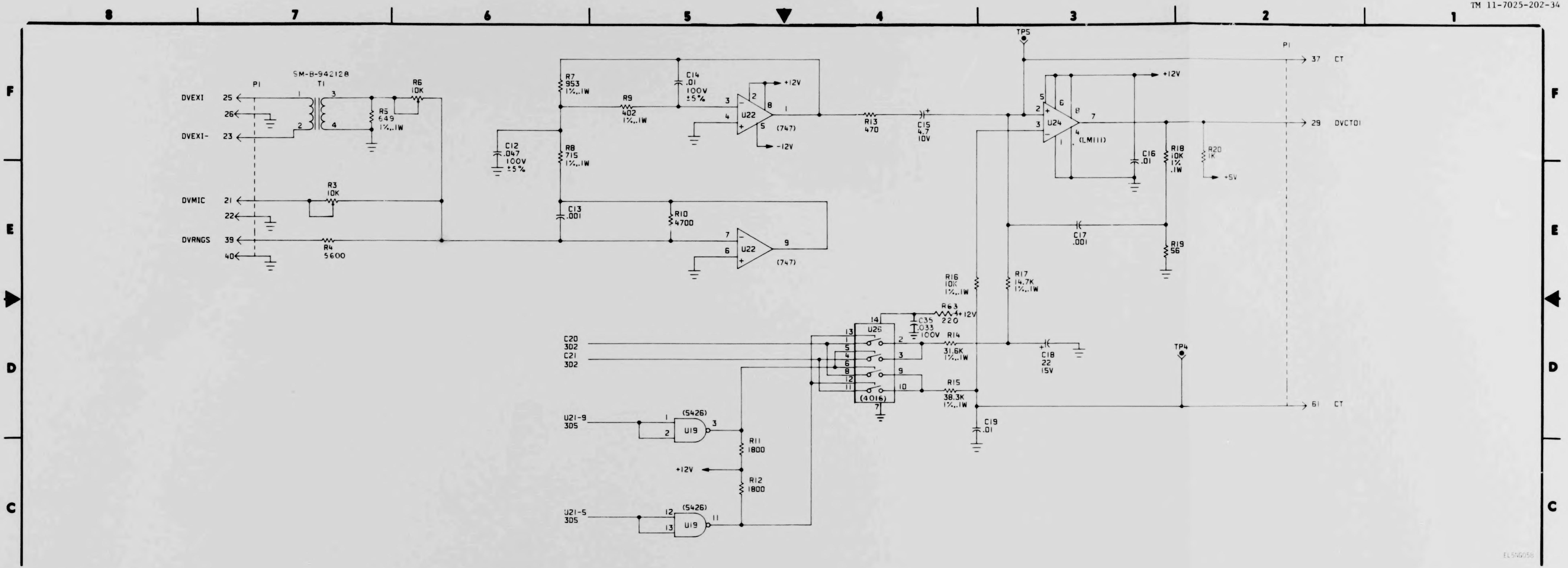

8
7
6
5
4
3
2
1
F
E
D
C
SM-B-942128
P1
T1
DVEXI 25
26
DVEXI- 23
R6 10K
R5 649 1%,.1W
DVMIC 21
22
R3 10K
DVRNGS 39
40
R4 5600
R7 953 1%,.1W
C14 .01 100V ±5%
R9 402 1%,.1W
C12 .047 100V ±5%
R8 715 1%,.1W
U22
(747)
+12V
-12V
C13 .001
R10 4700
R13 470
C15 4.7 10V
TP5
U24
(LM111)
+12V
C16 .01
R18 10K 1% .1W
R20 1K
+5V
37 CT
29 DVCT01
C17 .001
R19 56
R16 10K 1%,.1W
R17 14.7K 1%,.1W
R63 220
+12V
C35 .033 100V
U26
(4016)
R14 31.6K 1%,.1W
R15 38.3K 1%,.1W
C18 22 15V
TP4
61 CT
C19 .01
C20 3D2
C21 3D2
U21-9 3D5
U21-5 3D5
(5426)
U19
R11 1800
R12 1800
+12V
EL5NG058

Figure FO-7. DVOW card 21A11, schematic diagram (sheet 2 of 5).

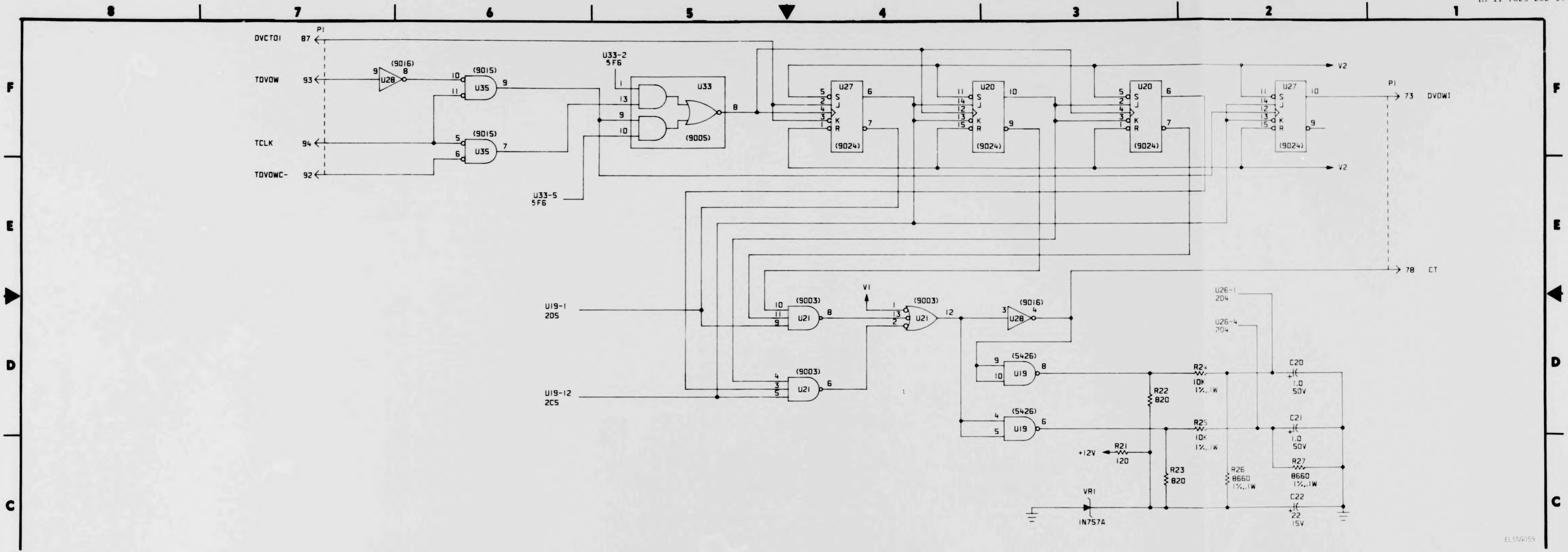

8
7
6
5
4
3
2
1
F
E
D
C
P1
DVCT01
87
TDVOW
93
TCLK
94
TDVOWC-
92
U28
(9016)
U35
(9015)
U33-2
5F6
U33-5
5F6
U33
(9005)
U27
U20
(9024)
V2
P1
73
DVOWI
78
CT
U19-1
2D5
U19-12
2C5
U21
(9003)
V1
U28
(9016)
U19
(5426)
U26-1
2D4
U26-4
2D4
R24
10K
1%,.1W
R25
10K
1%,.1W
R22
820
R23
820
R21
120
+12V
R26
8660
1%,.1W
R27
8660
1%,.1W
C20
1.0
50V
C21
1.0
50V
C22
22
15V
VR1
IN757A
EL5NG059

Figure FO-7. DVOW card 21A11, schematic diagram (sheet 3 of 5).

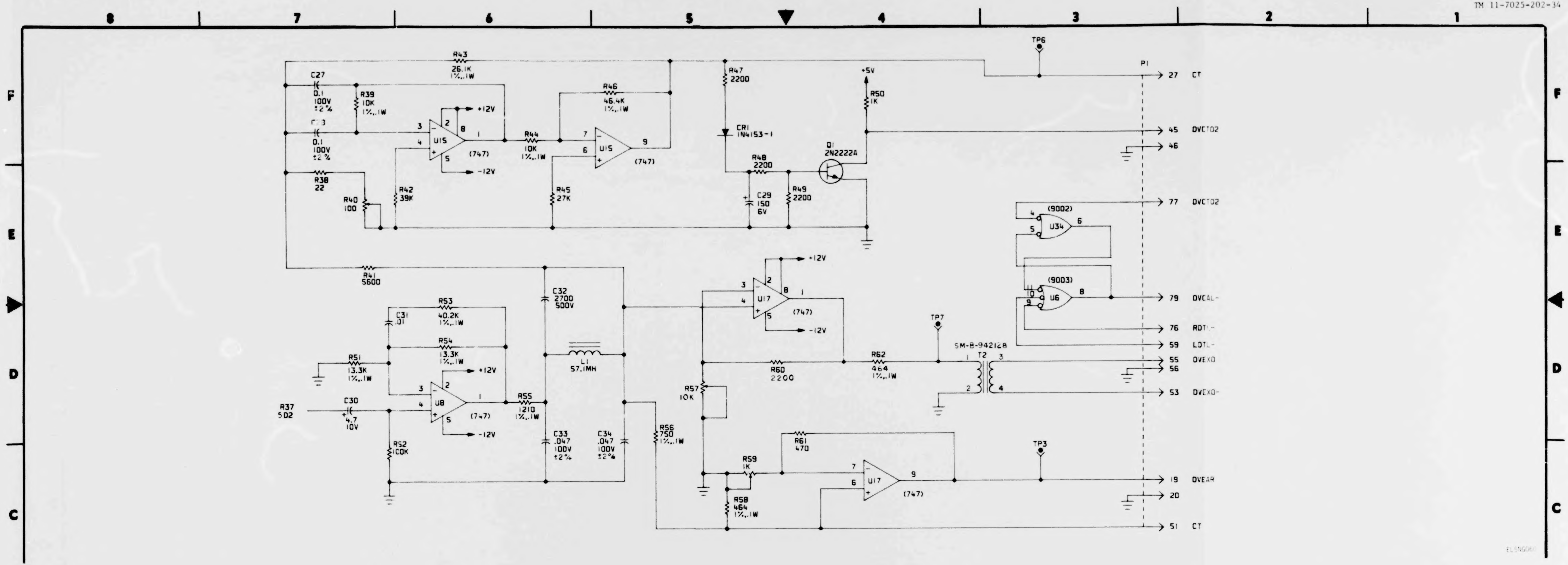

8
7
6
5
4
3
2
1
F
E
D
C
R43
26.1K
1%,.1W
C27
0.1
100V
±2%
R39
10K
1%,.1W
+12V
C28
0.1
100V
±2%
3
2
8
1
4
U15
5
(747)
-12V
R44
10K
1%,.1W
R46
46.4K
1%,.1W
7
6
U15
9
(747)
R38
22
R40
100
R42
39K
R45
27K
R47
2200
CR1
1N4153-1
+5V
R50
1K
Q1
2N2222A
R48
2200
C29
150
6V
R49
2200
TP6
P1
27 CT
45 DVCT02
46
77 DVCT02
(9002)
U34
(9003)
U6
79 DVCAL-
76 RDTL-
59 LDTL-
55 DVEXO
56
53 DVEXO-
R41
5600
C32
2700
500V
C31
.01
R53
40.2K
1%,.1W
R54
13.3K
1%,.1W
R51
13.3K
1%,.1W
U8
(747)
R37
502
C30
4.7
10V
R52
100K
R55
1210
1%,.1W
L1
57.1MH
C33
.047
100V
±2%
C34
.047
100V
±2%
R56
750
1%,.1W
U17
(747)
+12V
-12V
R57
10K
R60
2200
R62
464
1%,.1W
TP7
SM-B-942128
T2
R61
470
R59
1K
R58
464
1%,.1W
U17
(747)
TP3
19 DVEAR
20
51 CT
EL5NG060

Figure FO-7. DVOW card 2lA11, schematic diagram (sheet 4 of 5).

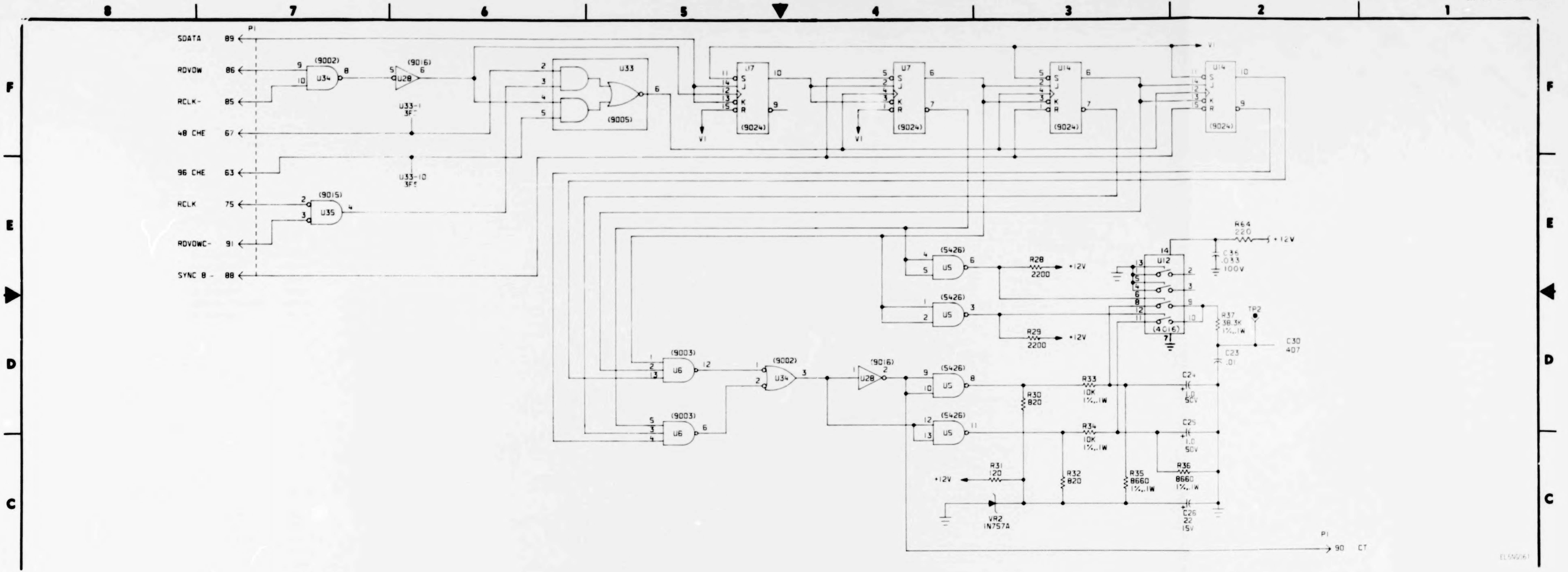
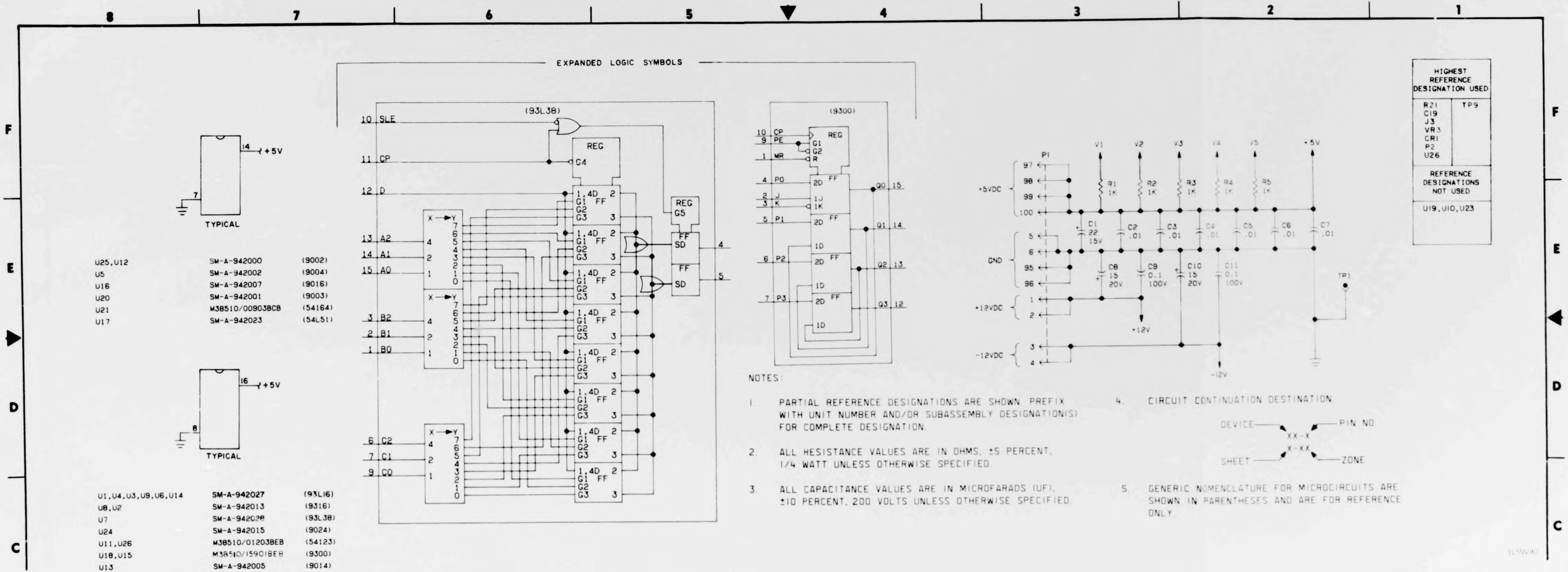

8
7
6
5
4
3
2
1
F
E
D
C
P1
SDATA 89
RDVOW 86
RCLK- 85
48 CHE 67
96 CHE 63
RCLK 75
RDVOWC- 91
SYNC 8 - 88
(9002) U34
(9016) U28
U33 (9005)
U33-1 3F5
U33-10 3F5
(9015) U35
U7 (9024)
U14 (9024)
V1
(5426) U5
(9003) U6
U12 (4016)
R64 220
+12V
C36 .033 100V
R28 2200
R29 2200
R37 38.3K 1%,.1W
TP2
C30 407
C23 .01
R33 10K 1%,.1W
R34 10K 1%,.1W
R30 820
R32 820
R31 120
R35 8660 1%,.1W
R36 8660 1%,.1W
C24 1.0 50V
C25 1.0 50V
C26 22 15V
VR2 1N757A
90 CT
EL5NG067

Figure FO-7. DVOW card 21A11, schematic diagram (sheet 5 of 5).


8
7
6
5
4
3
2
1
F
E
D
C
14
+5V
7
TYPICAL
16
+5V
8
TYPICAL
EXPANDED LOGIC SYMBOLS
(93L38)
10 SLE
11 CP
C4
REG
12 D
1,4D
G1 FF
G2
G3
13 A2
14 A1
15 A0
X → Y
3 B2
2 B1
1 B0
6 C2
7 C1
9 C0
REG
G5
FF
SD
4
5
(9300)
10 CP
9 PE
1 MR
G1
G2
R
4 P0
2D
2 J
3 K
1J
1K
5 P1
1D
6 P2
7 P3
Q0 15
Q1 14
Q2 13
Q3 12
P1
97
98
99
100
+5VDC
5
6
95
96
GND
1
2
+12VDC
3
4
-12VDC
V1
V2
V3
V4
V5
+5V
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
C1 22 15V
C2 .01
C3 .01
C4 .01
C5 .01
C6 .01
C7 .01
C8 15 20V
C9 0.1 100V
C10 15 20V
C11 0.1 100V
+12V
-12V
TP1
EL5N6062

U25,U12	SM-A-942000	(9002)
U5	SM-A-942002	(9004)
U16	SM-A-942007	(9016)
U20	SM-A-942001	(9003)
U21	M38510/00903BCB	(54164)
U17	SM-A-942023	(54L51)

U1,U4,U3,U9,U6,U14	SM-A-942027	(93L16)
U8,U2	SM-A-942013	(9316)
U7	SM-A-942028	(93L38)
U24	SM-A-942015	(9024)
U11,U26	M38510/01203BEB	(54123)
U18,U15	M38510/15901BEB	(9300)
U13	SM-A-942005	(9014)

HIGHEST REFERENCE DESIGNATION USED	
R21 C19 J3 VR3 CR1 P2 U26	TP9
REFERENCE DESIGNATIONS NOT USED	
U19,U10,U23	

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

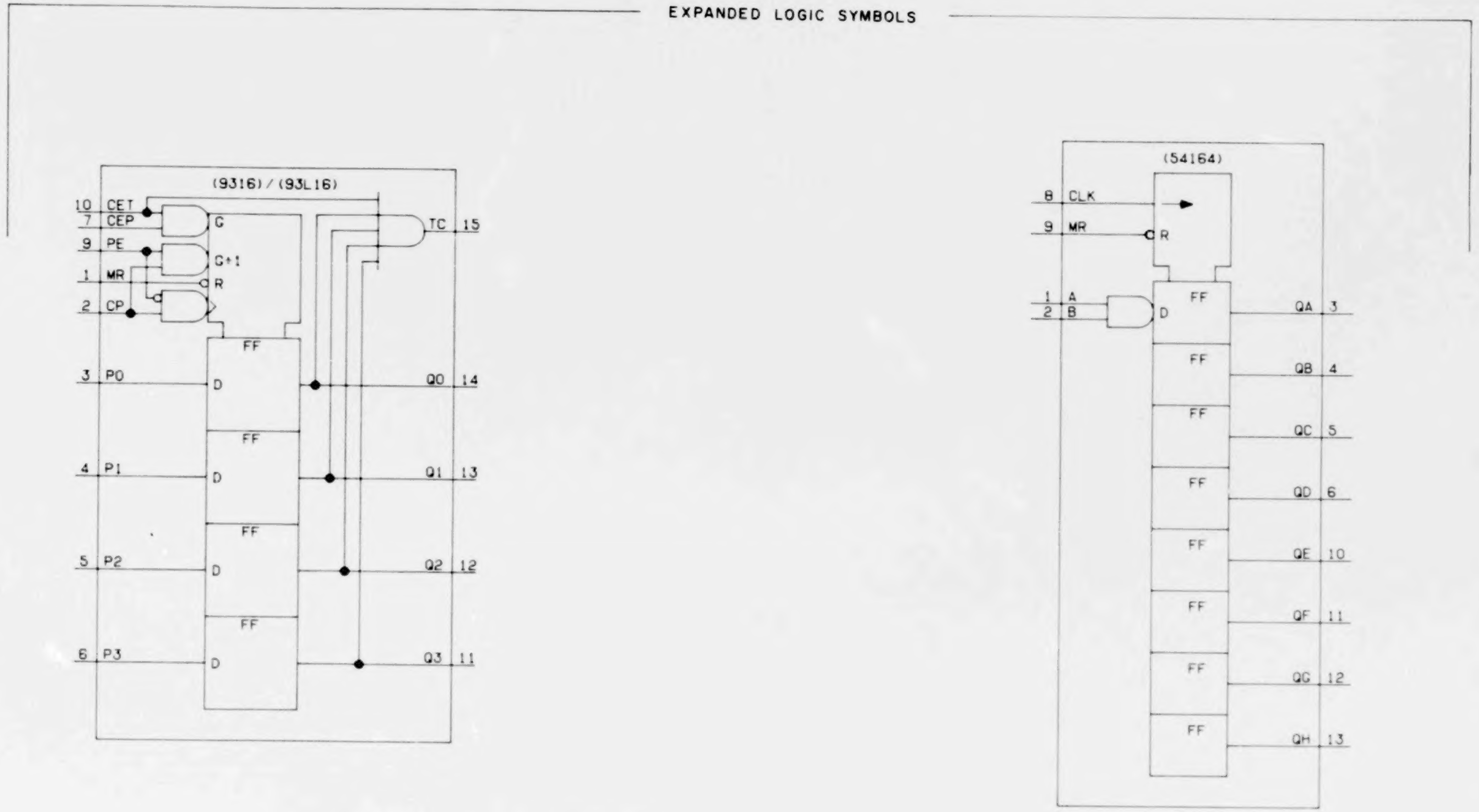
4. CIRCUIT CONTINUATION DESTINATION

DEVICE — XX-X — PIN NO
SHEET — X-XX — ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

Figure FO-8. DDOW encoder card 21A3, schematic diagram (sheet 1 of 5).

EXPANDED LOGIC SYMBOLS


(9316)/(93L16)
10 CET
7 CEP
9 PE
1 MR
2 CP
G
G+1
R
FF
D
TC 15
3 P0
4 P1
5 P2
6 P3
Q0 14
Q1 13
Q2 12
Q3 11
(54164)
8 CLK
9 MR
R
1 A
2 B
D
FF
QA 3
QB 4
QC 5
QD 6
QE 10
QF 11
QG 12
QH 13

EL5NG063

Figure FO-8. DDOW encoder card 21A3, schematic diagram (sheet 2 of 5).

Figure FO-8. DDOW encoder card 21A3, schematic diagram (sheet 2 of 5).

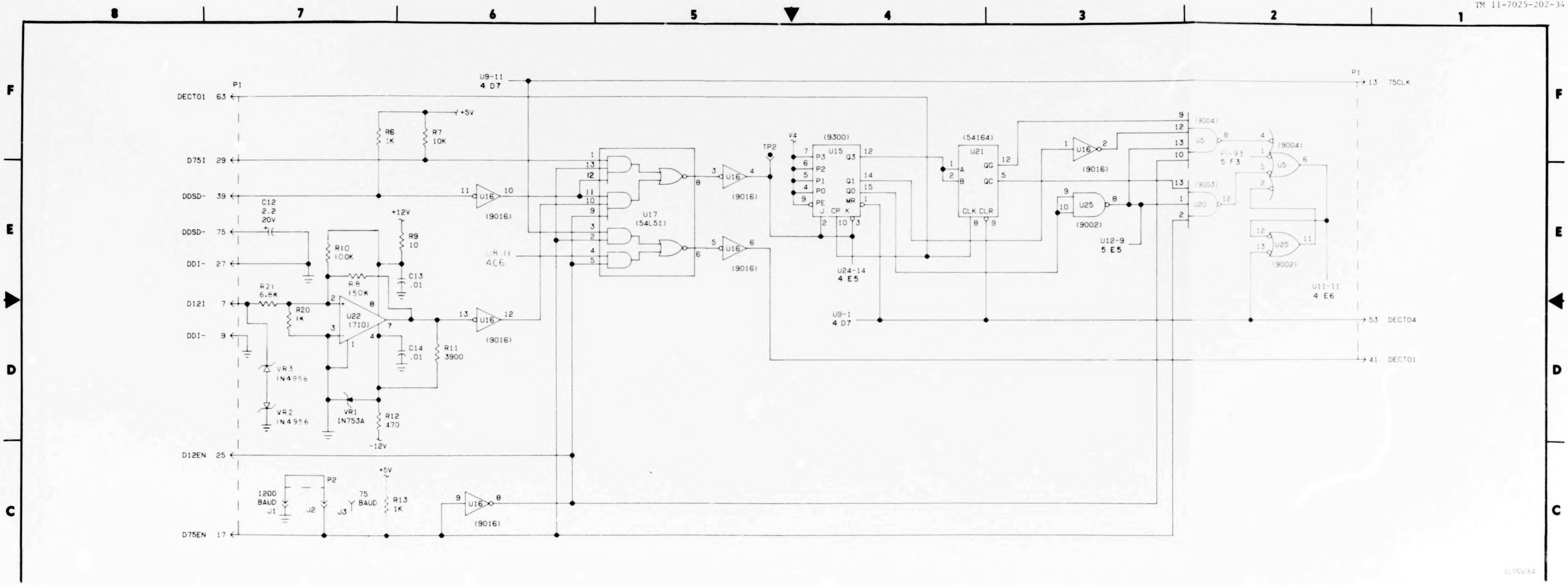

8
7
6
5
4
3
2
1
F
E
D
C
P1
DECT01 63
D75I 29
DDSD- 39
DDSD- 75
DDI- 27
D12I 7
DDI- 9
D12EN 25
D75EN 17
U9-11
4 D7
+5V
R6
1K
R7
10K
C12
2.2
20V
+12V
R9
10
R10
100K
R8
150K
C13
.01
R21
6.8K
R20
1K
U22
(710)
C14
.01
R11
3900
VR3
IN4956
VR2
IN4956
VR1
IN753A
R12
470
-12V
U16
(9016)
U8-11
4C6
U17
(54L51)
1200
BAUD
J1
J2
P2
J3
75
BAUD
R13
1K
+5V
TP2
V4
(9300)
U15
P3
P2
P1
P0
PE
Q3
Q1
Q0
MR
J
CP
K
U24-14
4 E5
(54164)
U21
A
B
QG
QC
CLK
CLR
U9-1
4 D7
U25
(9002)
U12-9
5 E5
(9004)
U5
P1-93
5 F3
(9003)
U20
U11-11
4 E6
P1
13 75CLK
53 DECT04
41 DECT01
EL5N6064

Figure FO-8. DDOW encoder card 21A3, schematic diagram (sheet 3 of 5).

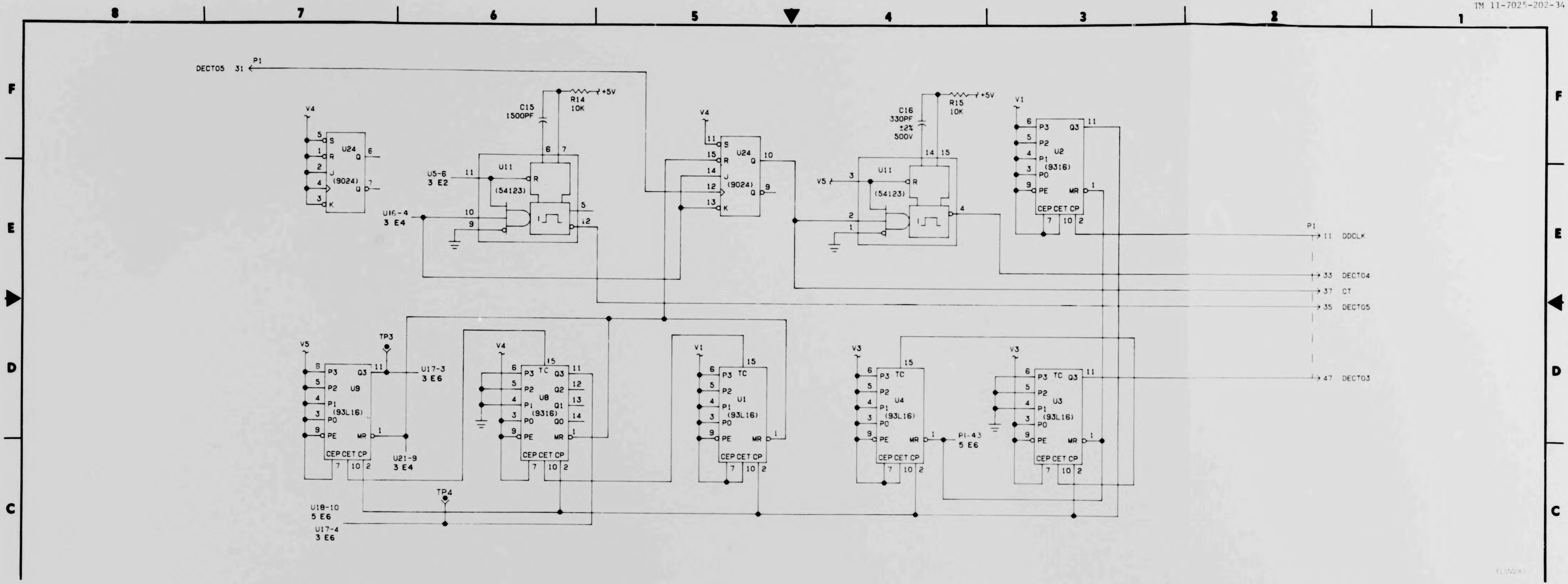

8
7
6
5
4
3
2
1
F
E
D
C
P1
DECTO5 31
V4
U24
(9024)
S
R
J
K
Q
C15
1500PF
R14
10K
+5V
U11
(54123)
U5-6
3 E2
U16-4
3 E4
U24
(9024)
C16
330PF
±2%
500V
R15
10K
V5
V1
U2
(9316)
P3
P2
P1
P0
PE
Q3
MR
CEP CET CP
P1
11 DDCLK
33 DECTO4
37 CT
35 DECTO5
47 DECTO3
TP3
V5
U9
(93L16)
U17-3
3 E6
U21-9
3 E4
V4
U8
(9316)
TC
Q2
Q1
Q0
V1
U1
(93L16)
V3
U4
(93L16)
P1-43
5 E6
V3
U3
(93L16)
TP4
U18-10
5 E6
U17-4
3 E6

Figure FO-8. DDOW encoder card 21A3, schematic diagram (sheet 4 of 5).

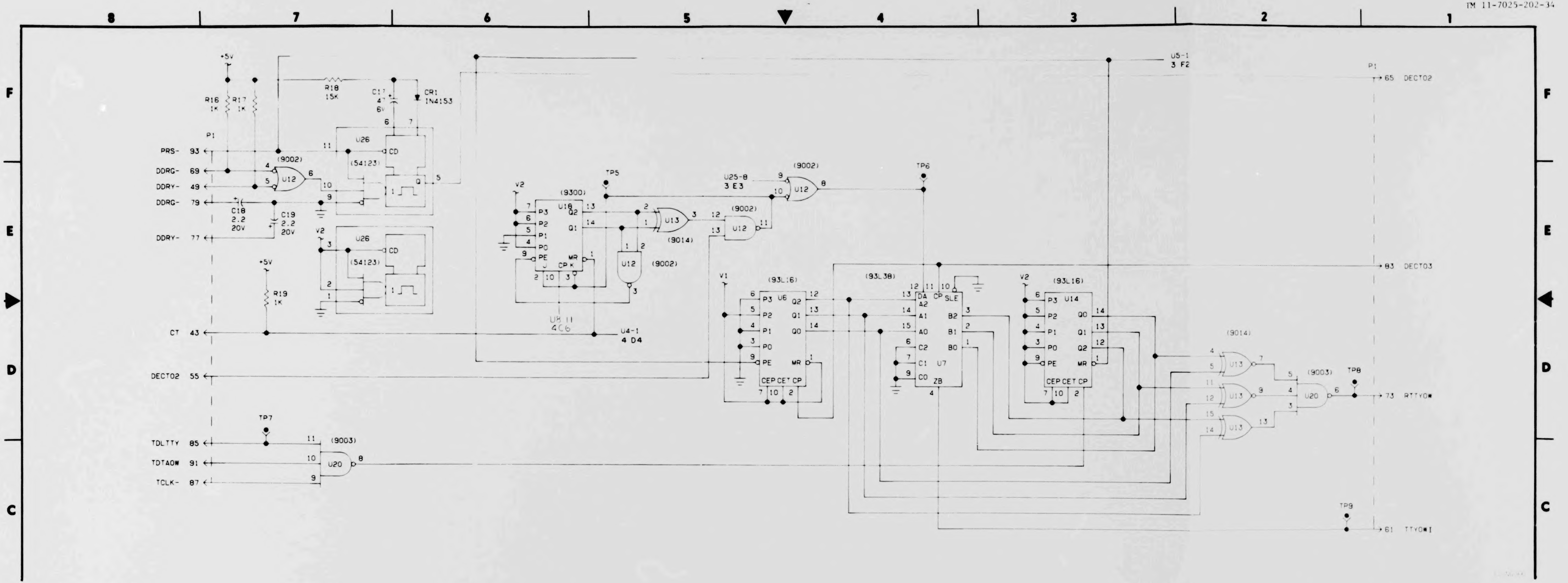
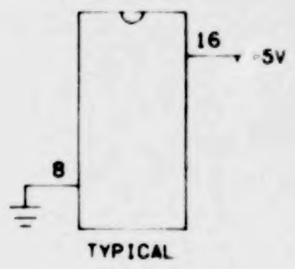
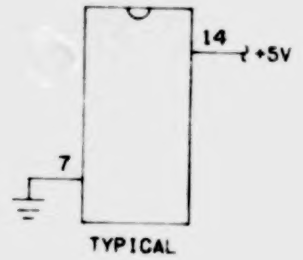

8
7
6
5
4
3
2
1
F
E
D
C
+5V
R16
1K
R17
1K
R18
15K
C17
47
6V
CR1
1N4153
P1
PRS- 93
DDRG- 69
DDRY- 49
DDRG- 79
DDRY- 77
C18
2.2
20V
C19
2.2
20V
(9002)
U12
U26
(54123)
CD
Q
U5-1
3 F2
V2
(9300)
U16
P3
P2
P1
P0
PE
Q2
Q1
MR
CP K
J
TP5
U13
(9014)
(9002)
U25-8
3 E3
TP6
+5V
R19
1K
CT 43
U8 11
4C6
U4-1
4 D4
DECTO2 55
V1
(93L16)
U6
CEP CET CP
(93L38)
DA
A2
A1
A0
C2
C1
C0
CP
SLE
B2
B1
B0
U7
ZB
U14
Q0
(9003)
U20
TP7
TDLTTY 85
TDTAOW 91
TCLK- 87
TP8
TP9
P1
65 DECTO2
83 DECTO3
73 RTTYOW
61 TTYOWI

Figure FO-8. DDOW encoder card 21A3, schematic diagram (sheet 5 of 5).

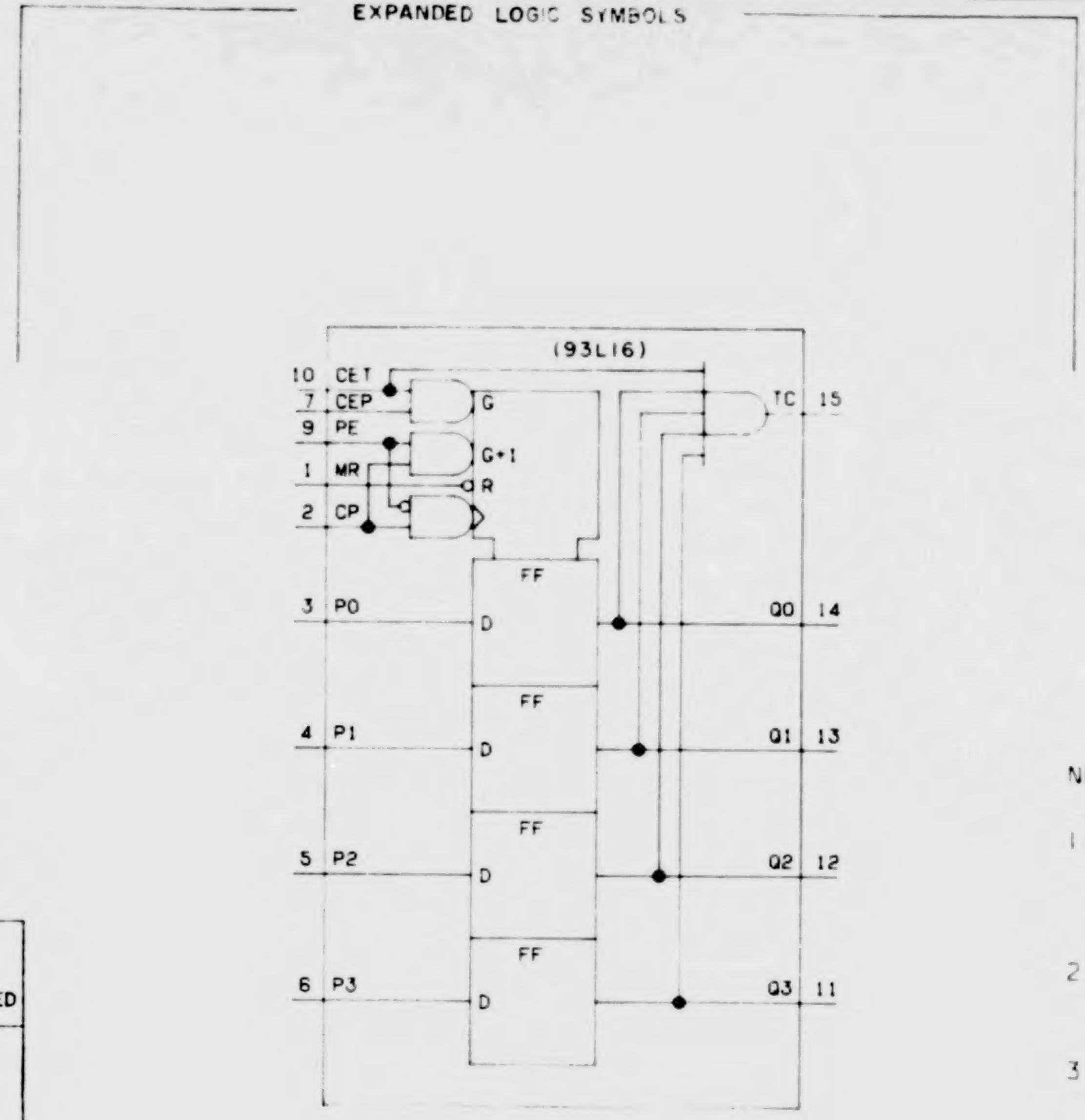

16
+5V
8
TYPICAL

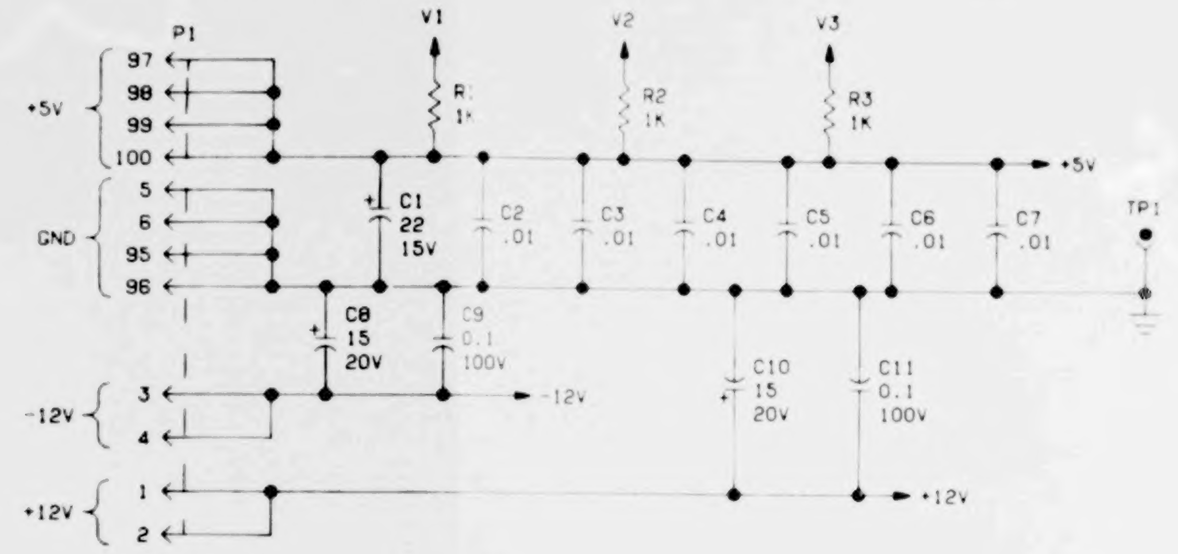
U10	M38510/01203BEB	(54123)
U1,U2,U8,U5,U15,U7	SM-A-942027	(93L16)
U4,U14	SM-A-942015	(9024)
U6	SM-A-942031	(9338)
U11	SM-A-942006	(9015)
U9	SM-A-942025	(54191)


14
+5V
7
TYPICAL

U20	SM-A-942000	(9002)
U21	SM-A-942003	(9007)
U18, U22	SM-A-942001	(9003)
U3	SM-A-942007	(9016)
U12	M38510/00903BCB	(54164)
U13	SM-A-942002	(9004)

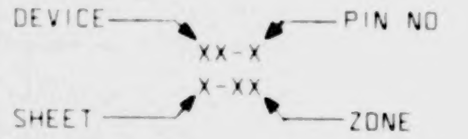
HIGHEST REFERENCE DESIGNATION USED	
C17 R12 CR1 VR4 U26 TP9 P1	Q1
REFERENCE DESIGNATIONS NOT USED	
U16,U17,U19. U23-U25 C16	


EXPANDED LOGIC SYMBOLS
(93L16)
10 CET
7 CEP
9 PE
1 MR
2 CP
G
G+1
R
TC 15
3 P0
4 P1
5 P2
6 P3
FF
D
Q0 14
Q1 13
Q2 12
Q3 11


P1
+5V
97
98
99
100
GND
5
6
95
96
-12V
3
4
+12V
1
2
V1
V2
V3
R1 1K
R2 1K
R3 1K
+5V
C1 22 15V
C2 .01
C3 .01
C4 .01
C5 .01
C6 .01
C7 .01
TP1
C8 15 20V
C9 0.1 100V
-12V
C10 15 20V
C11 0.1 100V
+12V

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.
4. CIRCUIT CONTINUATION DESTINATION


DEVICE
PIN NO
XX-X
X-XX
SHEET
ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

Figure FO-9. DDOW decoder card 21A8, schematic diagram (sheet 1 of 4).

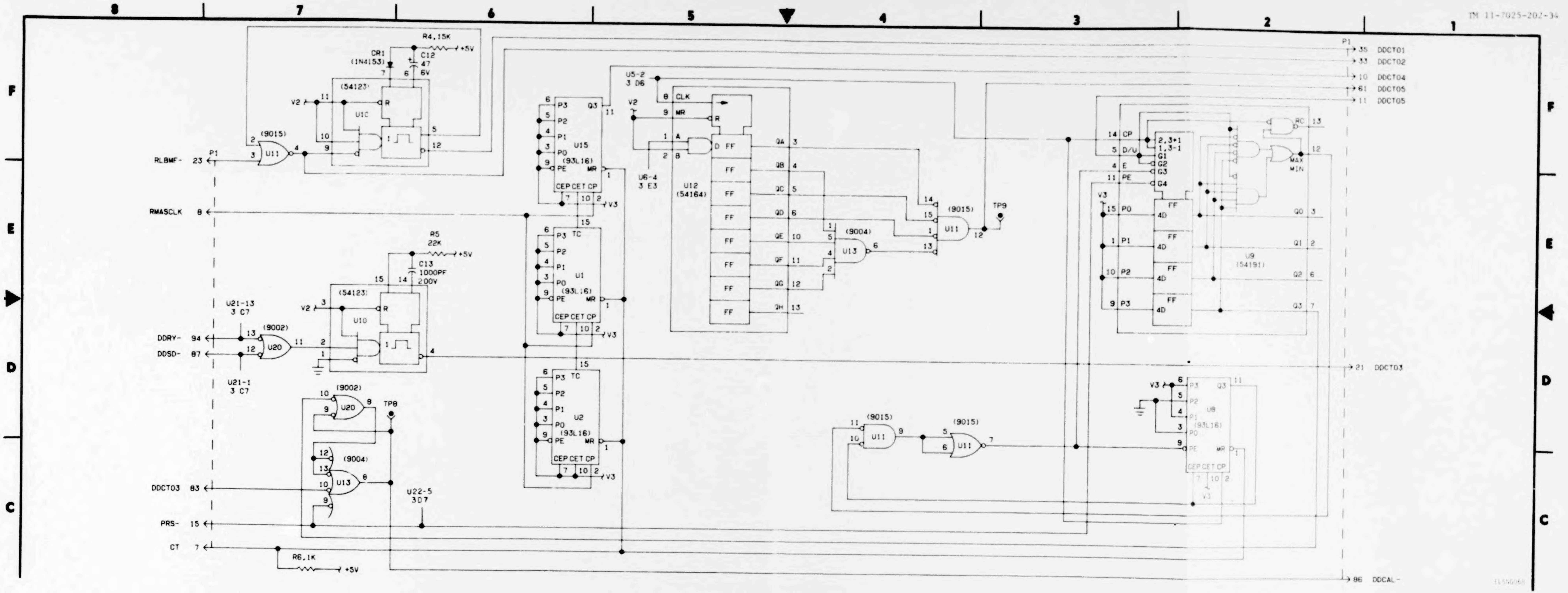
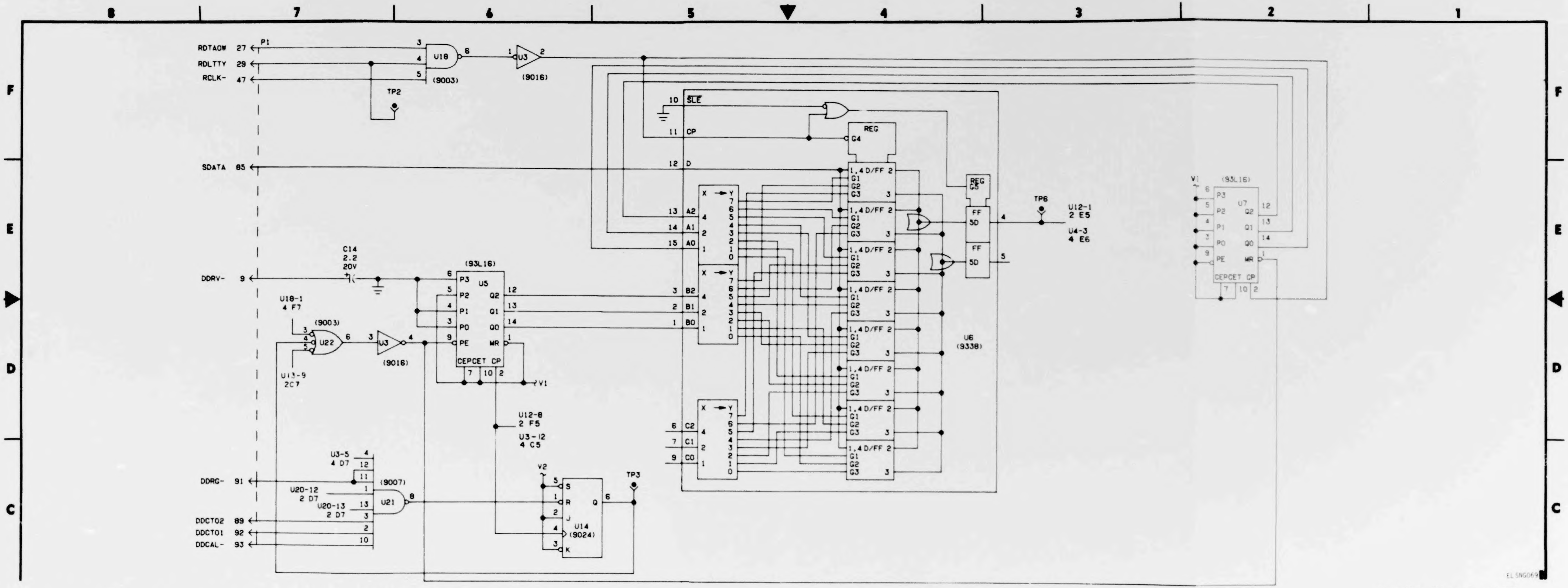

8
7
6
5
4
3
2
1
F
E
D
C
R4,15K
+5V
CR1
(1N4153)
C12
47
6V
(54123)
U1C
V2
RLBMF-
23
P1
(9015)
U11
P3
P2
P1
P0
U15
(93L16)
PE
MR
CEP CET CP
Q3
V3
RMASCLK
TC
U1
R5
22K
C13
1000PF
200V
U10
U21-13
3 C7
DDRY-
94
DDSD-
87
(9002)
U20
U21-1
3 C7
U2
TP8
(9004)
U13
DDCTO3
83
U22-5
3D7
PRS-
15
CT
7
R6,1K
U5-2
3 D6
CLK
MR
U6-4
3 E3
U12
(54164)
FF
QA
QB
QC
QD
QE
QF
QG
QH
TP9
DDCTO1
35
DDCTO2
33
DDCTO4
10
DDCTO5
61
DDCTO5
11
CP
D/U
E
PE
2,3+1
1,3-1
G1
G2
G3
G4
4D
U9
(54191)
RC
13
MAX
MIN
Q0
Q1
Q2
Q3
21
DDCTO3
U8
(93L16)
86
DDCAL-

Figure FO-9. DDOW decoder card 21A8, schematic diagram (sheet 2 of 4).



8
7
6
5
4
3
2
1
F
E
D
C
RDTAOW 27
RDLTTY 29
RCLK- 47
P1
U18
(9003)
U3
(9016)
TP2
10 SLE
11 CP
12 D
REG
G4
SDATA 85
1,4 D/FF 2
G1
G2
G3
13 A2
14 A1
15 A0
X → Y
REG
C5
FF
5D
TP6
U12-1
2 E5
U4-3
4 E6
C14
2.2
20V
DDRV- 9
(93L16)
U5
P3
P2
P1
P0
PE
Q2
Q1
Q0
MR
CEPCET CP
3 B2
2 B1
1 B0
U18-1
4 F7
(9003)
U22
U3
(9016)
U13-9
2C7
V1
U6
(9338)
U12-8
2 F5
U3-12
4 C5
V2
U14
(9024)
S
R
J
K
Q
TP3
U3-5
4 D7
DDRG- 91
(9007)
U21
U20-12
2 D7
U20-13
2 D7
DDCTO2 89
DDCTO1 92
DDCAL- 93
6 C2
7 C1
9 C0
(93L16)
U7
V1
ELSNG069

Figure FO-9. DDOW decoder card 21A8, schematic diagram (sheet 3 of 4).

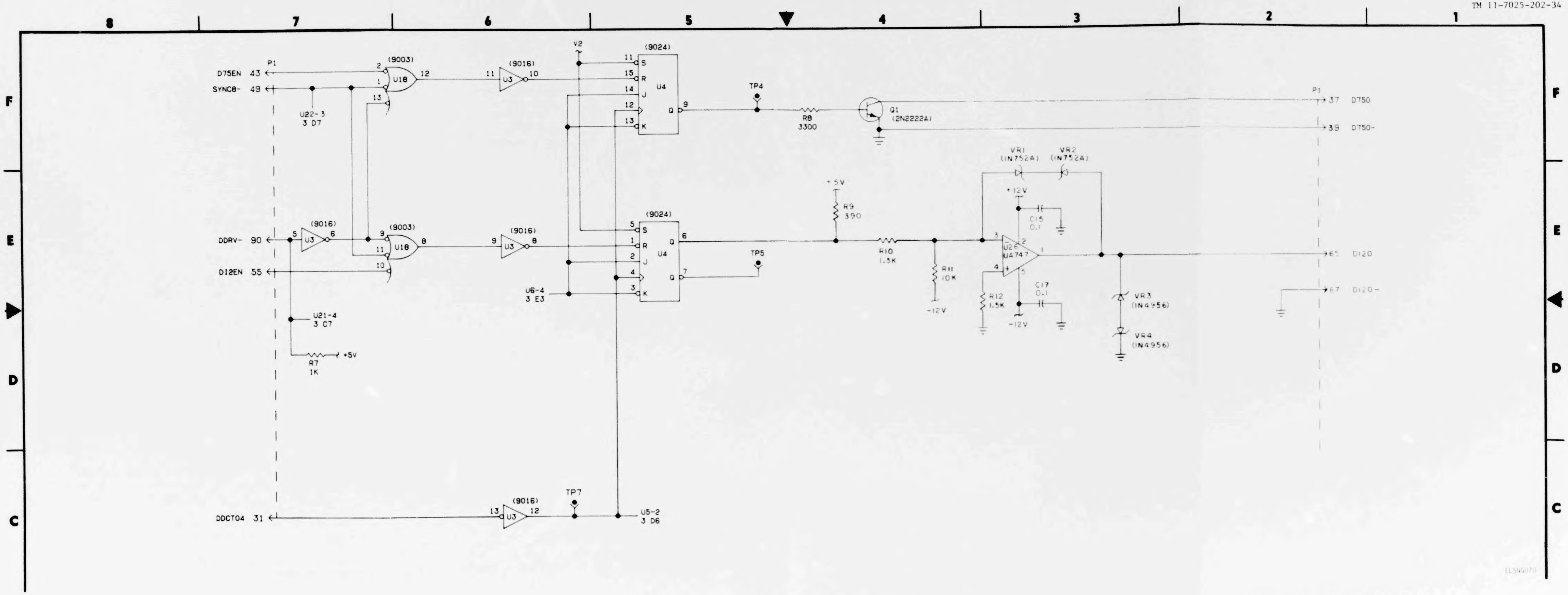
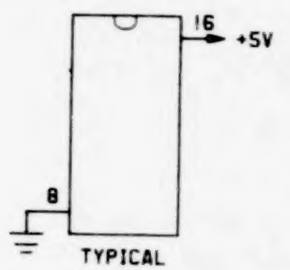

8
7
6
5
4
3
2
1
F
E
D
C
P1
D75EN 43
SYNC8- 49
U22-3
3 D7
(9003)
U18
2
1
13
12
(9016)
U3
11
10
V2
(9024)
U4
11 S
15 R
14 J
12
13 K
Q 9
TP4
R8
3300
Q1
(2N2222A)
P1
37 D750
39 D750-
DDRV- 90
DI2EN 55
(9016)
U3
5
6
(9003)
U18
9
11
10
8
(9016)
U3
9
8
(9024)
U4
5 S
1 R
2 J
4
3 K
Q 6
Q 7
TP5
U6-4
3 E3
U21-4
3 C7
R7
1K
+5V
+5V
R9
390
R10
1.5K
R11
10K
-12V
VR1
(IN752A)
VR2
(IN752A)
+12V
C15
0.1
U25
UA747
3
2
1
4
5
R12
1.5K
C17
0.1
-12V
VR3
(IN4956)
VR4
(IN4956)
65 DI20
67 DI20-
DDCT04 31
(9016)
U3
13
12
TP7
U5-2
3 D6
EL5NG070

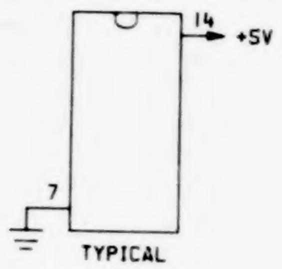
Figure FO-9. DDOW decoder card 21A8, schematic diagram (sheet 4 of 4).

8
7
6
5
4
3
2
1
F
E
D
C



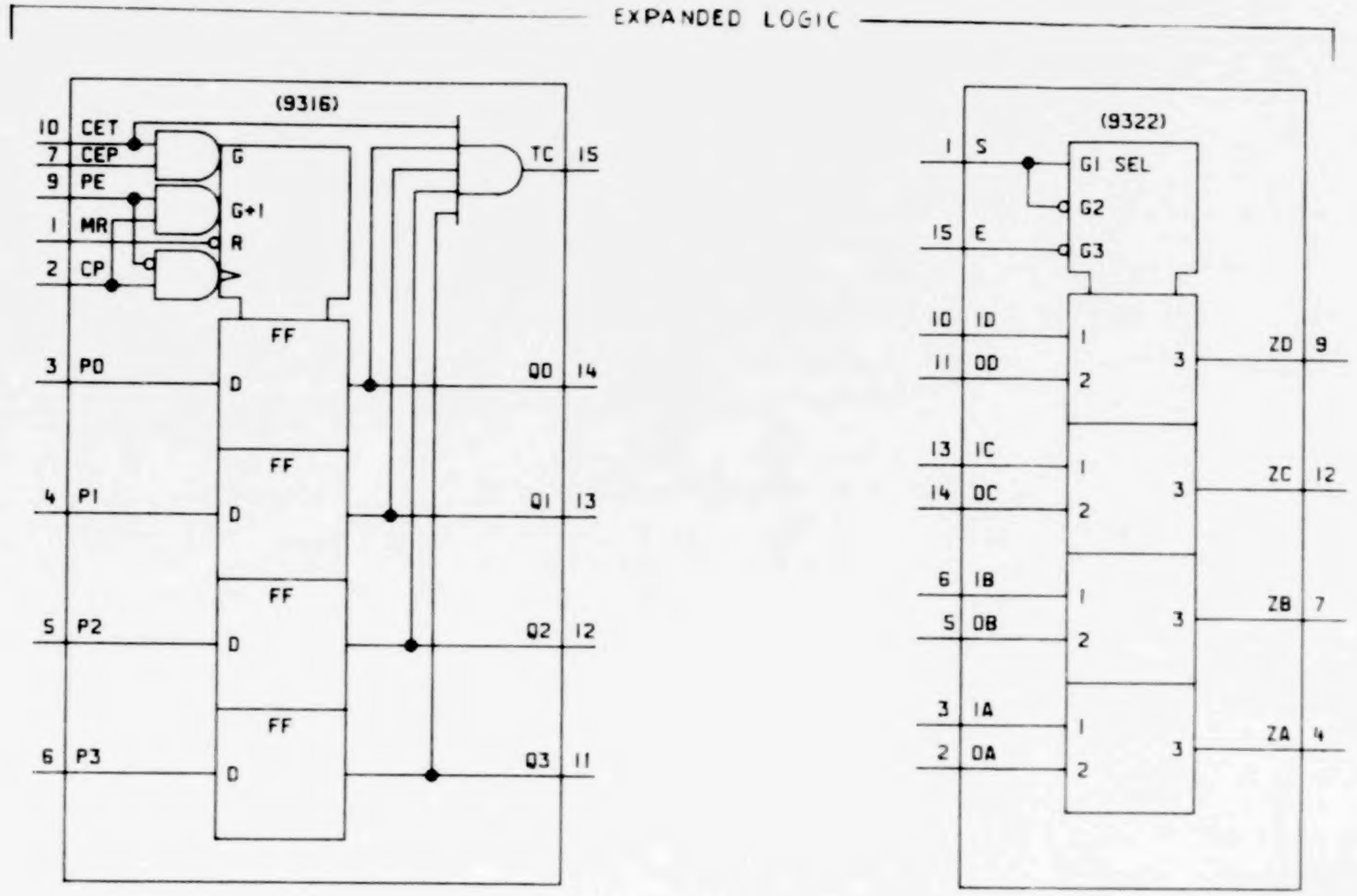
16
+5V
8
TYPICAL

U20	SM-A-942015	(9024)
U7	M38510/01405BEB	(9322)
U34	SM-A-942013	(9316)
U14,U28	M38510/01203BEB	(54123)
U6	SM-A-942163	(54S109)

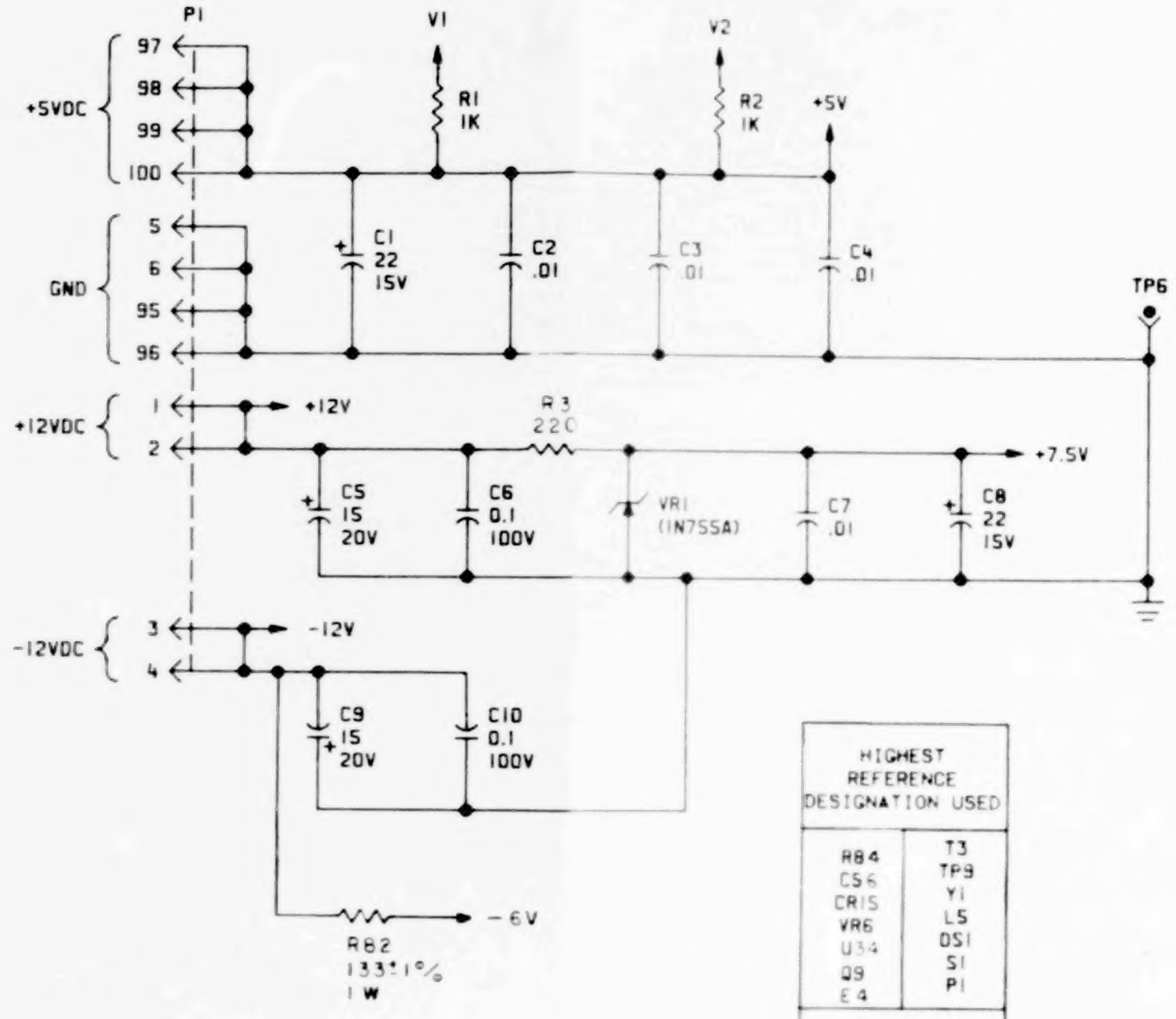


14
+5V
7
TYPICAL

U13,U27	SM-A-942001	(9003)
U21	SM-A-942007	(9016)



EXPANDED LOGIC
(9316)
10 CET
7 CEP
9 PE
1 MR
2 CP
G
G+1
R
TC 15
3 P0
D
FF
Q0 14
4 P1
D
FF
Q1 13
5 P2
D
FF
Q2 12
6 P3
D
FF
Q3 11
(9322)
1 S
G1 SEL
G2
15 E
G3
10 1D
11 0D
1
2
3
ZD 9
13 1C
14 0C
ZC 12
6 1B
5 0B
ZB 7
3 1A
2 0A
ZA 4



P1
+5VDC
97
98
99
100
V1
R1
1K
V2
R2
1K
+5V
GND
5
6
95
96
C1
22
15V
C2
.01
C3
.01
C4
.01
TP6
+12VDC
1
2
+12V
R3
220
+7.5V
C5
15
20V
C6
0.1
100V
VR1
(1N755A)
C7
.01
C8
22
15V
-12VDC
3
4
-12V
C9
15
20V
C10
0.1
100V
R82
133±1%
1W
-6V

HIGHEST REFERENCE DESIGNATION USED	
R84 C56 CR15 VR6 U34 Q9 E4	T3 TP9 Y1 L5 DS1 S1 P1
REFERENCE DESIGNATIONS NOT USED	
TP1-3 TP5 U1-5 U8-12 U15-18	U22-26 U31-33

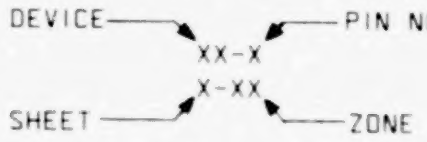
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

4. CIRCUIT CONTINUATION DESTINATION.



DEVICE
PIN NO.
XX-X
X-XX
SHEET
ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

6. ENCLOSED LEGEND FOR S1 INDICATES ACTUAL MARKING ON CARD FILE COVER ASSEMBLY.

EL5NG071

Figure FO-10. SG D/R card 21A9, schematic diagram (sheet 1 of 5).

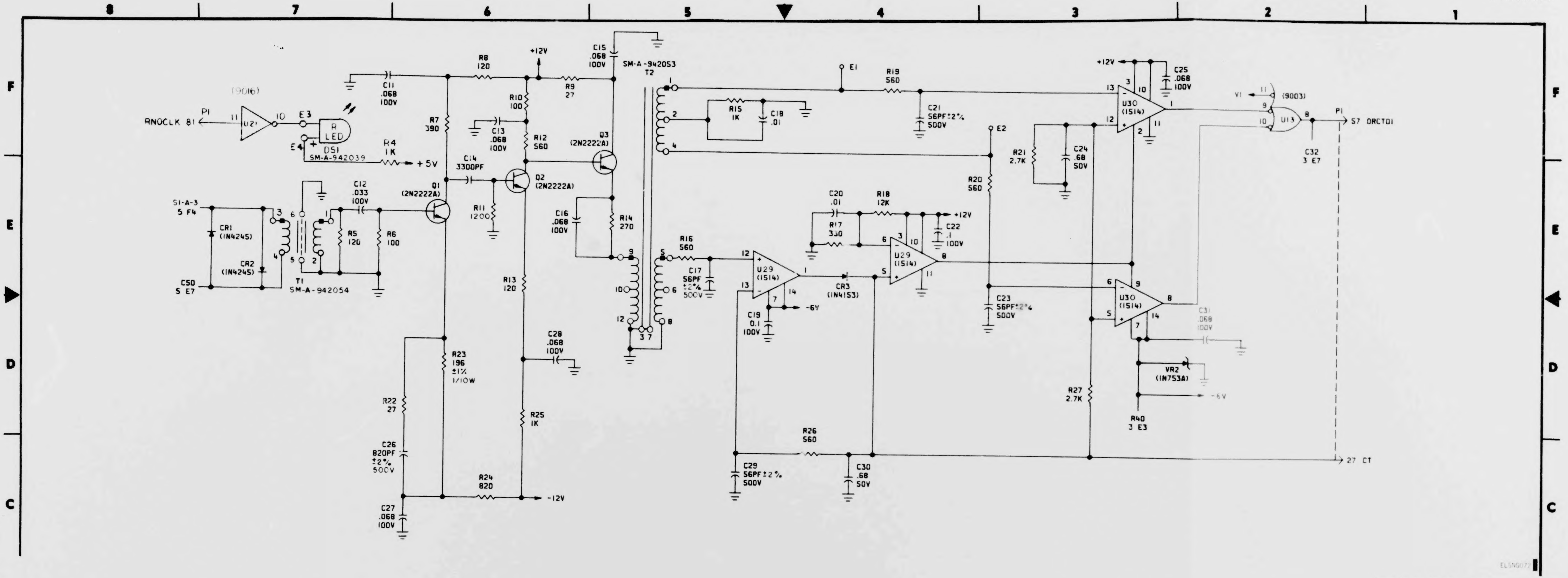

8
7
6
5
4
3
2
1
F
E
D
C
RNOCLK 81
P1
(9016)
U21
11
10
E3
E4
R LED
DS1
SM-A-942039
R4
1K
+5V
C11
.068
100V
R8
120
+12V
R9
27
R10
100
R7
390
C13
.068
100V
R12
560
Q3
(2N2222A)
C14
3300PF
Q2
(2N2222A)
Q1
(2N2222A)
C12
.033
100V
S1-A-3
5 F4
CR1
(1N4245)
CR2
(1N4245)
C50
5 E7
T1
SM-A-942054
R5
120
R6
100
R11
1200
C15
.068
100V
SM-A-942053
T2
C16
.068
100V
R14
270
R13
120
C28
.068
100V
R23
196
±1%
1/10W
R22
27
C26
820PF
±2%
500V
R24
820
-12V
R25
1K
C27
.068
100V
R15
1K
C18
.01
E1
R19
560
C21
56PF±2%
500V
R16
560
C17
56PF
±2%
500V
U29
(1514)
C19
0.1
100V
-6V
CR3
(1N4153)
C20
.01
R17
330
R18
12K
C22
.1
100V
R26
560
C29
56PF±2%
500V
C30
.68
50V
E2
R20
560
C23
56PF±2%
500V
R21
2.7K
C24
.68
50V
U30
(1514)
C25
.068
100V
R27
2.7K
VR2
(1N753A)
R40
3 E3
C31
.068
100V
V1
(9003)
U13
S7 DRCT01
C32
3 E7
27 CT
EL5NG072

Figure FO-10. SG D/R card 21A9, schematic diagram (sheet 2 of 5).

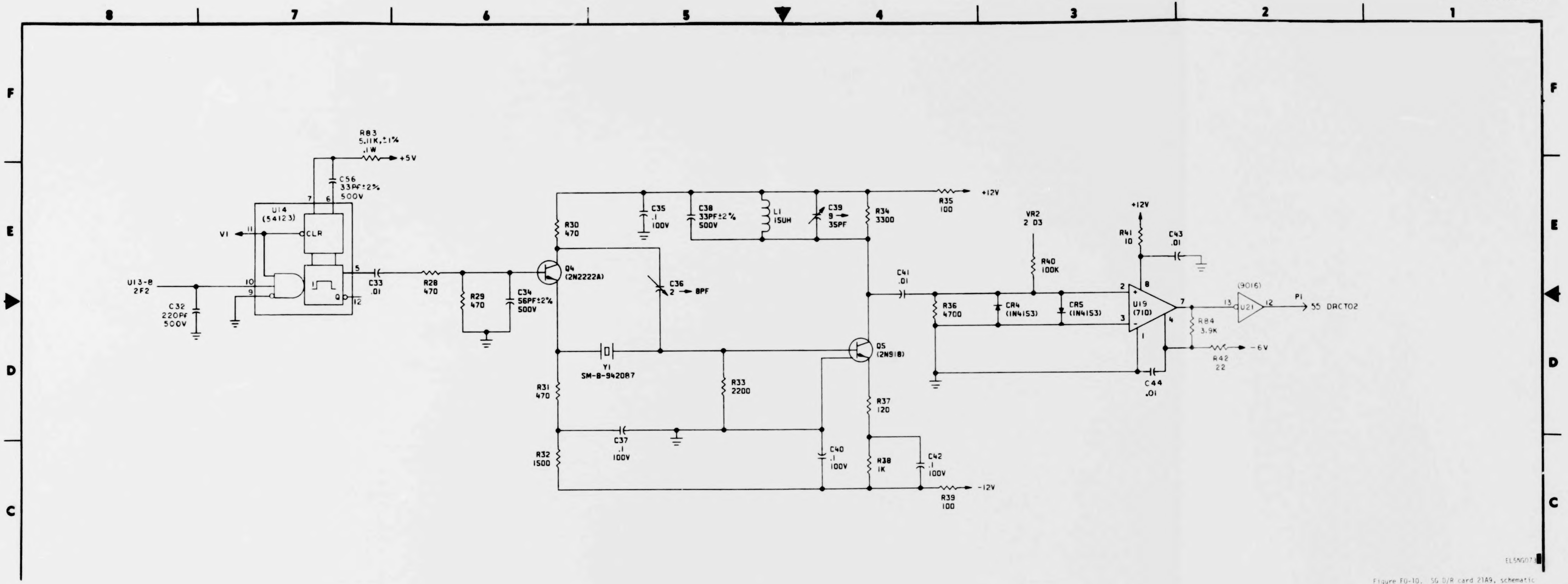

8
7
6
5
4
3
2
1
F
E
D
C
R83
5.11K,±1%
.1W
+5V
C56
33PF±2%
500V
7
6
U14
(54123)
V1
11
CLR
10
9
5
Q
12
U13-8
2F2
C32
220PF
500V
C33
.01
R28
470
R29
470
C34
56PF±2%
500V
Q4
(2N2222A)
R30
470
C35
.1
100V
C38
33PF±2%
500V
L1
15UH
C39
9 → 35PF
R34
3300
R35
100
+12V
C36
2 → 8PF
Y1
SM-B-942087
R31
470
R33
2200
Q5
(2N918)
R37
120
C37
.1
100V
R32
1500
C40
.1
100V
R38
1K
C42
.1
100V
R39
100
-12V
C41
.01
R36
4700
CR4
(1N4153)
CR5
(1N4153)
VR2
2 D3
R40
100K
+12V
R41
10
C43
.01
2
3
8
U19
(710)
7
4
1
C44
.01
R84
3.9K
R42
22
-6V
(9016)
13
U21
12
P1
55 DRCT02
EL5NG073

Figure FO-10. SG D/R card 21A9, schematic diagram (sheet 3 of 5).

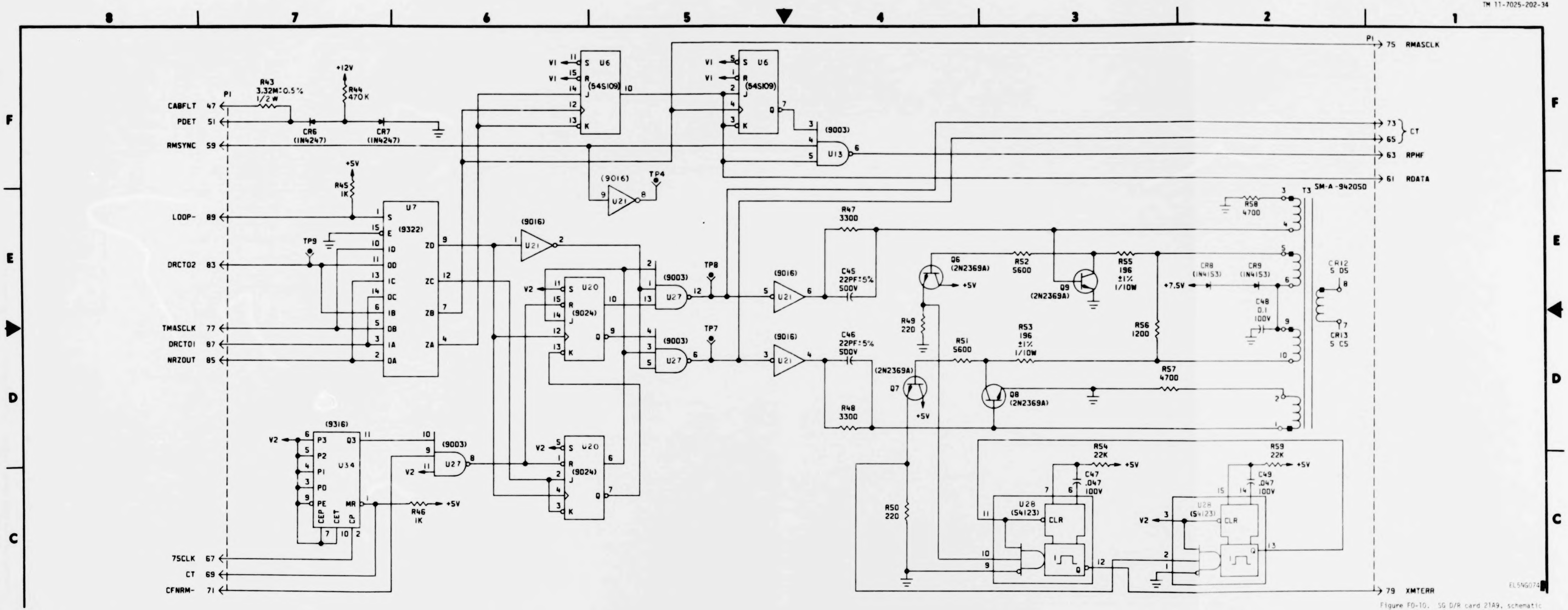
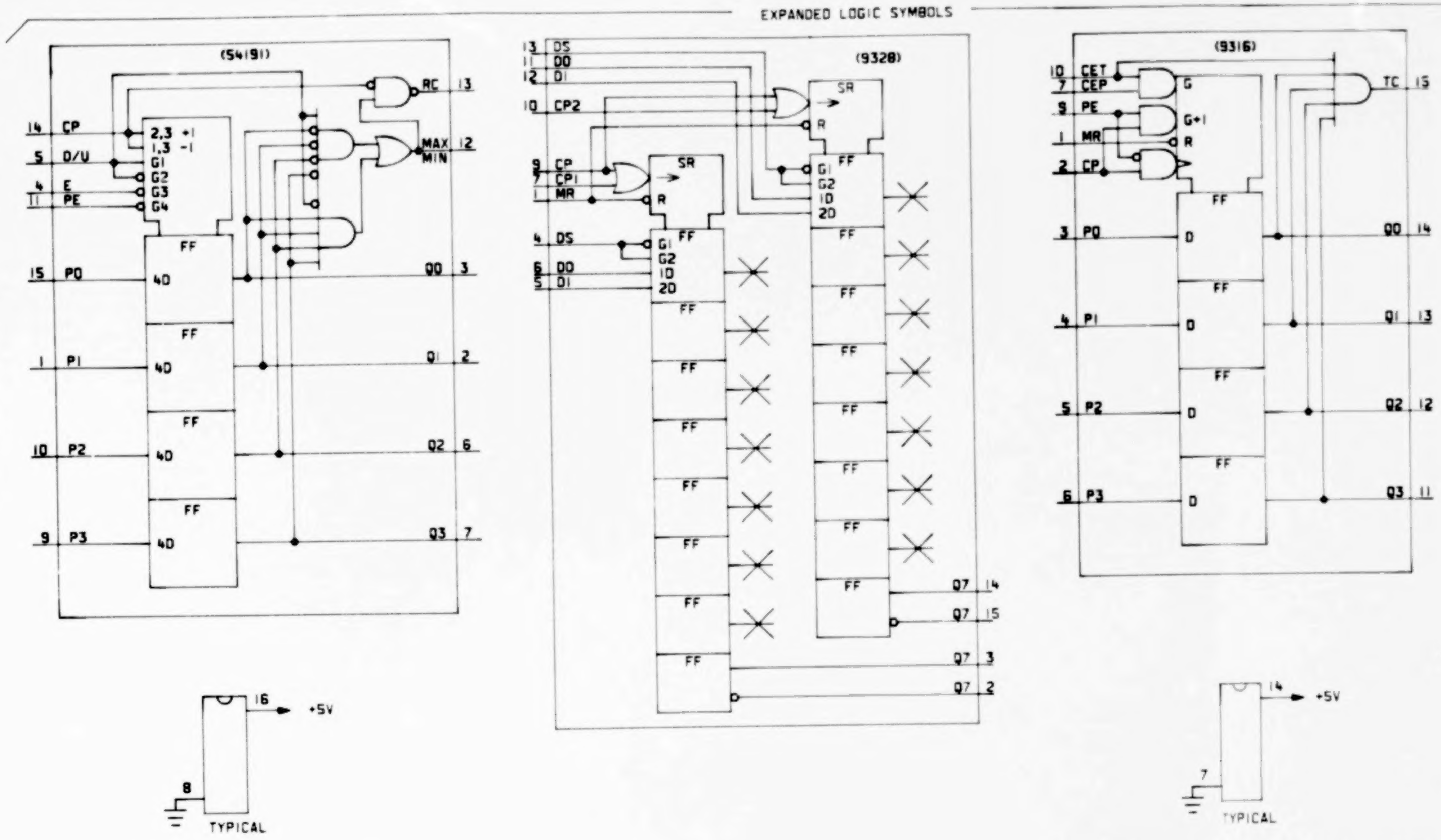
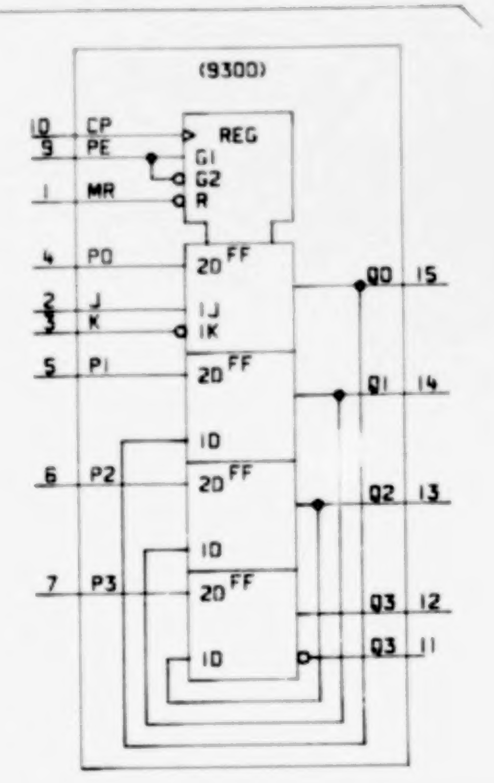

8
7
6
5
4
3
2
1
F
E
D
C
P1
CABFLT 47
PDET 51
RMSYNC 59
LOOP- 89
DRCTO2 83
TMASCLK 77
DRCTO1 87
NRZOUT 85
75CLK 67
CT 69
CFNRM- 71
R43 3.32M±0.5% 1/2 W
+12V
R44 470K
CR6 (1N4247)
CR7 (1N4247)
+5V
R45 1K
TP9
U7 (9322)
U6 (54S109)
VI
(9016) U21
TP4
(9003) U13
TP8
TP7
U20 (9024)
U27 (9003)
V2
(9316) U34
R46 1K
R47 3300
C45 22PF±5% 500V
C46 22PF±5% 500V
R48 3300
Q6 (2N2369A)
Q7 (2N2369A)
Q8 (2N2369A)
Q9 (2N2369A)
R49 220
R50 220
R51 5600
R52 5600
R53 196 ±1% 1/10W
R55 196 ±1% 1/10W
R56 1200
R57 4700
R58 4700
T3 SM-A-942050
CR8 (1N4153)
CR9 (1N4153)
+7.5V
C48 0.1 100V
CR12 5 DS
CR13 5 CS
R54 22K
R59 22K
C47 .047 100V
C49 .047 100V
U28 (54123)
CLR
75 RMASCLK
73 CT
65
63 RPHF
61 RDATA
79 XMTERR
EL5NG074

Figure FO-10. SG D/R card 21A9, schematic diagram (sheet 4 of 5).

HIGHEST REFERENCE DESIGNATION USED	
C13	R5
CR1	TP7
DS1	U33
E2	P1
REFERENCE DESIGNATIONS NOT USED	


8
7
6
5
4
EXPANDED LOGIC SYMBOLS
(54191)
CP
D/U
E
PE
P0
P1
P2
P3
2,3 +1
1,3 -1
G1
G2
G3
G4
FF
4D
RC
MAX
MIN
Q0
Q1
Q2
Q3
(9328)
DS
D0
D1
CP2
CP
CP1
MR
SR
R
G1
G2
1D
2D
Q7
(9316)
CET
CEP
PE
MR
CP
G
G+1
R
D
TC
16
+5V
8
TYPICAL
14
+5V
7
TYPICAL


3
(9300)
CP
PE
MR
REG
G1
G2
R
P0
J
K
P1
P2
P3
1J
1K
2D
1D
FF
Q0
Q1
Q2
Q3

U1,U2,U3,U5 U6,U9,U10,U13 U14,U15,U16	M38510/15902BEB	(9328) (9328) (9328)
U7,U8	M38510/15901BEB	(9300)
U4,U17,U33	SM-A-942015	(9024)
U29	M38510/01203BEB	(54123)
U24,U28	SM-A-942025	(54191)
U31	SM-A-942013	(9316)
U30	SM-A-942163	(54S109)

U11,U12,U18,U19	SM-A-942003	(9007)
U22,U23,U27	SM-A-942004	(9009)
U21,U32	SM-A-942008	(9005)
U20	SM-A-942007	(9016)
U25	SM-A-942002	(9004)
U26	SM-A-942001	(9003)

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.
4. CIRCUIT CONTINUATION DESTINATION.

DEVICE — XX-X — PIN NO
SHEET — X-XX — ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

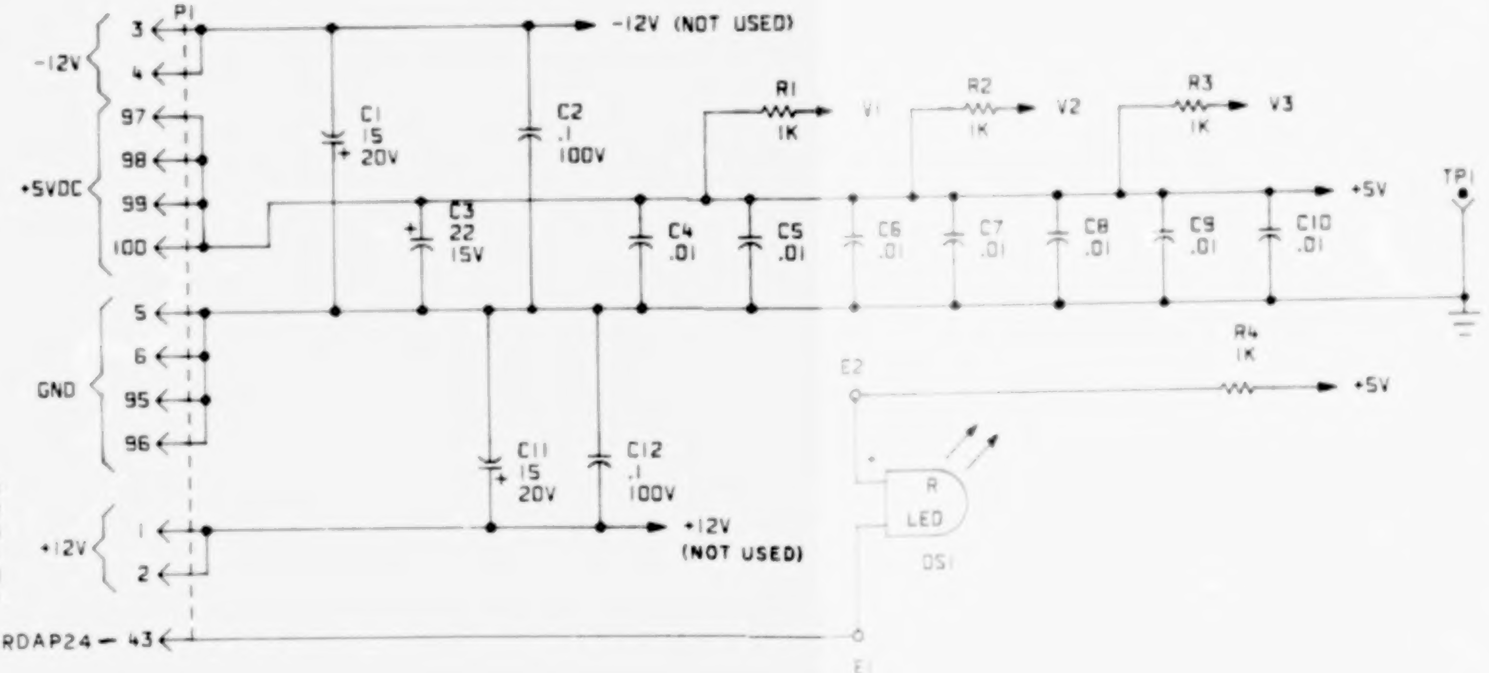

2
1
P1
-12V
+5VDC
GND
+12V
3
4
97
98
99
100
5
6
95
96
1
2
-12V (NOT USED)
C1 15 20V
C2 .1 100V
C3 22 15V
C4 .01
C5 .01
C6 .01
C7 .01
C8 .01
C9 .01
C10 .01
R1 1K
R2 1K
R3 1K
V1
V2
V3
+5V
TP1
R4 1K
+5V
E2
R
LED
DS1
C11 15 20V
C12 .1 100V
+12V (NOT USED)
RDAP24 — 43
E1

Figure FO-11. FS card 21A7, schematic diagram (sheet 1 of 6).

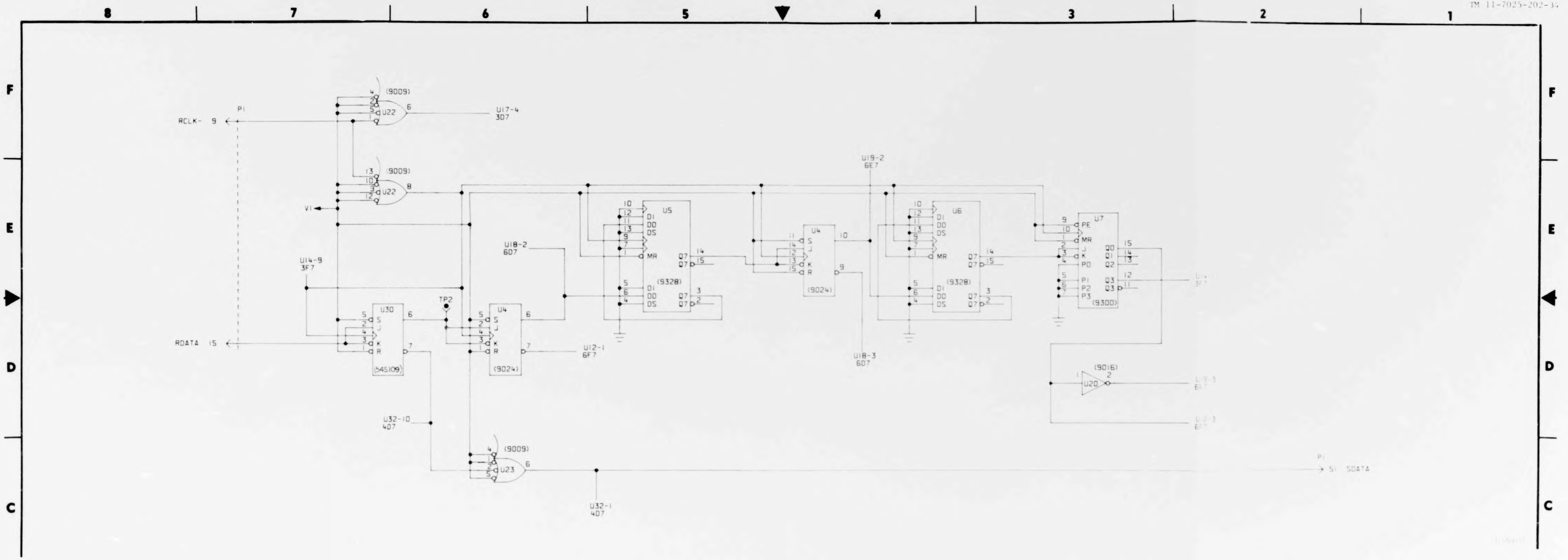

8
7
6
5
4
3
2
1
F
E
D
C
RCLK- 9
P1
RDATA 15
(9009)
U22
U17-4
3D7
V1
U14-9
3F7
U30
(54S109)
TP2
U4
(9024)
U12-1
6F7
U18-2
6D7
U32-10
4D7
U23
U32-1
4D7
U5
(9328)
MR
DI
DO
DS
Q7
U19-2
6E7
(9024)
U18-3
6D7
U6
(9328)
U7
(9300)
PE
PO
P1
P2
P3
Q0
Q1
Q2
Q3
(9016)
U20
U14-11
3F7
U19-3
6F7
U12-3
6F7
P1
51 SDATA

Figure FO-11. FS card 21A7, schematic diagram (sheet 2 of 6).

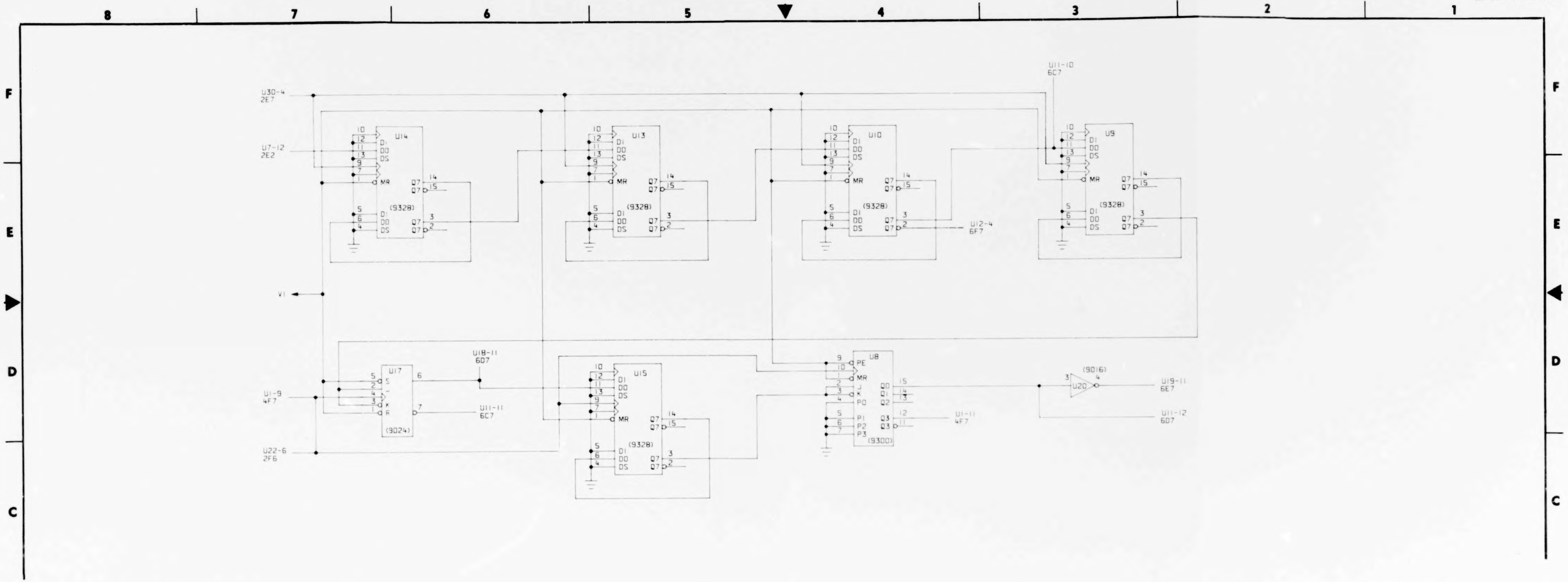

8
7
6
5
4
3
2
1
F
E
D
C
U30-4
2E7
U7-12
2E2
U14
U13
U10
U9
(9328)
DI
DO
DS
MR
Q7
U11-10
6C7
U12-4
6F7
V1
U17
(9024)
U18-11
6D7
U11-11
6C7
U1-9
4F7
U22-6
2F6
U15
U8
(9300)
PE
J
K
P0
P1
P2
P3
Q0
Q1
Q2
Q3
U1-11
4F7
U20
(9016)
U19-11
6E7
U11-12
6D7

Figure FO-11. FS card 2A7, schematic diagram (sheet 3 of 6).

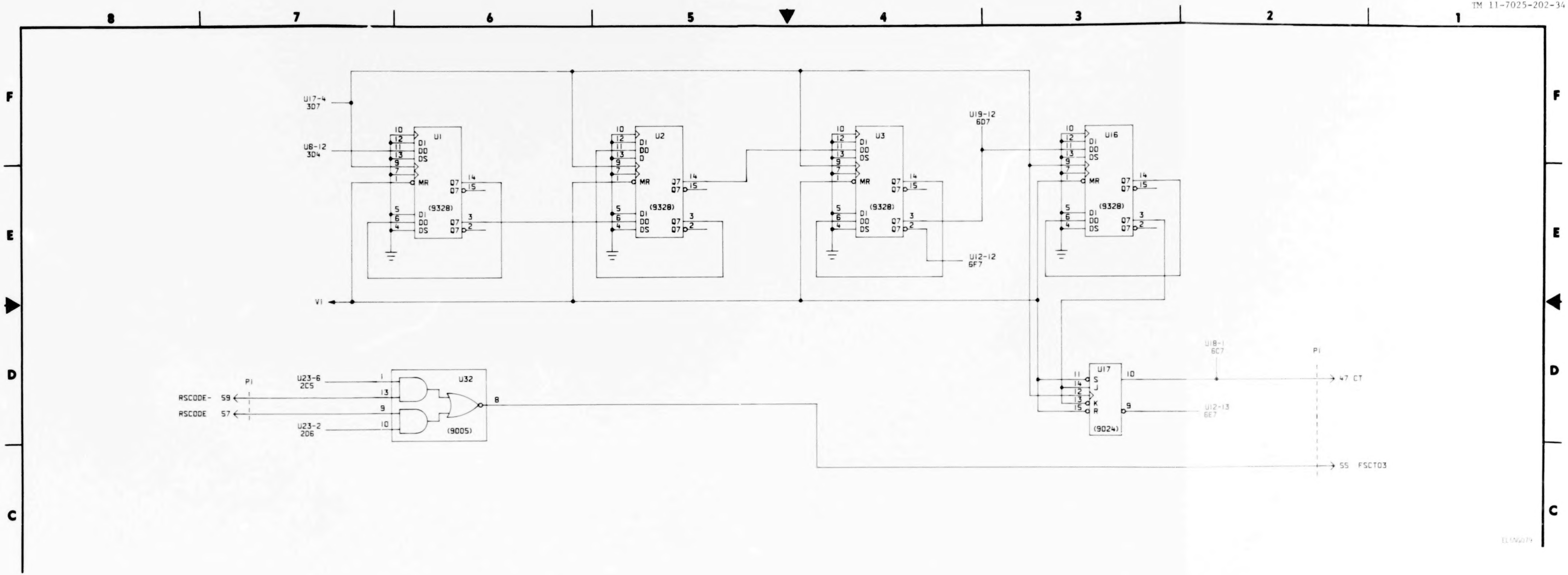
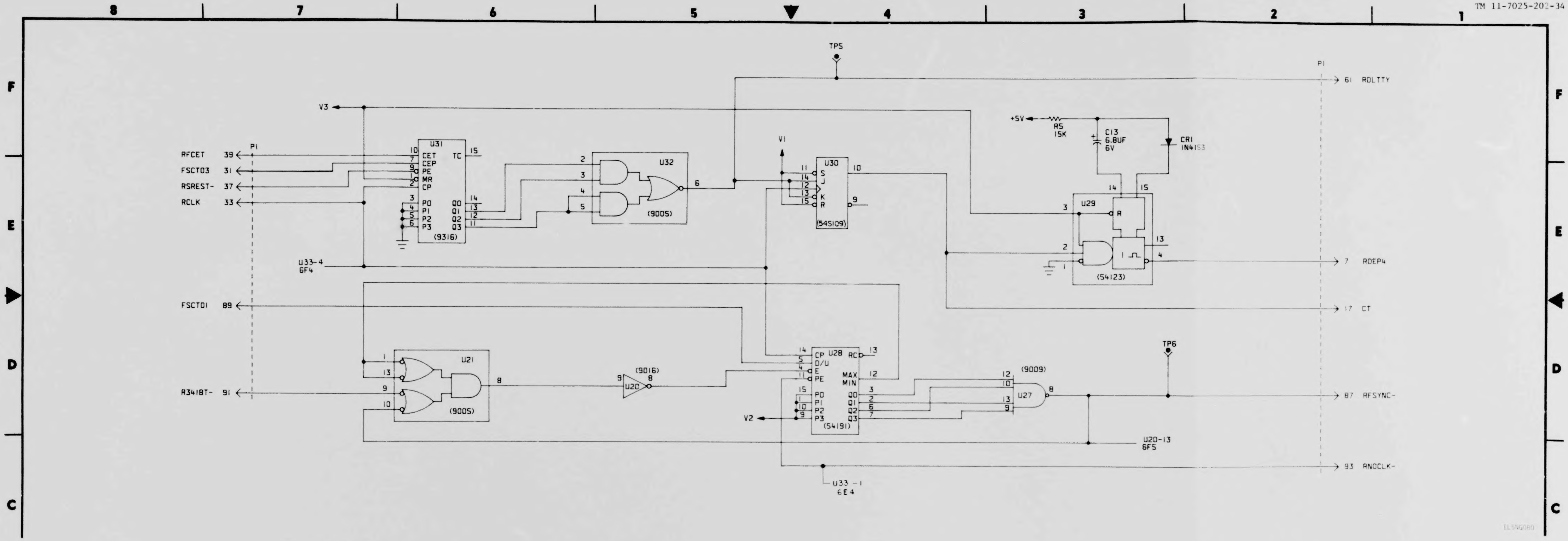

8
7
6
5
4
3
2
1
F
E
D
C
U17-4
3D7
U8-12
3D4
U1
U2
U3
U16
(9328)
MR
DI
DO
DS
U19-12
6D7
U12-12
6F7
V1
U18-1
6C7
P1
U17
(9024)
47 CT
U12-13
6E7
U23-6
2C5
U23-2
2D6
U32
(9005)
RSCODE- 59
RSCODE 57
55 FSCT03

Figure FO-11. FS card 21A7, schematic diagram (sheet 4 of 6).



8
7
6
5
4
3
2
1
F
E
D
C
TP5
P1
61 RDLTTY
V3
+5V
R5
15K
C13
6.8UF
6V
CR1
1N4153
RFCET 39
FSCT03 31
RSREST- 37
RCLK 33
U31
CET
CEP
PE
MR
CP
TC
P0
P1
P2
P3
Q0
Q1
Q2
Q3
(9316)
U32
(9005)
V1
U30
S
J
K
R
(54S109)
U29
R
(54123)
7 RDEP4
17 CT
U33-4
6F4
FSCT01 89
R341BT- 91
U21
(9005)
(9016)
U20
U28
CP
D/U
E
PE
RC
MAX
MIN
(54191)
V2
(9009)
U27
TP6
87 RFSYNC-
U20-13
6F5
93 RNOCLK-
U33-1
6E4
EL5NG080

Figure FO-11. FS card 21A7, schematic diagram (sheet 5 of 6).

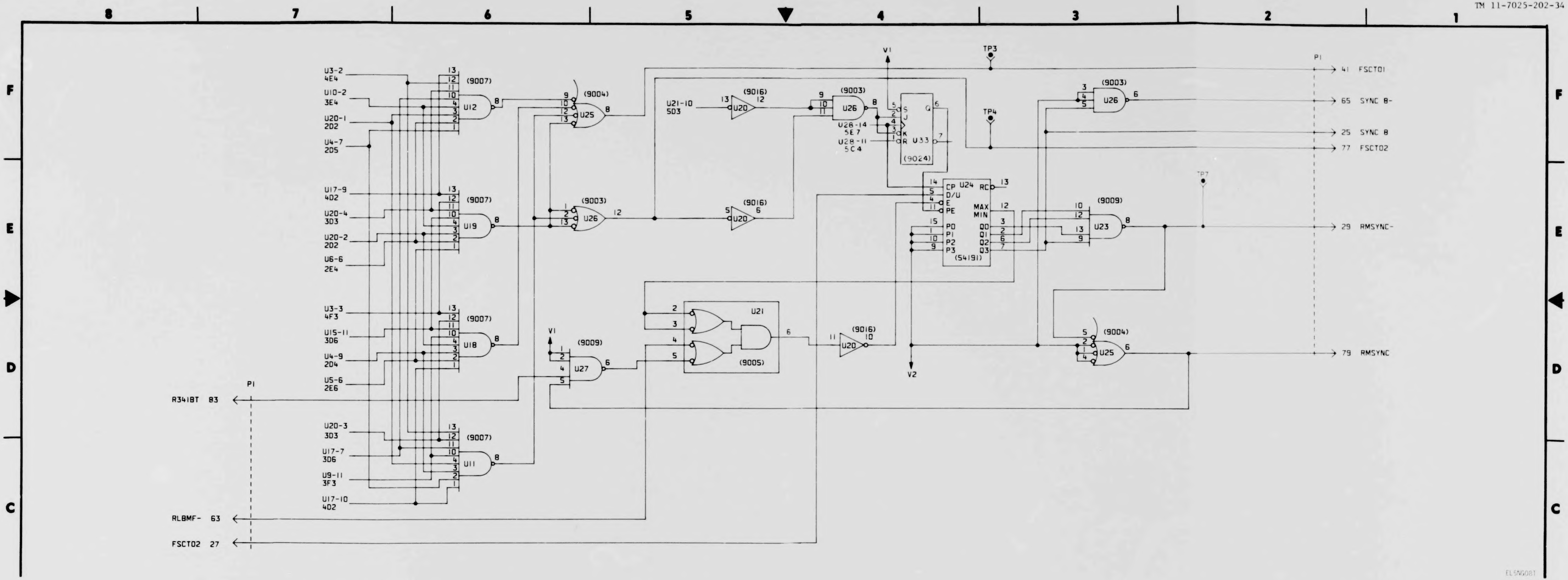
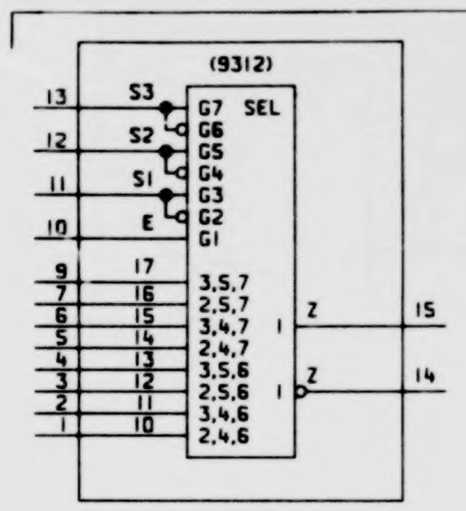
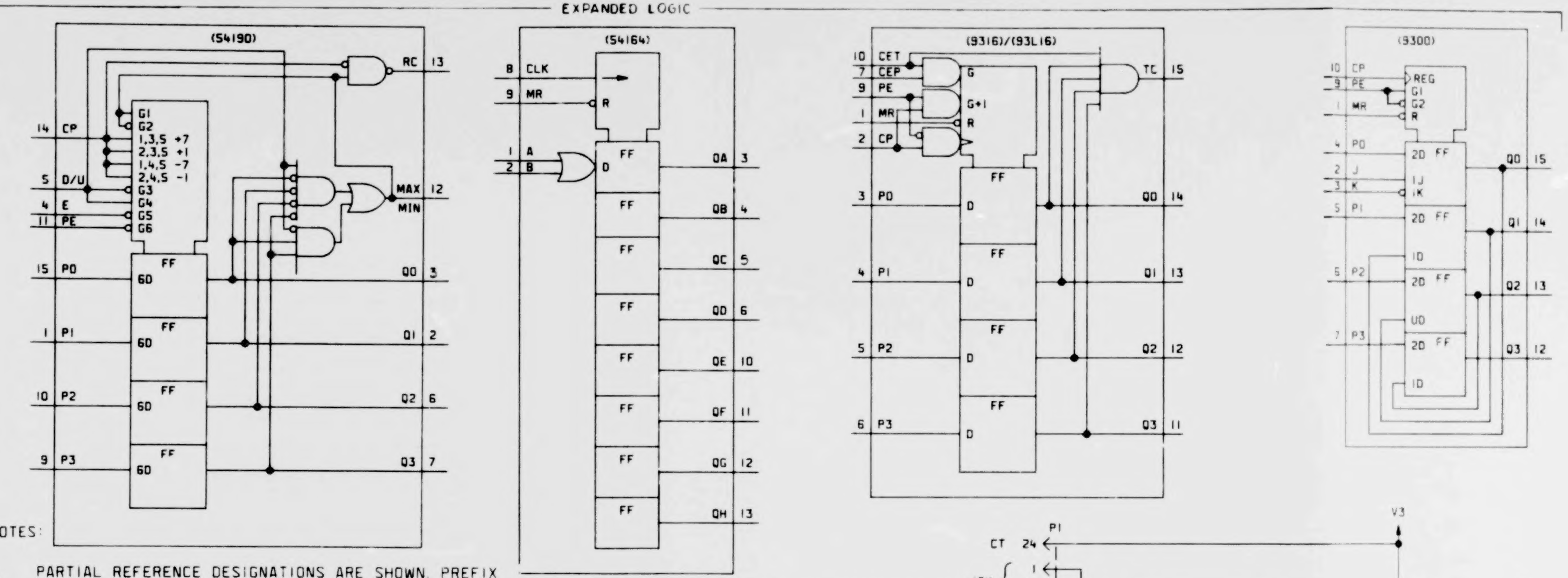
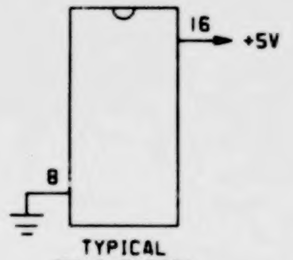

8
7
6
5
4
3
2
1
F
E
D
C
U3-2 4E4
U10-2 3E4
U20-1 2D2
U4-7 2D5
U12 (9007)
U25 (9004)
U21-10 5D3
U20 (9016)
U26 (9003)
U28-14 5E7
U28-11 5C4
U33 (9024)
V1
TP3
TP4
U26 (9003)
P1
41 FSCT01
65 SYNC 8-
25 SYNC 8
77 FSCT02
U17-9 4D2
U20-4 3D3
U20-2 2D2
U6-6 2E4
U19 (9007)
U26 (9003)
U20 (9016)
U24 (54191)
CP
D/U
E
PE
P0
P1
P2
P3
RC
MAX MIN
Q0
Q1
Q2
Q3
U23 (9009)
TP7
29 RMSYNC-
U3-3 4F3
U15-11 3D6
U4-9 2D4
U5-6 2E6
U18 (9007)
V1
U27 (9009)
U21 (9005)
U20 (9016)
V2
U25 (9004)
79 RMSYNC
P1
R341BT 83
U20-3 3D3
U17-7 3D6
U9-11 3F3
U17-10 4D2
U11 (9007)
RLBMF- 63
FSCT02 27
EL5NG081

Figure FO-11. FS card 21A7, schematic diagram (sheet 6 of 6).

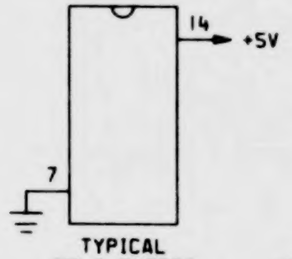

EXPANDED LOGIC
(9312)
S3
S2
S1
E
G7 SEL
G6
G5
G4
G3
G2
G1
3,5,7
2,5,7
3,4,7
2,4,7
3,5,6
2,5,6
3,4,6
2,4,6
Z
15
14


(54190)
CP
D/U
E
PE
P0
P1
P2
P3
1,3,5 +7
2,3,5 +1
1,4,5 -7
2,4,5 -1
6D
FF
RC
MAX
MIN
Q0
Q1
Q2
Q3
(54164)
CLK
MR
A
B
FF
QA
QB
QC
QD
QE
QF
QG
QH
(9316)/(93L16)
CET
CEP
PE
MR
CP
TC
P0
P1
P2
P3
Q0
Q1
Q2
Q3
(9300)
CP
PE
MR
REG
J
K
2D FF
1J
1K
1D
UD



TYPICAL

U17	SM-A-942024	(54190)
U8	SM-A-942027	(93L16)
U2	SM-A-942015	(9024)
U15	SM-A-942013	(9316)
U10	SM-A-942006	(9015)
U1,U3,U6,U7,U13,U14	M38510/01203BEB	(54123)
U22,U23,U24,U25	SM-A-942026	(93L12)
U9	M38510/15901BEB	(9300)

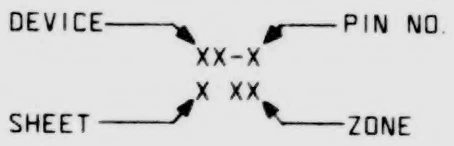


TYPICAL

U11	SM-A-942003	(9007)
U16,U18,U21	SM-A-942007	(9016)
U4	SM-A-942000	(9002)
U5	M38510/00903BCB	(54164)

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.
4. CIRCUIT CONTINUATION DESTINATION.


DEVICE
PIN NO.
XX-X
X XX
SHEET
ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.
6. CAPACITANCE VALUES ARE IN PICOFARADS (PF) FOR C19,20,24,25,29,30,34 AND 35 SHALL BE ±.5 PF.
7. CAPACITANCE VALUES ARE IN PICOFARADS (PF) FOR C16,21,26,31,36-39 SHALL BE ±2%, 500V.

HIGHEST REFERENCE DESIGNATION USED	
R64 C39 U35 CR1 VR1	TP9 P1 L8
REFERENCE DESIGNATIONS NOT USED	
U12 U20 U27	U29-U34

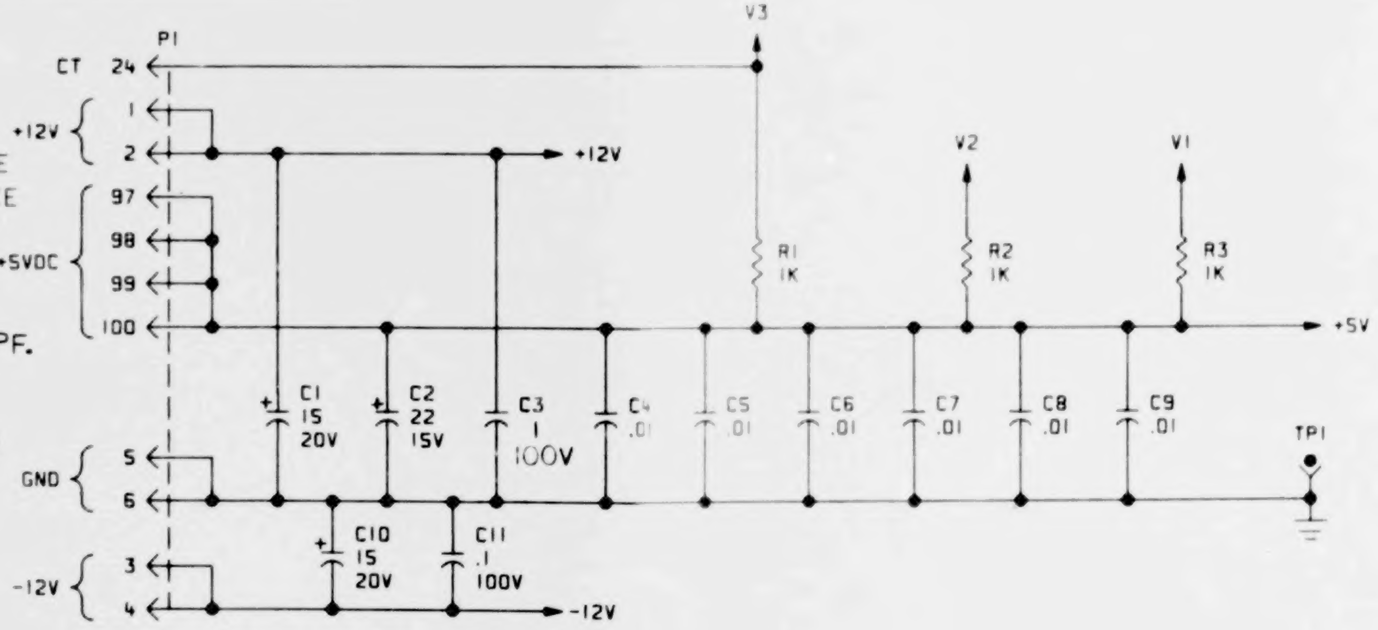

P1
CT
24
+12V
1
2
+5VDC
97
98
99
100
GND
5
6
-12V
3
4
V3
V2
V1
R1
1K
R2
1K
R3
1K
+12V
+5V
C1
15
20V
C2
22
15V
C3
1
100V
C4
.01
C5
.01
C6
.01
C7
.01
C8
.01
C9
.01
C10
15
20V
C11
.1
100V
TP1
-12V

Figure FO-12. GTM card 21A2, schematic diagram (sheet 1 of 5).

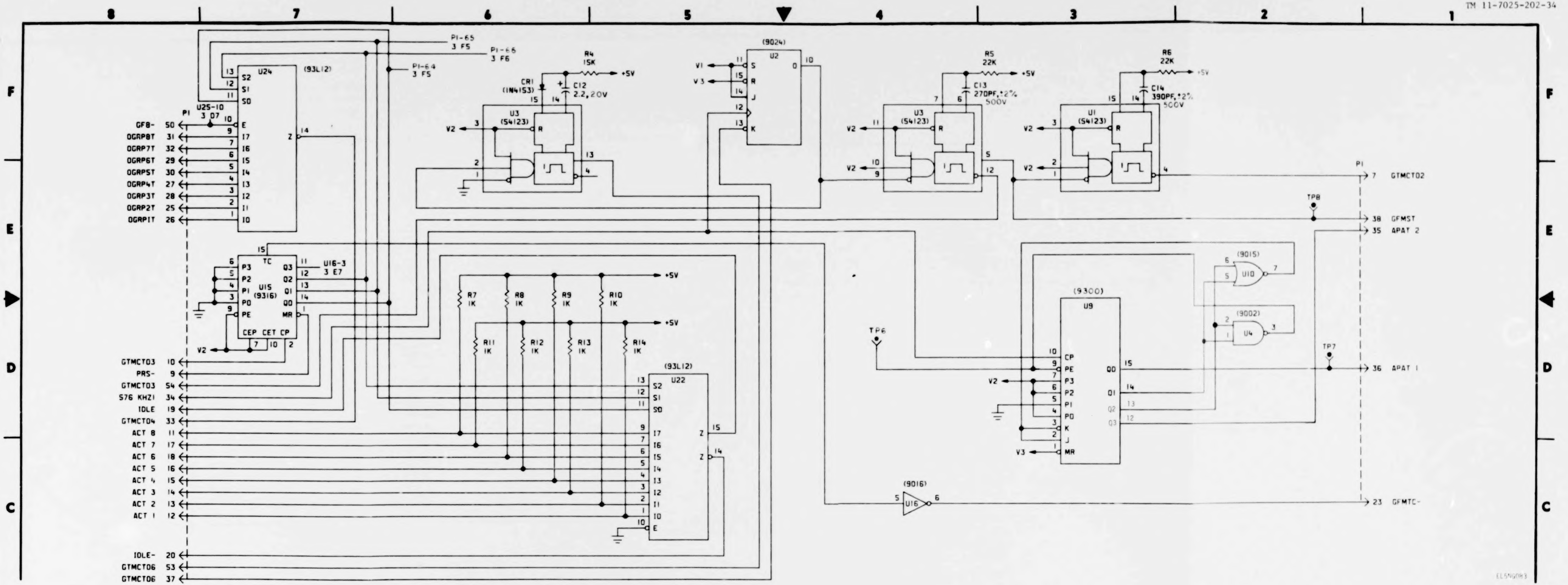

8
7
6
5
4
3
2
1
F
E
D
C
P1-65
3 F5
P1-66
3 F6
P1-64
3 F5
U24
(93L12)
S2
S1
S0
E
I7
I6
I5
I4
I3
I2
I1
I0
Z
U25-10
3 D7
P1
GF8-
OGRP8T
OGRP7T
OGRP6T
OGRP5T
OGRP4T
OGRP3T
OGRP2T
OGRP1T
U15
(9316)
TC
P3
P2
P1
P0
PE
Q3
Q2
Q1
Q0
MR
CEP
CET
CP
U16-3
3 E7
V2
GTMCT03
PRS-
GTMCT03
576 KHZ1
IDLE
GTMCT04
ACT 8
ACT 7
ACT 6
ACT 5
ACT 4
ACT 3
ACT 2
ACT 1
IDLE-
GTMCT06
GTMCT06
CR1
(1N4153)
R4
15K
+5V
C12
2.2,20V
U3
(54123)
R
R7
1K
R8
1K
R9
1K
R10
1K
R11
1K
R12
1K
R13
1K
R14
1K
U22
(93L12)
(9024)
U2
S
R
J
K
Q
V1
V3
R5
22K
C13
270PF,±2%
500V
R6
22K
C14
390PF,±2%
500V
U1
(54123)
GTMCT02
TP8
GFMST
APAT 2
(9015)
U10
(9002)
U4
(9300)
U9
TP6
TP7
CP
PE
P3
P2
P1
P0
K
J
MR
Q0
Q1
Q2
Q3
APAT 1
(9016)
U16
GFMTC-
EL5NG083

Figure FO-12. GTM card 21A2, schematic diagram (sheet 2 of 5).

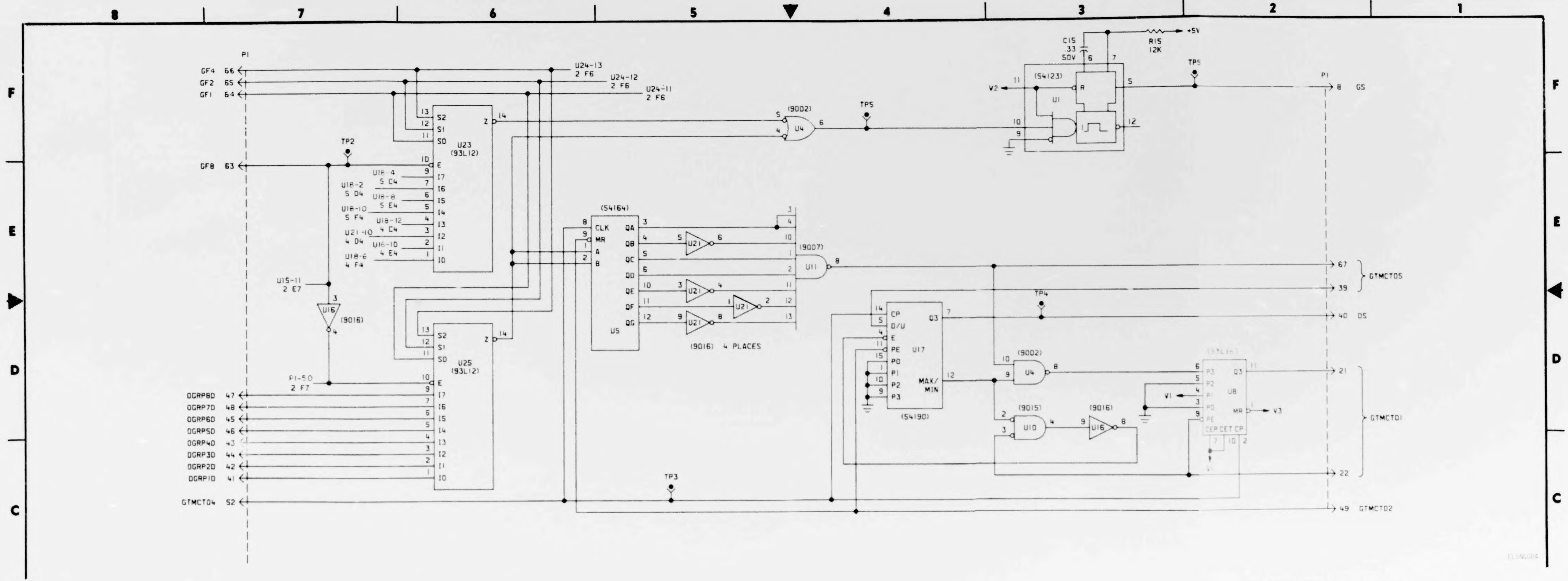

8
7
6
5
4
3
2
1
F
E
D
C
P1
GF4 66
GF2 65
GF1 64
GF8 63
U24-13 2 F6
U24-12 2 F6
U24-11 2 F6
TP2
U23 (93L12)
U18-4 5 C4
U18-2 5 D4
U18-8 5 E4
U18-10 5 F4
U18-12 4 C4
U21-10 4 D4
U16-10 4 E4
U18-6 4 F4
U15-11 2 E7
U16 (9016)
P1-50 2 F7
U25 (93L12)
DGRP8D 47
DGRP7D 48
DGRP6D 45
DGRP5D 46
DGRP4D 43
DGRP3D 44
DGRP2D 42
DGRP1D 41
GTMCT04 52
(9002) U4
TP5
(S4164) U5
CLK MR A B QA QB QC QD QE QF QG
U21
(9007) U11
(9016) 4 PLACES
TP3
C15 .33 50V
R15 12K
+5V
(S4123) U1
V2
TP5
P1
8 GS
TP4
U17 (S4190)
CP D/U E PE P0 P1 P2 P3 Q3 MAX/MIN
(9002) U4
(9015) U10
(9016) U16
(93L16) U8
V1
V3
67
39
GTMCT05
40 DS
21
22
GTMCT01
49 GTMCT02
EL5NG084

Figure FO-12. GTM card 21A2, schematic diagram (sheet 3 of 5).

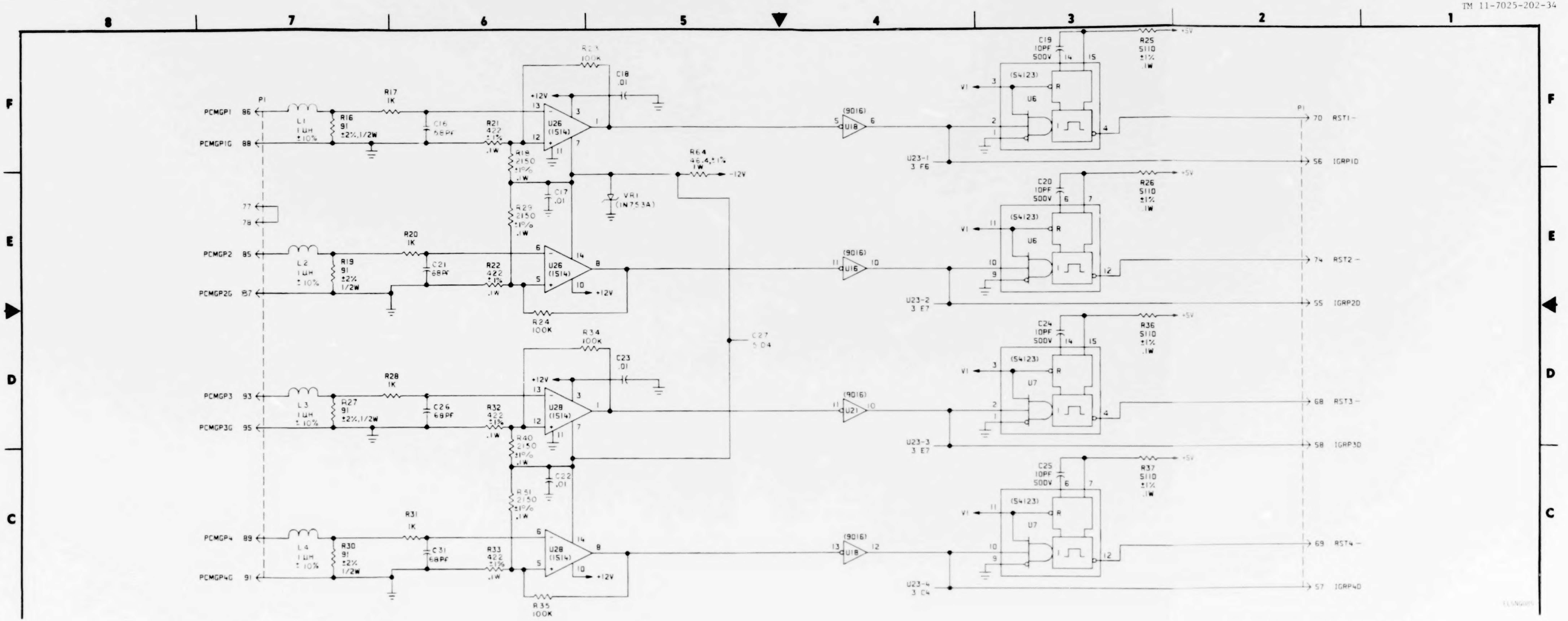

8
7
6
5
4
3
2
1
F
E
D
C
PCMGP1 86
PCMGP1G 88
PCMGP2 85
PCMGP2G 87
PCMGP3 93
PCMGP3G 95
PCMGP4 89
PCMGP4G 91
77
78
P1
L1 1UH ±10%
L2 1UH ±10%
L3 1UH ±10%
L4 1UH ±10%
R16 91 ±2%,1/2W
R19 91 ±2% 1/2W
R27 91 ±2%,1/2W
R30 91 ±2% 1/2W
R17 1K
R20 1K
R28 1K
R31 1K
C16 68PF
C21 68PF
C26 68PF
C31 68PF
R21 422 ±1% .1W
R22 422 ±1% .1W
R32 422 ±1% .1W
R33 422 ±1% .1W
R18 2150 ±1% .1W
R29 2150 ±1% .1W
R40 2150 ±1% .1W
R51 2150 ±1% .1W
C17 .01
C22 .01
R23 100K
R24 100K
R34 100K
R35 100K
C18 .01
C23 .01
U26 (1514)
U28 (1514)
+12V
R64 46.4,±1% .1W
-12V
VR1 (IN753A)
C27 5 D4
(9016) U18
(9016) U16
(9016) U21
U23-1 3 F6
U23-2 3 E7
U23-3 3 E7
U23-4 3 C4
V1
(54123)
U6
U7
R
C19 10PF 500V
C20 10PF 500V
C24 10PF 500V
C25 10PF 500V
R25 5110 ±1% .1W
R26 5110 ±1% .1W
R36 5110 ±1% .1W
R37 5110 ±1% .1W
+5V
70 RST1-
56 IGRP1D
74 RST2-
55 IGRP2D
68 RST3-
58 IGRP3D
69 RST4-
57 IGRP4D
EL5NG005

Figure FO-12. GTM card 21A2, schematic diagram (sheet 4 of 5).

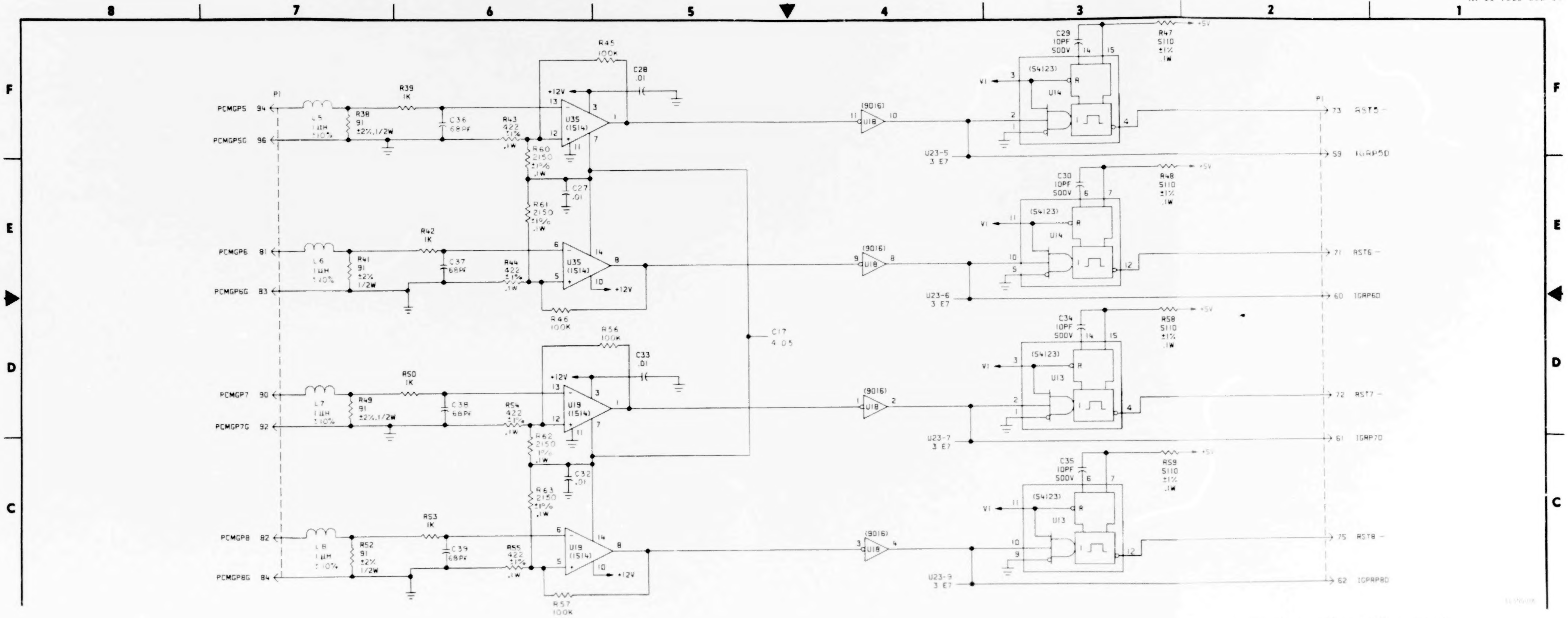
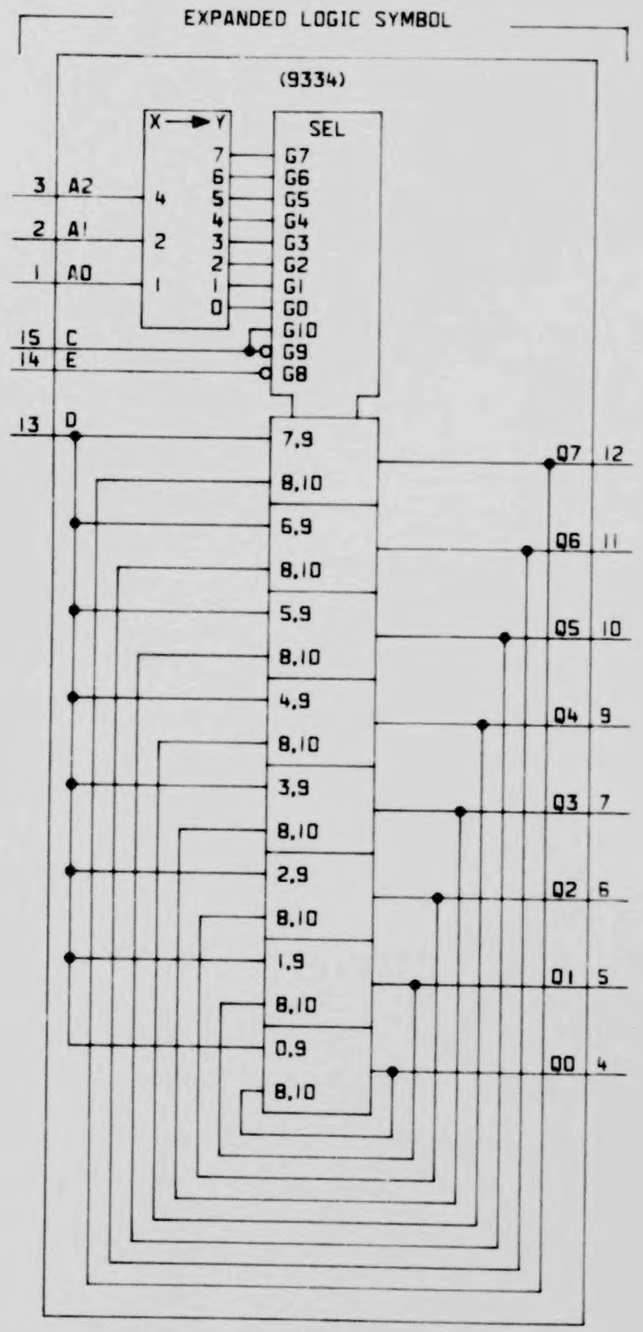

PCMGP5 94
PCMGP5G 96
PCMGP6 81
PCMGP6G 83
PCMGP7 90
PCMGP7G 92
PCMGP8 82
PCMGP8G 84
P1
L5 1 μH ±10%
L6 1 μH ±10%
L7 1 μH ±10%
L8 1 μH ±10%
R38 91 ±2%,1/2W
R41 91 ±2% 1/2W
R49 91 ±2%,1/2W
R52 91 ±2% 1/2W
R39 1K
R42 1K
R50 1K
R53 1K
C36 68PF
C37 68PF
C38 68PF
C39 68PF
R43 422 ±1% .1W
R44 422 ±1% .1W
R54 422 ±1% .1W
R55 422 ±1% .1W
R60 2150 ±1% .1W
R61 2150 ±1% .1W
R62 2150 ±1% .1W
R63 2150 ±1% .1W
C27 .01
C28 .01
C32 .01
C33 .01
R45 100K
R46 100K
R56 100K
R57 100K
U35 (1514)
U19 (1514)
+12V
C17 4 D5
(9016) U18
U23-5 3 E7
U23-6 3 E7
U23-7 3 E7
U23-9 3 E7
C29 10PF 500V
C30 10PF 500V
C34 10PF 500V
C35 10PF 500V
R47 5110 ±1% .1W
R48 5110 ±1% .1W
R58 5110 ±1% .1W
R59 5110 ±1% .1W
+5V
(S4123)
U14
U13
V1
R
73 RST5 −
59 IGRP5D
71 RST6 −
60 IGRP6D
72 RST7 −
61 IGRP7D
75 RST8 −
62 IGRP8D
8
7
6
5
4
3
2
1
F
E
D
C

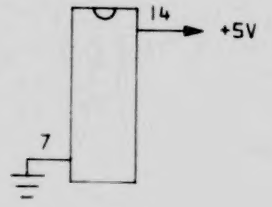
Figure FO-12. GTM card 21A2, schematic diagram (sheet 5 of 5).

EXPANDED LOGIC SYMBOL


(9334)
SEL
X → Y
3 A2 4
2 A1 2
1 A0 1
7 G7
6 G6
5 G5
4 G4
3 G3
2 G2
1 G1
0 G0
15 C G10
14 E G9
G8
13 D
7,9
8,10
6,9
8,10
5,9
8,10
4,9
8,10
3,9
8,10
2,9
8,10
1,9
8,10
0,9
8,10
Q7 12
Q6 11
Q5 10
Q4 9
Q3 7
Q2 6
Q1 5
Q0 4

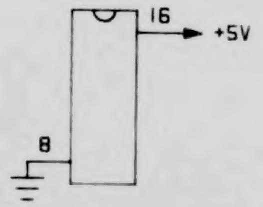
HIGHEST REFERENCE DESIGNATION USED	
C16	P1
CR1	R16
Q2	TP9
VR1	U28

REFERENCE DESIGNATIONS NOT USED
U3,U5,U24 C14



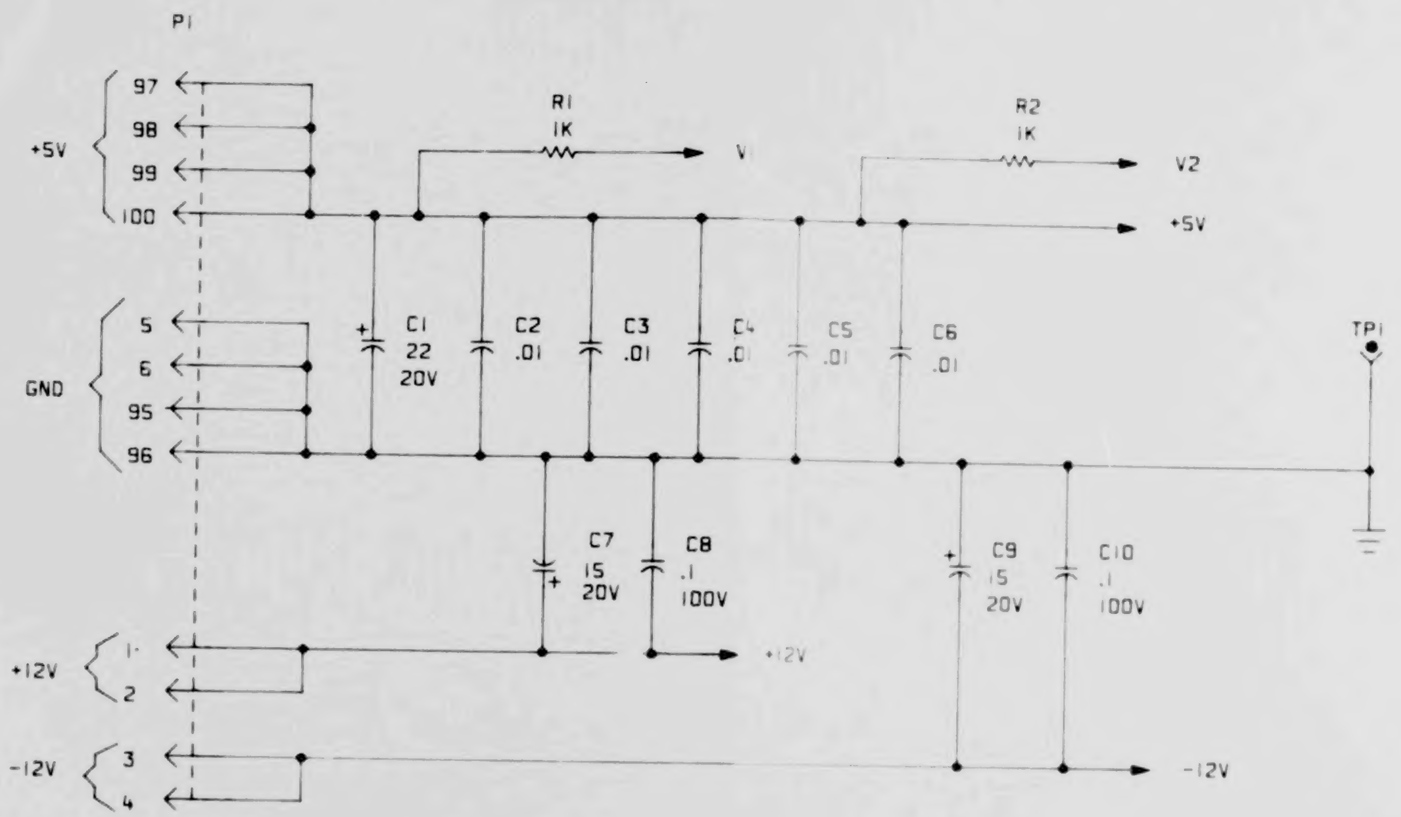
TYPICAL

U1,U18	SM-A-942000	(9002)
U10	SM-A-942001	(9003)
U8	SM-A-942004	(9009)
U7,U14,U17,U19	M38510/00805BCB	(5426)
U21,U22,U26	M38510/00805BCB	(5426)
U12,U13,U23	SM-A-942007	(9016)
U16	SM-A-942003	(9007)



TYPICAL

U27	M38510/01203BEB	(54123)
U20	SM-A-942015	(9024)
U2,U6,U25	SM-A-942006	(9015)
U4,U9,U11	SM-A-942030	(9334)
U15	SM-A-942005	(9014)


P1
+5V
97
98
99
100
R1
1K
V
R2
1K
V2
+5V
GND
5
6
95
96
C1
22
20V
C2
.01
C3
.01
C4
.01
C5
.01
C6
.01
TP1
C7
15
20V
C8
.1
100V
C9
15
20V
C10
.1
100V
+12V
1
2
+12V
-12V
3
4
-12V

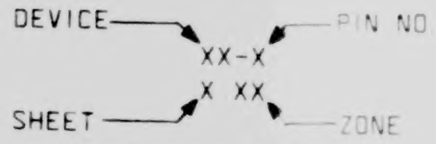
NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

4. CIRCUIT CONTINUATION DESTINATION.


DEVICE
PIN NO.
XX-X
X XX
SHEET
ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.

Figure FO-13. AD card 21A1, schematic diagram (sheet 1 of 5).

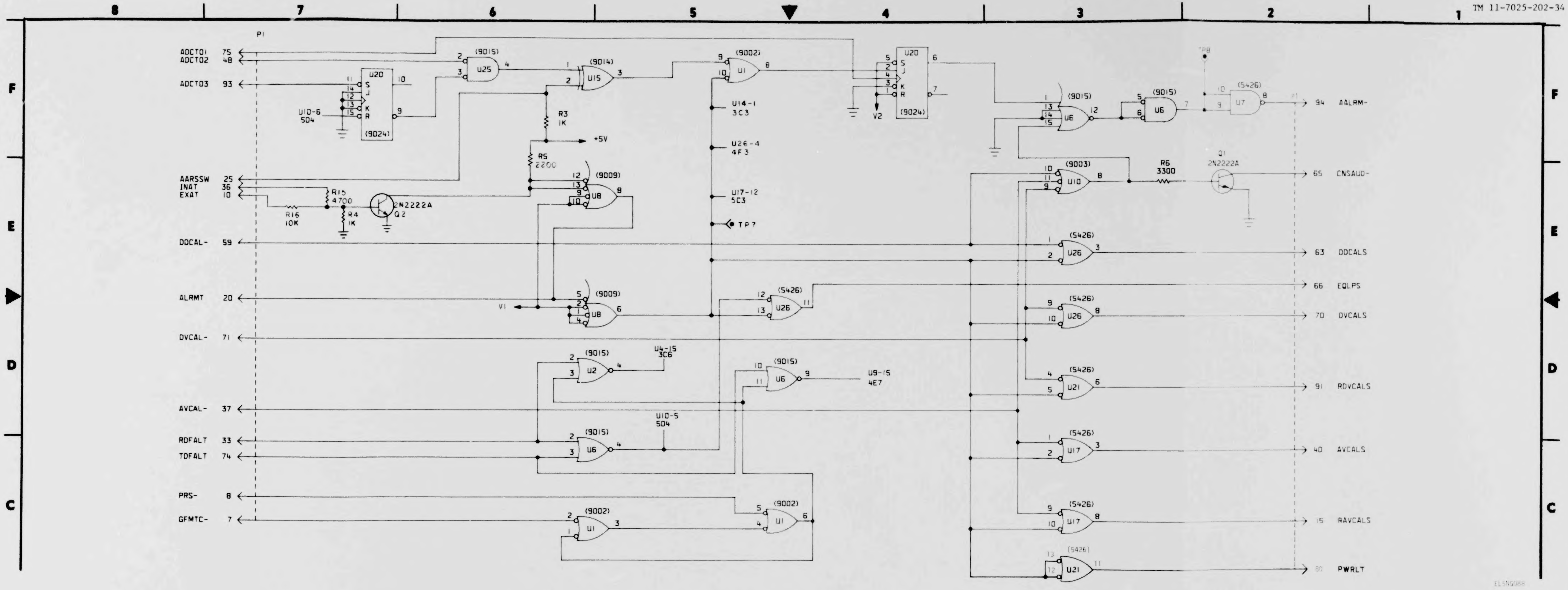

8
7
6
5
4
3
2
1
F
E
D
C
P1
ADCT01 75
ADCT02 48
ADCT03 93
AARSSW 25
INAT 36
EXAT 10
DDCAL- 59
ALRMT 20
DVCAL- 71
AVCAL- 37
RDFALT 33
TDFALT 74
PRS- 8
GFMTC- 7
U20 (9024)
U10-6 5D4
U25 (9015)
U15 (9014)
U1 (9002)
U14-1 3C3
U26-4 4F3
U17-12 5C3
TP7
R3 1K
+5V
R5 2200
R15 4700
R16 10K
R4 1K
2N2222A Q2
U8 (9009)
V1
U26 (5426)
U2 (9015)
U4-15 3C6
U6 (9015)
U10-5 5D4
U9-15 4E7
V2
TP8
U7 (5426)
U10 (9003)
R6 3300
Q1 2N2222A
U17 (5426)
U21 (5426)
94 AALRM-
65 CNSAUD-
63 DDCALS
66 EQLPS
70 DVCALS
91 RDVCALS
40 AVCALS
15 RAVCALS
80 PWRLT
EL5NG088

Figure FO-13. AD card 21A1, schematic diagram (sheet 2 of 5).

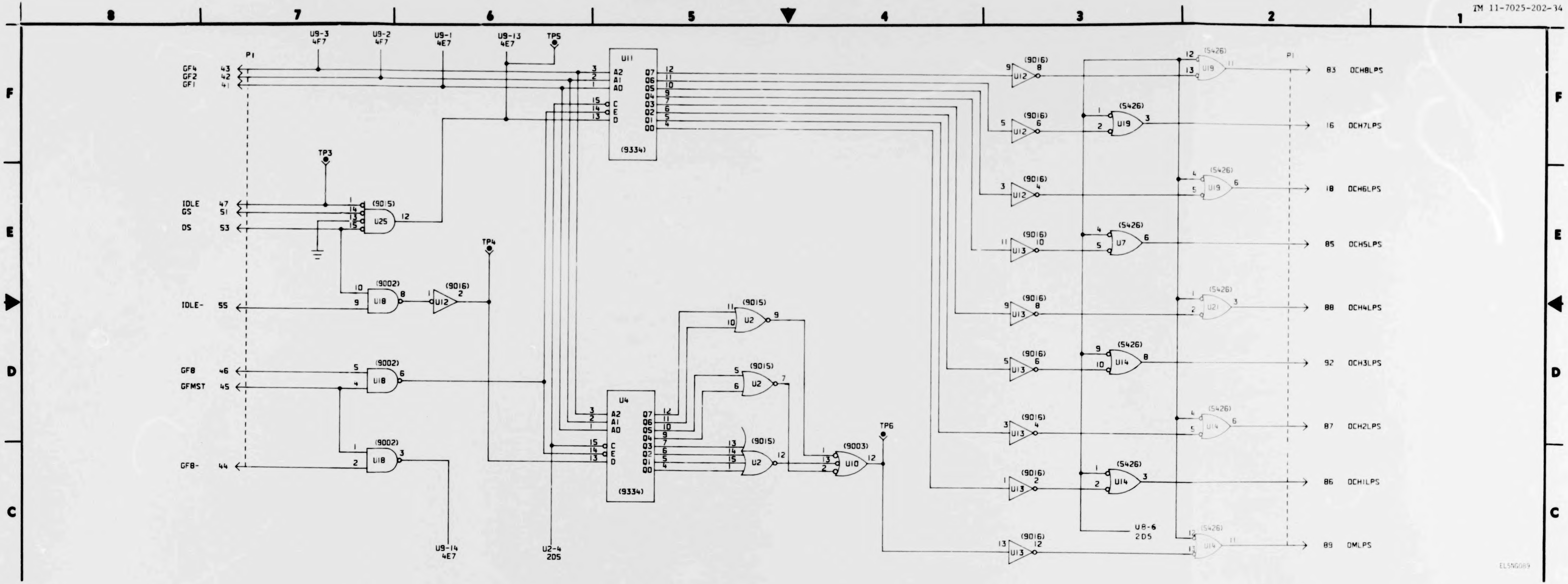

8
7
6
5
4
3
2
1
F
E
D
C
P1
GF4 43
GF2 42
GF1 41
U9-3 4E7
U9-2 4E7
U9-1 4E7
U9-13 4E7
TP5
U11
(9334)
A2
A1
A0
C
E
D
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
TP3
IDLE 47
GS 51
DS 53
(9015)
U25
TP4
(9002)
U18
(9016)
U12
IDLE- 55
GF8 46
GFMST 45
GF8- 44
U9-14 4E7
U2-4 2D5
U4
(9334)
U2
(9015)
(9003)
U10
TP6
U13
(S426)
U19
U7
U21
U14
U8-6 2D5
83 OCH8LPS
16 OCH7LPS
18 OCH6LPS
85 OCH5LPS
88 OCH4LPS
92 OCH3LPS
87 OCH2LPS
86 OCH1LPS
89 OMLPS
EL5NG089

Figure FO-13. AD card 21A1, schematic diagram (sheet 3 of 5).

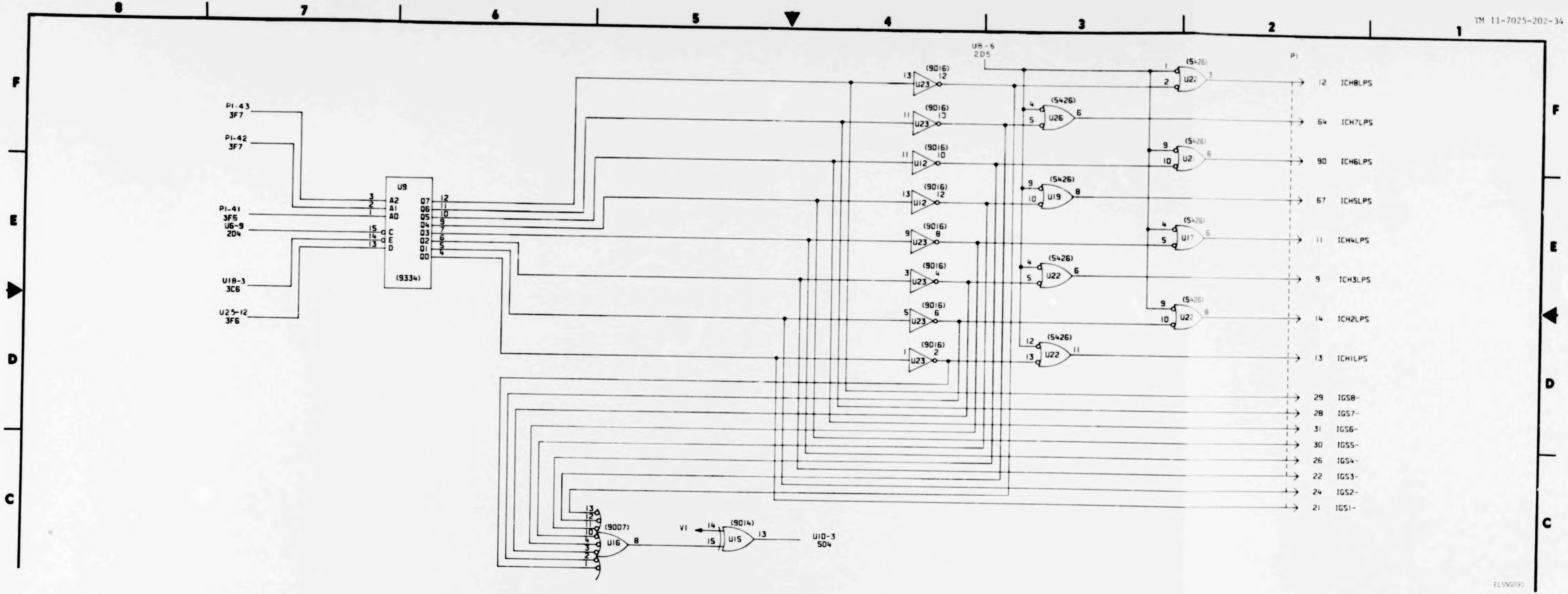

8
7
6
5
4
3
2
1
F
E
D
C
P1-43
3F7
P1-42
3F7
P1-41
3F6
U6-9
2D4
U18-3
3C6
U25-12
3F6
U9
(9334)
A2
A1
A0
C
E
D
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
U8-6
2D5
(9016)
U23
U12
(5426)
U22
U26
U21
U19
U17
P1
12 ICH8LPS
64 ICH7LPS
90 ICH6LPS
67 ICH5LPS
11 ICH4LPS
9 ICH3LPS
14 ICH2LPS
13 ICH1LPS
29 IGS8-
28 IGS7-
31 IGS6-
30 IGS5-
26 IGS4-
22 IGS3-
24 IGS2-
21 IGS1-
(9007)
U16
V1
(9014)
U15
U10-3
5D4
EL5NG090

Figure FO-13. AD card 21A1, schematic diagram (sheet 4 of 5).

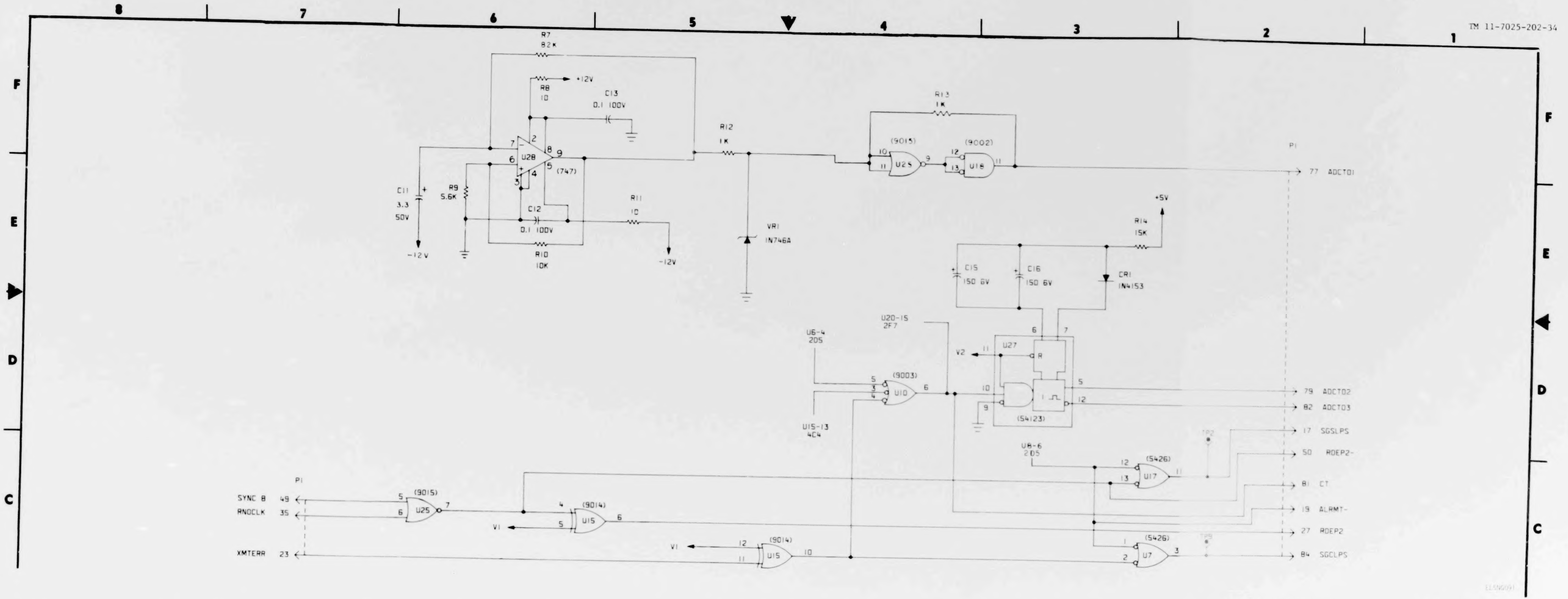
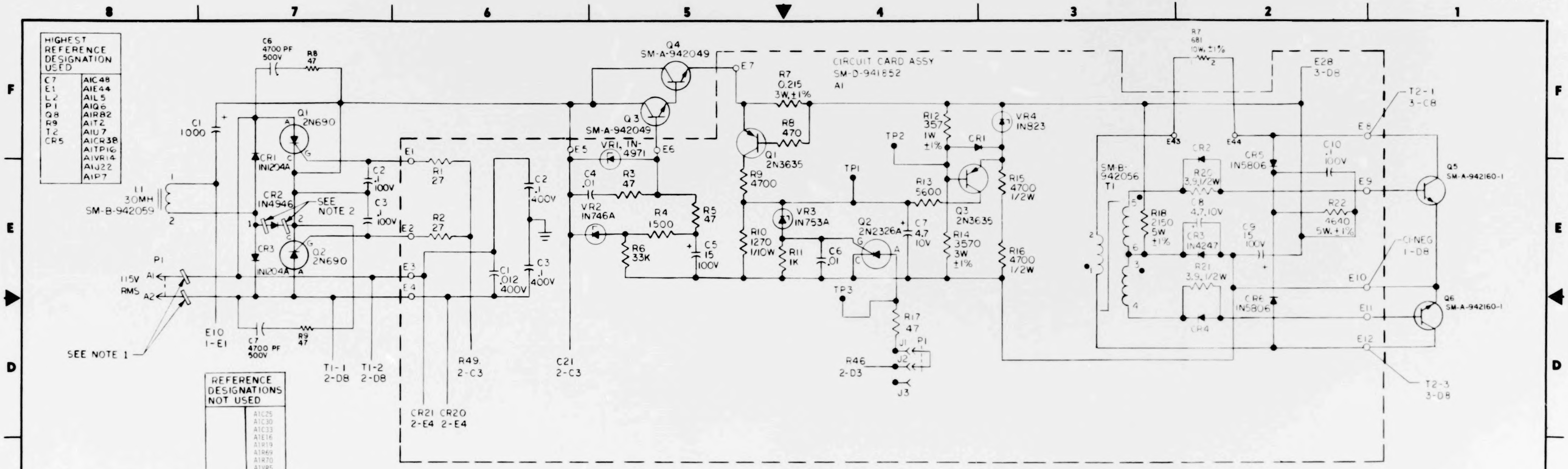

8
7
6
5
4
3
2
1
F
E
D
C
R7
82K
R8
10
+12V
C13
0.1 100V
U28
(747)
C11
3.3
50V
-12V
R9
5.6K
C12
0.1 100V
R10
10K
R11
10
-12V
R12
1K
VR1
1N746A
R13
1K
(9015)
U25
(9002)
U18
P1
77 ADCT01
+5V
R14
15K
C15
150 6V
C16
150 6V
CR1
1N4153
U20-15
2F7
U6-4
2D5
(9003)
U10
U27
V2
R
(54123)
U15-13
4C4
79 ADCT02
82 ADCT03
17 SGSLPS
50 RDEP2-
U8-6
2D5
(5426)
U17
TP2
81 CT
19 ALRMT-
27 RDEP2
(5426)
U7
TP9
84 SGCLPS
P1
SYNC 8 49
RNOCLK 35
XMTERR 23
(9015)
U25
(9014)
U15
V1
(9014)
U15
V1
EL5NG091

Figure FO-13. AD card 21A1, schematic diagram (sheet 5 of 5).


8
7
6
5
4
3
2
1
F
E
D
C
C6 4700 PF 500V
R8 47
C1 1000
Q1 2N690
CR1 IN1204A
CR2 IN4946
SEE NOTE 2
CR3 IN1204A
Q2 2N690
L1 30MH SM-B-942059
P1
115V RMS
A1
A2
E10 1-E1
C7 4700 PF 500V
R9 47
SEE NOTE 1
C2 .1 100V
C3 .1 100V
E1
E2
E3
E4
R1 27
R2 27
C2 .1 400V
C1 .012 400V
C3 .1 400V
T1-1 2-D8
T1-2 2-D8
R49 2-C3
CR21 2-E4
CR20 2-E4
Q4 SM-A-942049
Q3 SM-A-942049
E5
E6
E7
VR1 IN-4971
C4 .01
R3 47
VR2 IN746A
R4 1500
R5 47
R6 33K
C5 15 100V
C21 2-C3
CIRCUIT CARD ASSY SM-D-941852 A1
R7 0.215 3W, ±1%
R8 470
Q1 2N3635
R9 4700
R10 1270 1/10W
VR3 IN753A
R11 1K
C6 .01
Q2 2N2326A
TP1
TP2
TP3
R12 357 1W ±1%
CR1
VR4 IN823
R13 5600
C7 4.7 10V
Q3 2N3635
R14 3570 3W ±1%
R15 4700 1/2W
R16 4700 1/2W
R17 47
J1
J2
J3
P1
R46 2-D3
R7 681 10W, ±1%
E43
E44
E28 3-D8
SM-B-942056 T1
R18 2150 5W ±1%
CR2
R20 3.9, 1/2W
C8 4.7, 10V
CR3 IN4247
R21 3.9, 1/2W
CR4
CR5 IN5806
CR6 IN5806
C10 .1 100V
C9 15 100V
R22 4640 5W, ±1%
E8
E9
E10
E11
E12
T2-1 3-C8
-C(-NEG 1-D8
T2-3 3-D8
Q5 SM-A-942160-1
Q6 SM-A-942160-1

HIGHEST REFERENCE DESIGNATION USED	
C7	A1C48
E1	A1E44
L2	A1L5
P1	A1Q6
Q8	A1R82
R9	A1T2
T2	A1U7
CR5	A1CR38
	A1TP16
	A1VR14
	A1J22
	A1P7

REFERENCE DESIGNATIONS NOT USED	
	A1C25 A1C30 A1C33 A1E16 A1R19 A1R69 A1R70 A1VR5 A1VR6

NOTES:

1. FERRITE BEAD SM-A-942085-2 ON LEADS BETWEEN P1-A1 AND E3 AND P1-A2 AND E4.
2. FERRITE BEAD SM-A-942085-1 ON BOTH SIDES OF CR2.
3. ALL ± 1 PERCENT RESISTORS ARE WIREWOUND.
4. ALL DIODES ARE IN4153-1 UNLESS OTHERWISE SPECIFIED.
5. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), 200V UNLESS OTHERWISE SPECIFIED.
6. ALL RESISTANCE VALUES ARE IN OHMS, ± 5 PERCENT 1/4W UNLESS OTHERWISE SPECIFIED.
7. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NUMBER AND / OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
8. CIRCUIT CONTINUATION DESTINATION

DEVICE — XX-X — PIN NO.
SHEET — X-XX — ZONE

EL5NG092

Figure FO-14. Power supply 21A12, schematic diagram (sheet 1 of 4).

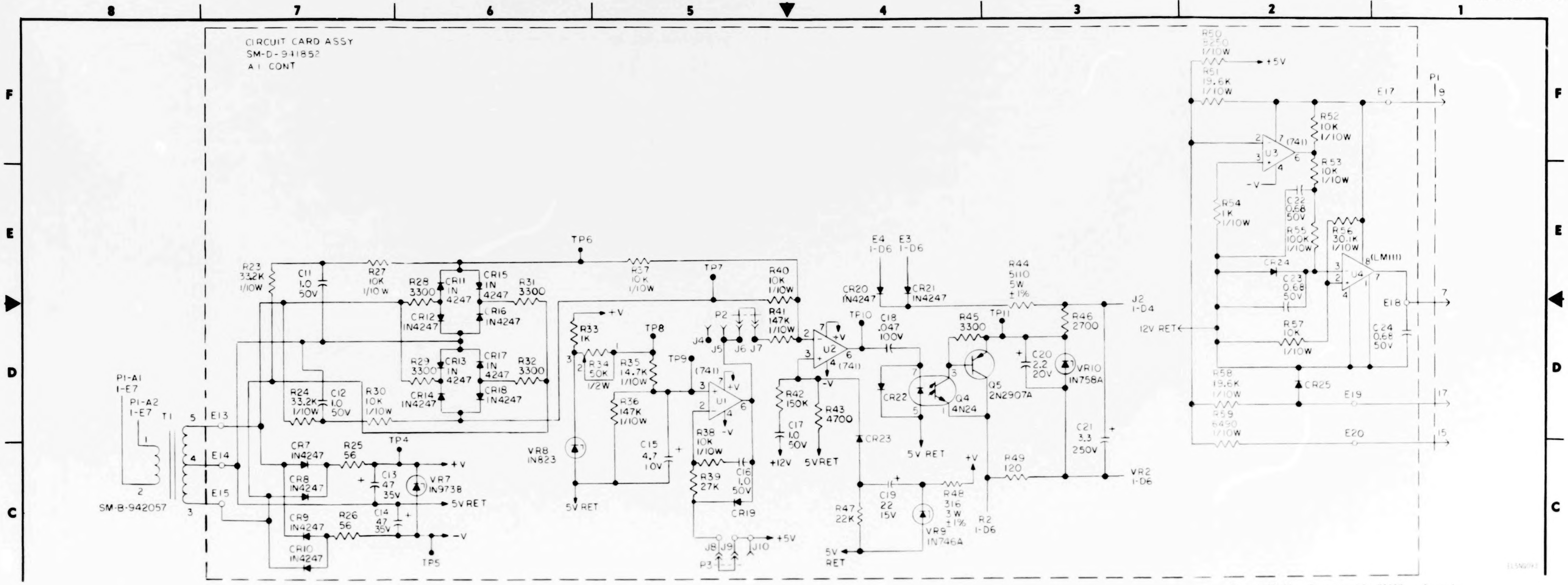

8
7
6
5
4
3
2
1
F
E
D
C
CIRCUIT CARD ASSY
SM-D-941852
A1 CONT
R50
8250
1/10W
+5V
R51
19.6K
1/10W
P1
9
E17
R52
10K
1/10W
U3
(741)
R53
10K
1/10W
-V
C22
0.68
50V
R54
1K
1/10W
R55
100K
1/10W
R56
30.1K
1/10W
(LM111)
U4
CR24
C23
0.68
50V
E18
7
C24
0.68
50V
R57
10K
1/10W
12V RET
R58
19.6K
1/10W
CR25
E19
17
R59
6490
1/10W
E20
15
TP6
R23
33.2K
1/10W
C11
1.0
50V
R27
10K
1/10W
R28
3300
CR11
IN
4247
CR15
IN
4247
R31
3300
CR12
IN4247
CR16
IN4247
R29
3300
CR13
IN
4247
CR17
IN
4247
R32
3300
CR14
IN4247
CR18
IN4247
R24
33.2K
1/10W
C12
1.0
50V
R30
10K
1/10W
P1-A1
1-E7
P1-A2
1-E7
T1
SM-B-942057
E13
E14
E15
CR7
IN4247
R25
56
TP4
+V
CR8
IN4247
C13
47
35V
VR7
IN9738
5V RET
CR9
IN4247
R26
56
C14
47
35V
-V
CR10
IN4247
TP5
R37
10K
1/10W
TP7
R40
10K
1/10W
+V
R33
1K
R34
50K
1/2W
R35
14.7K
1/10W
TP8
TP9
(741)
U1
R36
147K
1/10W
VR8
IN823
5V RET
C15
4.7
10V
R38
10K
1/10W
C16
1.0
50V
R39
27K
CR19
J8
J9
J10
+5V
P3
P2
J4
J5
J6
J7
R41
147K
1/10W
U2
(741)
R42
150K
C17
1.0
50V
+12V
R43
4700
5V RET
E4
1-D6
E3
1-D6
CR20
IN4247
CR21
IN4247
TP10
C18
.047
100V
CR22
Q4
4N24
5V RET
CR23
C19
22
15V
R47
22K
5V
RET
VR9
IN746A
R48
316
3W
±1%
+V
R45
3300
TP11
Q5
2N2907A
R2
1-D6
R44
5110
5W
±1%
C20
2.2
20V
VR10
IN758A
R46
2700
J2
1-D4
R49
120
C21
3.3
250V
VR2
1-D6
115NG093

Figure FO-14. Power supply 21A12, schematic diagram (sheet 2 of 4).

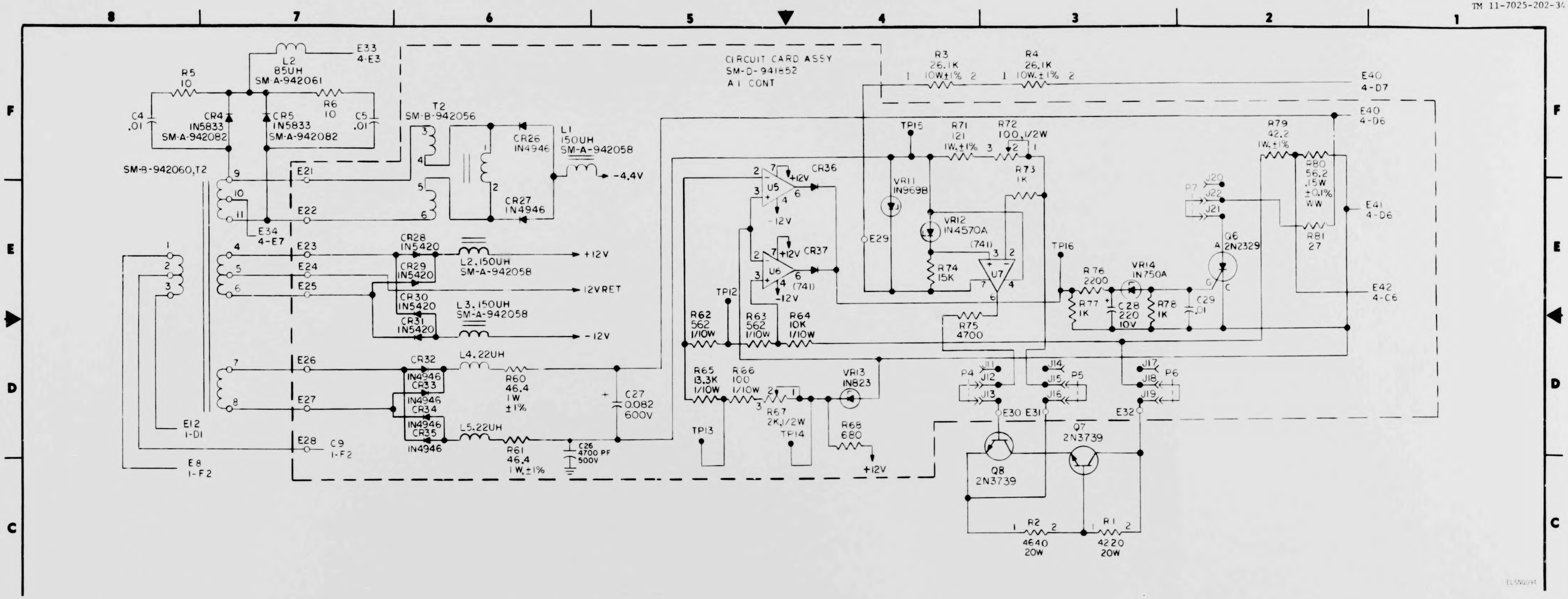

8
7
6
5
4
3
2
1
F
E
D
C
CIRCUIT CARD ASSY
SM-D-941852
A1 CONT
L2
85UH
SM-A-942061
E33
4-E3
R5
10
R6
10
C4
.01
C5
.01
CR4
1N5833
SM-A-942082
CR5
1N5833
SM-A-942082
SM-B-942060,T2
T2
SM-B-942056
CR26
1N4946
CR27
1N4946
L1
150UH
SM-A-942058
-4.4V
E21
E22
E34
4-E7
E23
E24
E25
CR28
1N5420
CR29
1N5420
CR30
1N5420
CR31
1N5420
L2,150UH
SM-A-942058
L3,150UH
SM-A-942058
+12V
12VRET
-12V
E26
E27
E28
C9
1-F2
E12
1-D1
E8
1-F2
CR32
1N4946
CR33
1N4946
CR34
1N4946
CR35
1N4946
L4,22UH
L5,22UH
R60
46.4
1W
±1%
R61
46.4
1W,±1%
C26
4700 PF
500V
C27
0.082
600V
R3
26.1K
10W±1%
R4
26.1K
10W,±1%
E40
4-D7
E40
4-D6
TP15
R71
121
1W,±1%
R72
100,1/2W
R73
1K
VR11
1N969B
VR12
1N4570A
R74
15K
U7
(741)
E29
TP16
U5
CR36
+12V
-12V
U6
CR37
(741)
TP12
R62
562
1/10W
R63
562
1/10W
R64
10K
1/10W
R75
4700
R65
13.3K
1/10W
R66
100
1/10W
R67
2K,1/2W
TP13
TP14
VR13
1N823
R68
680
+12V
R76
2200
VR14
1N750A
R77
1K
C28
220
10V
R78
1K
C29
.01
Q6
2N2329
R79
42.2
1W,±1%
R80
56.2
.15W
±0.1%
WW
R81
27
E41
4-D6
E42
4-C6
P7
J20
J22
J21
P4
J11
J12
J13
J14
J15
J16
P5
J17
J18
J19
P6
E30
E31
E32
Q7
2N3739
Q8
2N3739
R2
4640
20W
R1
4220
20W
EL5NG094

Figure FO-14. Power supply 21A12, schematic diagram (sheet 3 of 4).

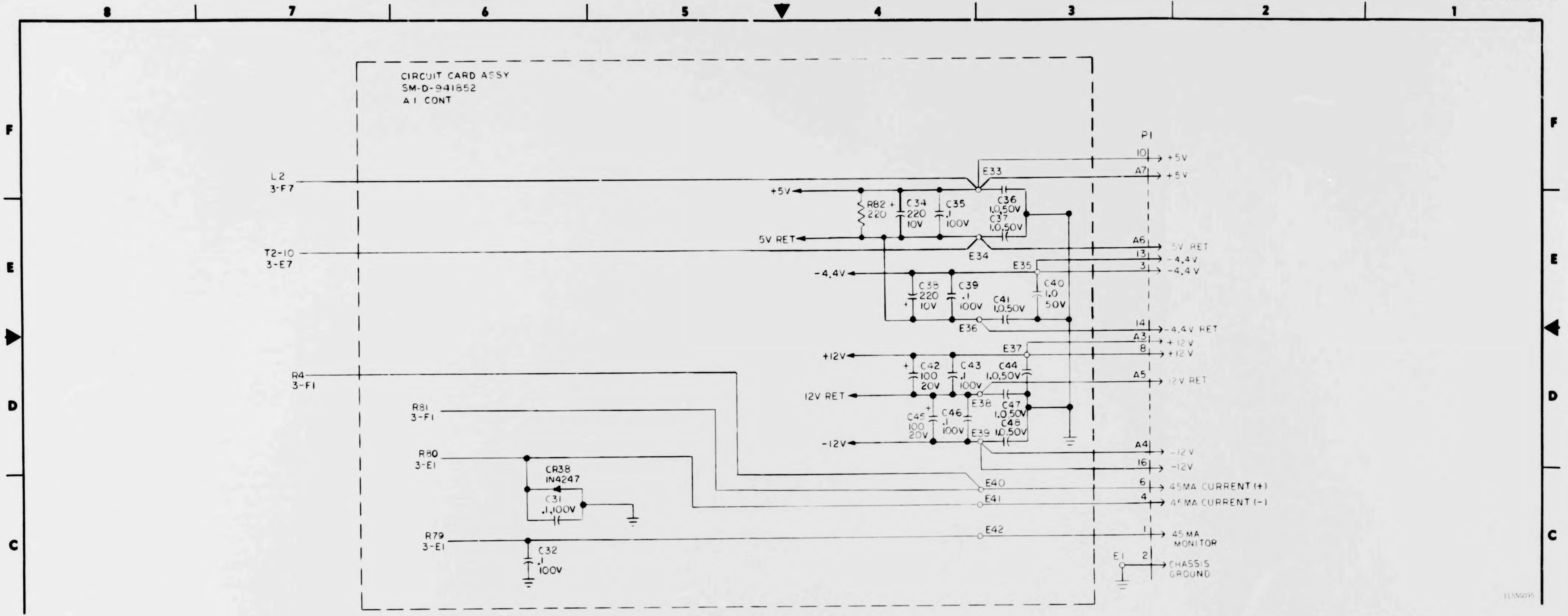
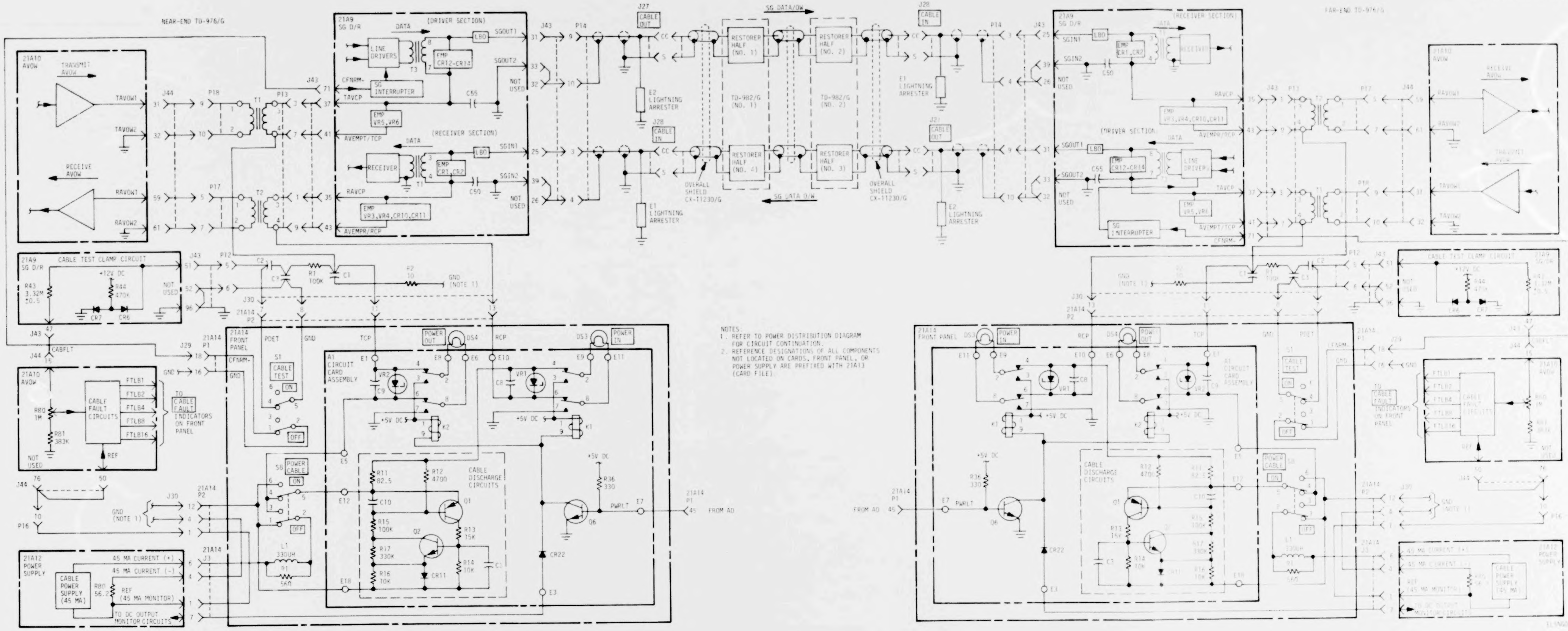

8
7
6
5
4
3
2
1
F
E
D
C
CIRCUIT CARD ASSY
SM-D-941852
A1 CONT
L2
3-F7
T2-10
3-E7
R4
3-F1
R81
3-F1
R80
3-E1
CR38
1N4247
C31
.1,100V
R79
3-E1
C32
.1
100V
+5V
5V RET
-4.4V
+12V
12V RET
-12V
R82
220
C34
220
10V
C35
.1
100V
C36
1.0,50V
C37
1.0,50V
E33
E34
E35
E36
E37
E38
E39
E40
E41
E42
C38
220
10V
C39
.1
100V
C40
1.0
50V
C41
1.0,50V
C42
100
20V
C43
.1
100V
C44
1.0,50V
C45
100
20V
C46
.1
100V
C47
1.0,50V
C48
1.0,50V
P1
10
A7
A6
13
3
14
A3
8
A5
A4
16
6
4
1
2
E1
+5V
+5V
5V RET
-4.4V
-4.4V
-4.4V RET
+12V
+12V
12V RET
-12V
-12V
45MA CURRENT (+)
45MA CURRENT (-)
45MA
MONITOR
CHASSIS
GROUND
EL5NG095

Figure FO-14. Power supply 21A12, schematic diagram (sheet 4 of 4).


NEAR-END TD-976/G
FAR-END TD-976/G
21A10 AVOW
TRANSMIT AVOW
RECEIVE AVOW
21A9 SG D/R
DRIVER SECTION
RECEIVER SECTION
LINE DRIVERS
RECEIVER
SG INTERRUPTER
J27 CABLE OUT
J28 CABLE IN
E1 LIGHTNING ARRESTER
E2 LIGHTNING ARRESTER
RESTORER HALF (NO. 1)
RESTORER HALF (NO. 2)
RESTORER HALF (NO. 3)
RESTORER HALF (NO. 4)
TD-982/G (NO. 1)
TD-982/G (NO. 2)
SG DATA/OW
SG DATA O/W
OVERALL SHIELD CX-11230/G
CABLE TEST CLAMP CIRCUIT
21A14 FRONT PANEL
A1 CIRCUIT CARD ASSEMBLY
CABLE DISCHARGE CIRCUITS
CABLE FAULT CIRCUITS
TO CABLE FAULT INDICATORS ON FRONT PANEL
21A12 POWER SUPPLY
CABLE POWER SUPPLY (45 MA)
45 MA CURRENT (+)
45 MA CURRENT (-)
REF (45 MA MONITOR)
TO DC OUTPUT MONITOR CIRCUITS
S1 CABLE TEST
S6 POWER CABLE
POWER OUT
POWER IN
FROM AD
GND (NOTE 1)

NOTES:
1. REFER TO POWER DISTRIBUTION DIAGRAM FOR CIRCUIT CONTINUATION.
2. REFERENCE DESIGNATIONS OF ALL COMPONENTS NOT LOCATED ON CARDS, FRONT PANEL, OR POWER SUPPLY ARE PREFIXED WITH 21A13 (CARD FILE).

Figure FO-15. Typical cable system interfaces.

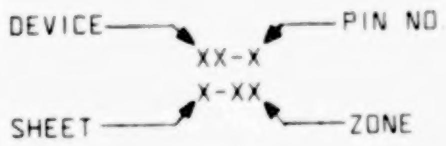
NOTES:

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.

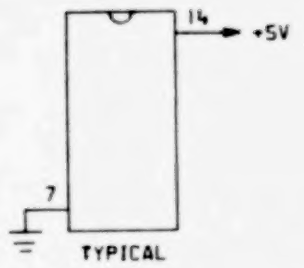
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.

3. ALL CAPACITANCE VALUES ARE IN MICROFARADS (UF), ±10 PERCENT, 200 VOLTS UNLESS OTHERWISE SPECIFIED.

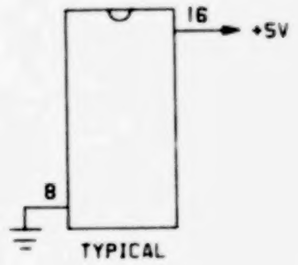
4. CIRCUIT CONTINUATION DESTINATION.


DEVICE
PIN NO.
XX-X
X-XX
SHEET
ZONE

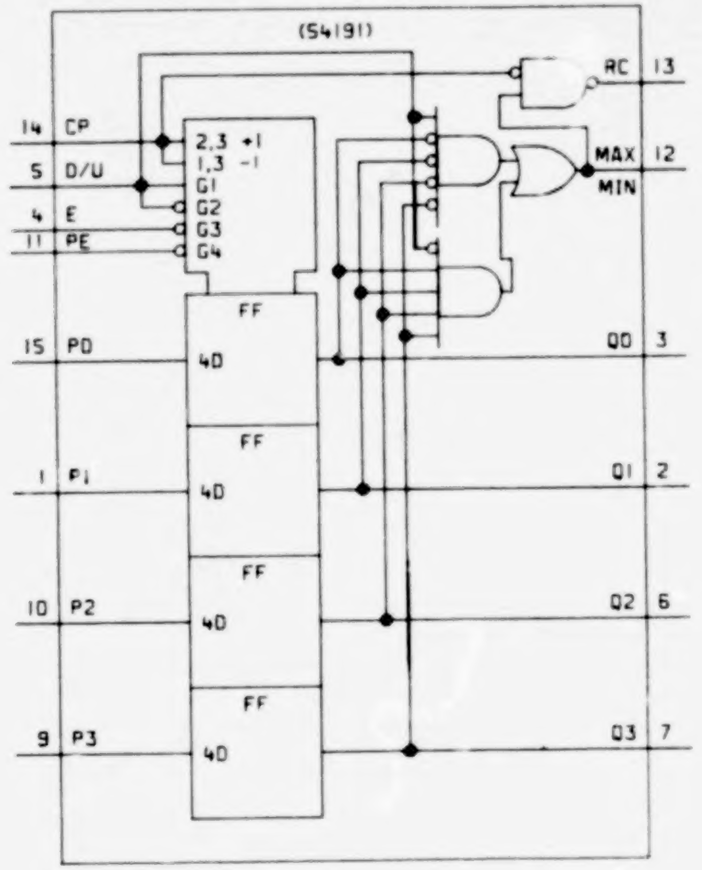
5. GENERIC NOMENCLATURE FOR MICROCIRCUITS ARE SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.


14
+5V
7
TYPICAL

U2,U30,U32	SM-A-942000	(9002)


16
+5V
8
TYPICAL

U1	SM-A-942015	(9024)
U8,U22	SM-A-942025	(54191)
U29 U34,U35	SM-A-942006	(9015)


(54191)
14 CP
5 D/U
4 E
11 PE
2,3 +1
1,3 -1
G1
G2
G3
G4
RC 13
MAX 12
MIN
FF
15 PD
4D
QD 3
1 P1
Q1 2
10 P2
Q2 6
9 P3
Q3 7

HIGHEST REFERENCE DESIGNATION USED	
C56 CR7 Q11 R106 VR4	P1 U35
REFERENCE DESIGNATIONS NOT USED	
U5-7 U11-14 U16 U18-20 U23 U24	U26-28 U31 U33

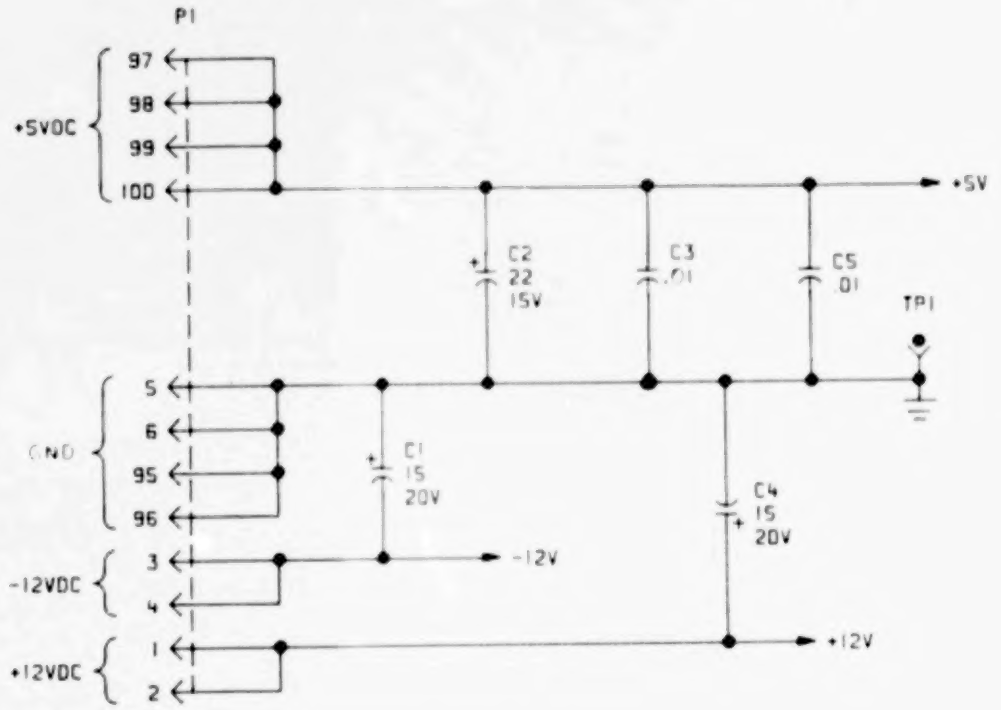

P1
+5VDC
97
98
99
100
+5V
C2
22
15V
C3
.01
C5
.01
TP1
GND
5
6
95
96
C1
15
20V
C4
15
20V
-12VDC
3
4
-12V
+12VDC
1
2
+12V

Figure FO-16. AVOW card 21A10, schematic diagram (sheet 1 of 5).

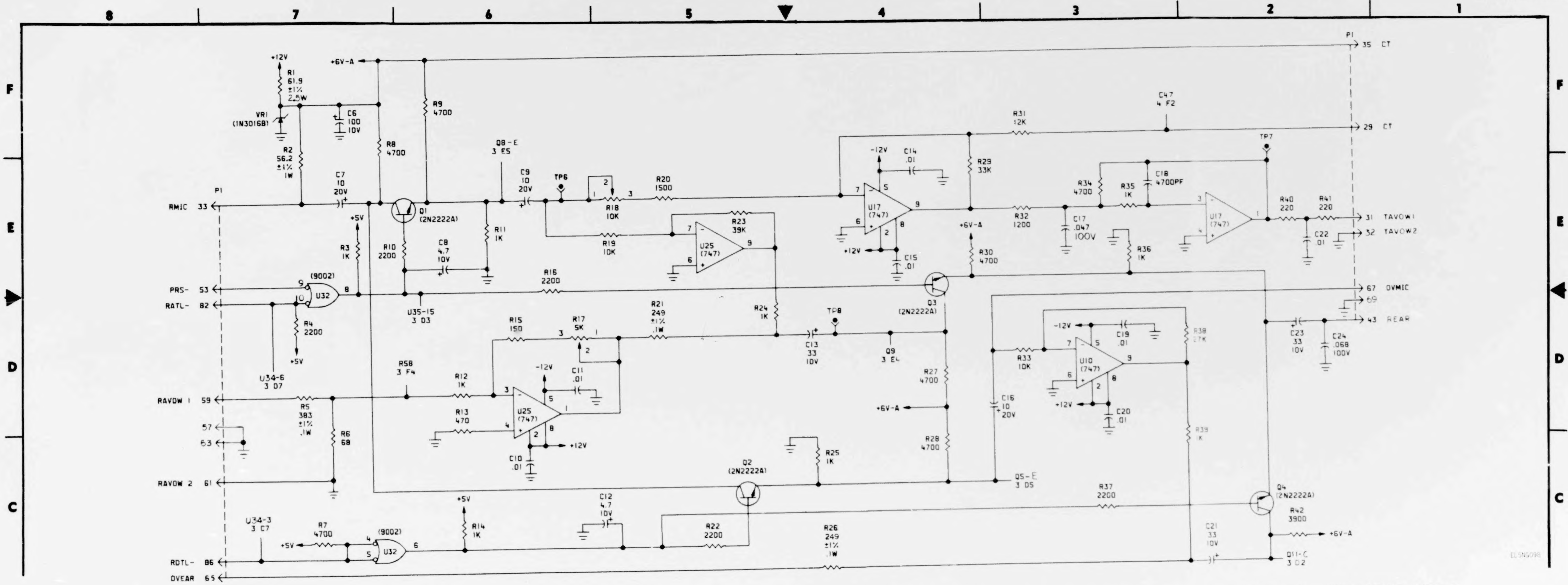

8
7
6
5
4
3
2
1
F
E
D
C
P1
35 CT
29 CT
31 TAVOW1
32 TAVOW2
67 OVMIC
69
43 REAR
+12V
R1
61.9
±1%
2.5W
VR1
(1N3016B)
C6
100
10V
R2
56.2
±1%
1W
+6V-A
R9
4700
R8
4700
Q8-E
3 E5
C7
10
20V
RMIC 33
Q1
(2N2222A)
C9
10
20V
TP6
R18
10K
R20
1500
R23
39K
R19
10K
U25
(747)
R10
2200
C8
4.7
10V
R11
1K
+5V
R3
1K
(9002)
U32
PRS- 53
RATL- 82
R16
2200
U35-15
3 D3
R4
2200
U34-6
3 D7
R15
150
R17
5K
R21
249
±1%
.1W
R24
1K
TP8
C13
33
10V
Q9
3 E4
R58
3 F4
R12
1K
R13
470
-12V
C11
.01
C10
.01
+12V
RAVOW 1 59
R5
383
±1%
.1W
R6
68
57
63
RAVOW 2 61
-12V
C14
.01
U17
(747)
C15
.01
R29
33K
R31
12K
C47
4 F2
R32
1200
C17
.047
100V
R30
4700
Q3
(2N2222A)
R27
4700
R28
4700
R25
1K
Q2
(2N2222A)
TP7
C18
4700PF
R34
4700
R35
1K
R36
1K
R40
220
R41
220
C22
.01
R38
27K
C19
.01
R33
10K
U10
(747)
C16
10
20V
C20
.01
R39
1K
C23
33
10V
C24
.068
100V
Q5-E
3 D5
R37
2200
Q4
(2N2222A)
R42
3900
C21
33
10V
Q11-C
3 D2
U34-3
3 C7
R7
4700
R14
1K
C12
4.7
10V
R22
2200
R26
249
±1%
.1W
RDTL- 86
OVEAR 65
EL5NG098

Figure FO-16. AVOW card 21A10, schematic diagram (sheet 2 of 5).

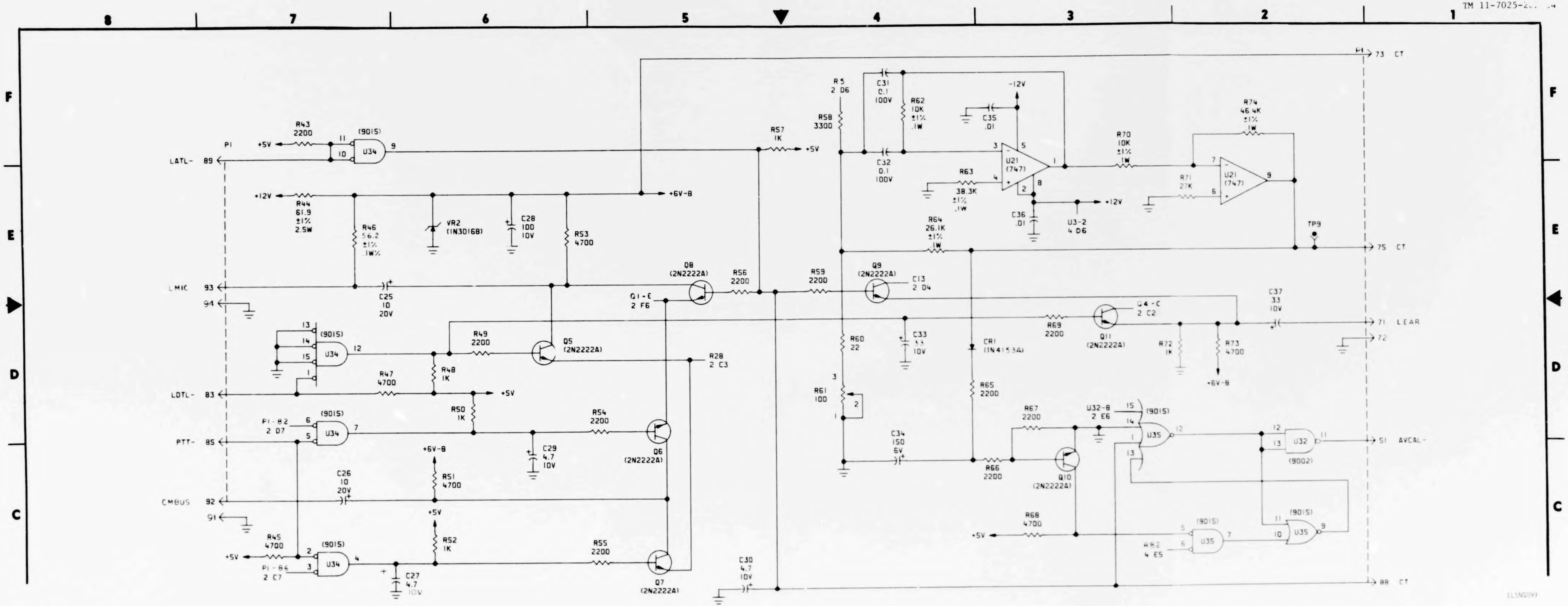

8
7
6
5
4
3
2
1
F
E
D
C
P1
LATL- 89
+5V
R43 2200
11
10
(9015)
U34
9
+12V
R44 61.9 ±1% 2.5W
R46 56.2 ±1% .1W%
VR2 (1N3016B)
C28 100 10V
R53 4700
+6V-B
R57 1K
+5V
LMIC 93
94
C25 10 20V
Q8 (2N2222A)
Q1-E 2 F6
R56 2200
R59 2200
Q9 (2N2222A)
C13 2 D4
13
14
15
(9015)
U34
12
1
R49 2200
Q5 (2N2222A)
R48 1K
R28 2 C3
LDTL- 83
R47 4700
+5V
R50 1K
P1-82 2 D7
6
5
(9015)
U34
7
R54 2200
PTT- 85
C29 4.7 10V
Q6 (2N2222A)
+6V-B
R51 4700
C26 10 20V
CMBUS 92
91
+5V
R52 1K
R45 4700
+5V
2
3
(9015)
U34
4
P1-86 2 C7
C27 4.7 10V
R55 2200
Q7 (2N2222A)
C30 4.7 10V
R5 2 D6
R58 3300
C31 0.1 100V
R62 10K ±1% .1W
-12V
C35 .01
C32 0.1 100V
R63 38.3K ±1% .1W
3
5
4
2
8
U21 (747)
1
C36 .01
+12V
U3-2 4 D6
R70 10K ±1% .1W
R74 46.4K ±1% .1W
R71 27K
7
6
U21 (747)
9
TP9
R64 26.1K ±1% .1W
P1
73 CT
75 CT
C37 33 10V
Q4-C 2 C2
R69 2200
Q11 (2N2222A)
R72 1K
R73 4700
+6V-B
71 LEAR
72
R60 22
C33 33 10V
CR1 (1N4153A)
3
R61 100
2
1
R65 2200
R67 2200
U32-B 2 E6
15
14
1
13
(9015)
U35
12
12
13
U32
(9002)
11
51 AVCAL-
C34 150 6V
R66 2200
Q10 (2N2222A)
R68 4700
+5V
R82 4 E5
5
6
(9015)
U35
7
11
10
(9015)
U35
9
88 CT
EL5NG099

Figure FO-16. AVOW card 21A10, schematic diagram (sheet 3 of 5).

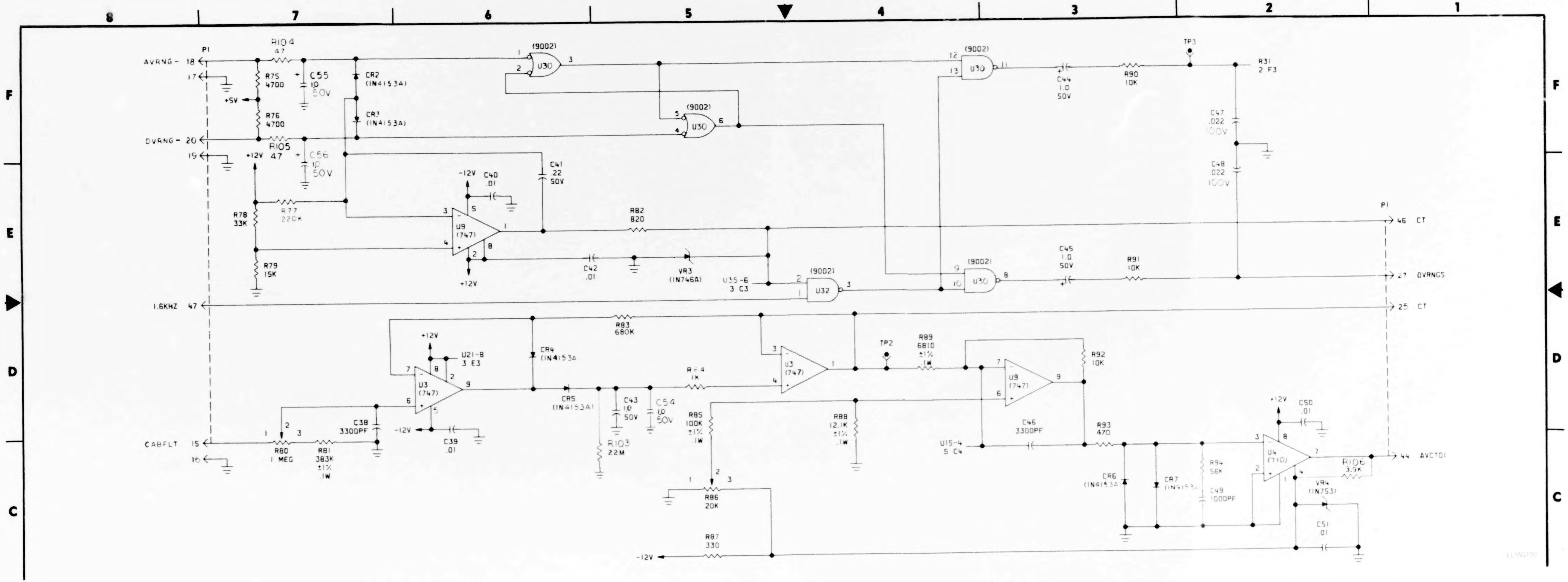

8
7
6
5
4
3
2
1
F
E
D
C
P1
AVRNG- 18
17
DVRNG- 20
19
+5V
+12V
R104
47
R105
47
R75
4700
R76
4700
C55
10
50V
C56
10
50V
CR2
(IN4153A)
CR3
(IN4153A)
(9002)
U30
U32
C41
.22
50V
-12V
C40
.01
R77
220K
R78
33K
R79
15K
U9
(747)
R82
820
C42
.01
VR3
(IN746A)
U35-6
3 C3
TP3
C44
1.0
50V
R90
10K
R31
2 F3
C47
.022
100V
C48
.022
100V
46 CT
C45
1.0
50V
R91
10K
27 DVRNGS
1.6KHZ 47
25 CT
R83
680K
U21-8
3 E3
CR4
(IN4153A)
U3
(747)
CR5
(IN4153A)
C43
10
50V
C54
10
50V
R84
1K
TP2
R89
6810
±1%
.1W
R92
10K
C38
3300PF
C39
.01
R103
22M
R85
100K
±1%
.1W
R88
12.1K
±1%
.1W
C46
3300PF
U15-4
5 C4
R93
470
CABFLT 15
16
R80
1 MEG
R81
383K
±1%
.1W
R86
20K
R87
330
-12V
CR6
(IN4153A)
CR7
(IN4153A)
R94
56K
C49
1000PF
U4
(710)
C50
.01
R106
3.9K
VR4
(IN753)
C51
.01
44 AVCTOI

Figure FO-16. AVOW card 21A10, schematic diagram (sheet 4 of 5)

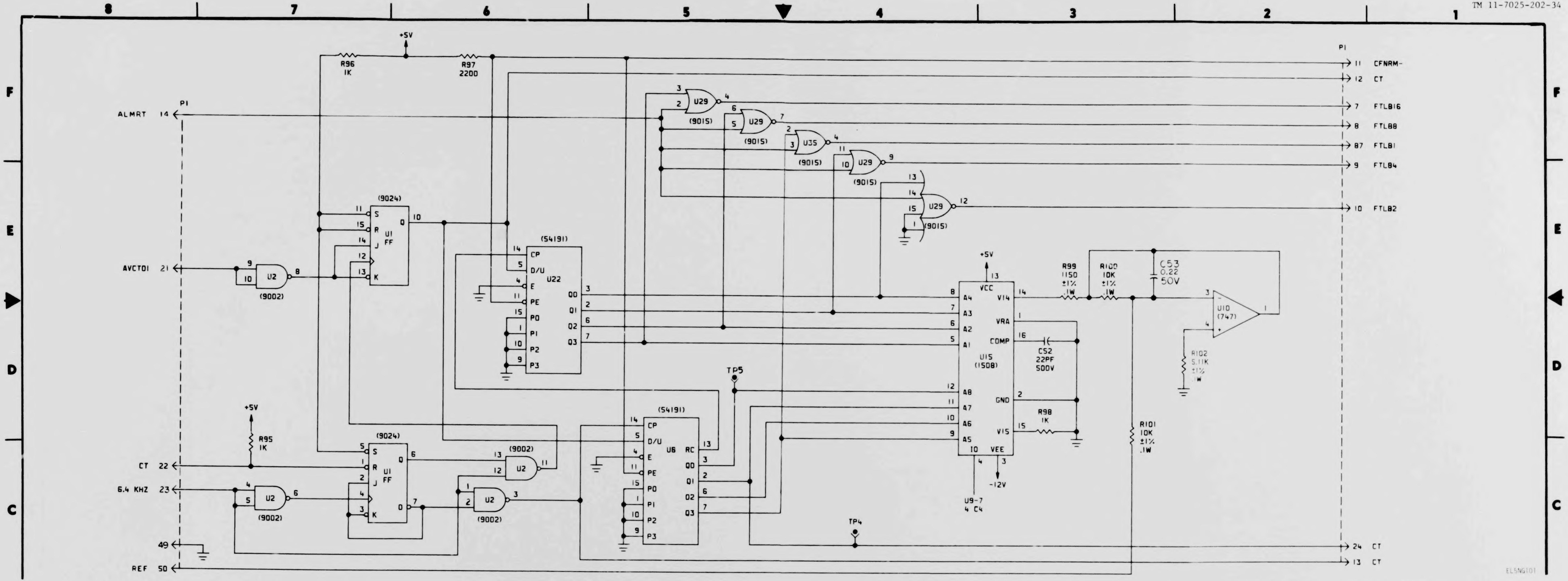

8
7
6
5
4
3
2
1
F
E
D
C
+5V
R96
1K
R97
2200
P1
11 CFNRM-
12 CT
7 FTLB16
8 FTLB8
87 FTLB1
9 FTLB4
10 FTLB2
ALMRT 14
U29
(9015)
U35
(9015)
(9024)
U1
FF
S
R
J
K
Q
AVCT01 21
U2
(9002)
(S4191)
U22
CP
D/U
E
PE
P0
P1
P2
P3
Q0
Q1
Q2
Q3
+5V
VCC
V14
VRA
COMP
U15
(1508)
GND
V15
VEE
A1
A2
A3
A4
A5
A6
A7
A8
R99
1150
±1%
.1W
R100
10K
±1%
.1W
C53
0.22
50V
U10
(747)
C52
22PF
500V
R102
5.11K
±1%
.1W
R98
1K
R101
10K
±1%
.1W
-12V
U9-7
4 C4
TP5
TP4
(S4191)
U6
RC
R95
1K
CT 22
6.4 KHZ 23
49
REF 50
24 CT
13 CT
EL5NG101

Figure FO-16. AVOW card 21A10, schematic diagram (sheet 5 of 5)

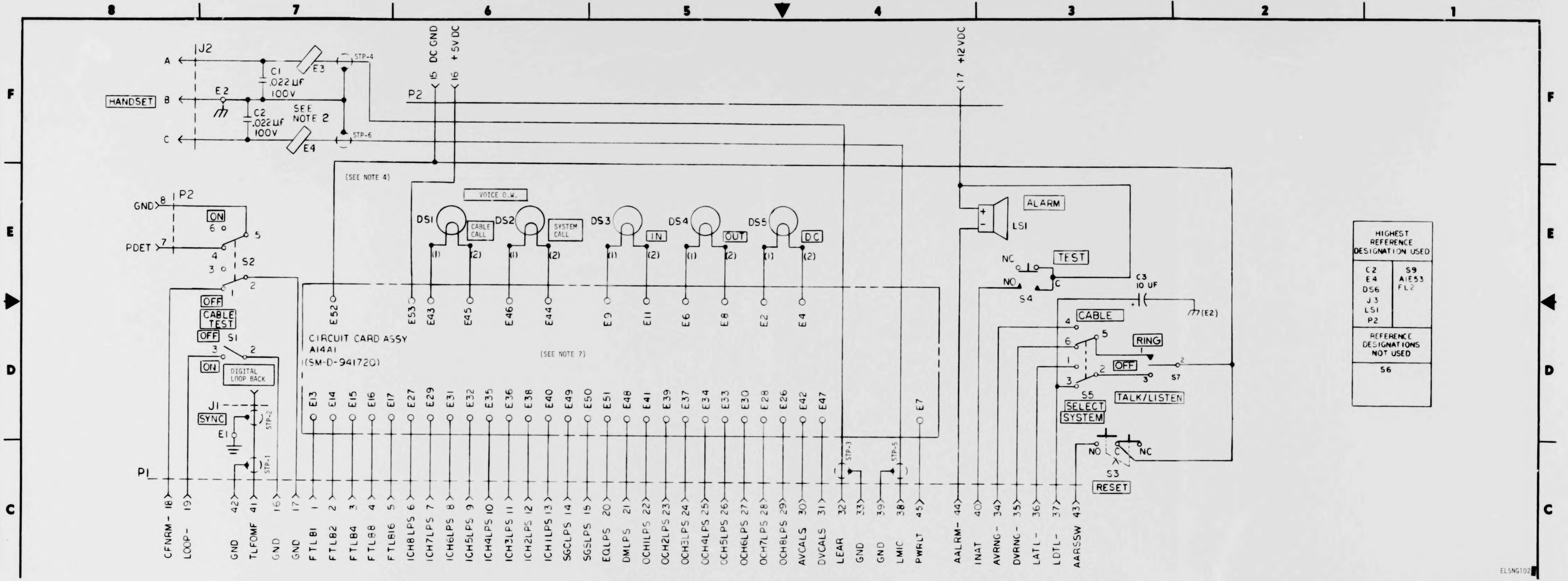
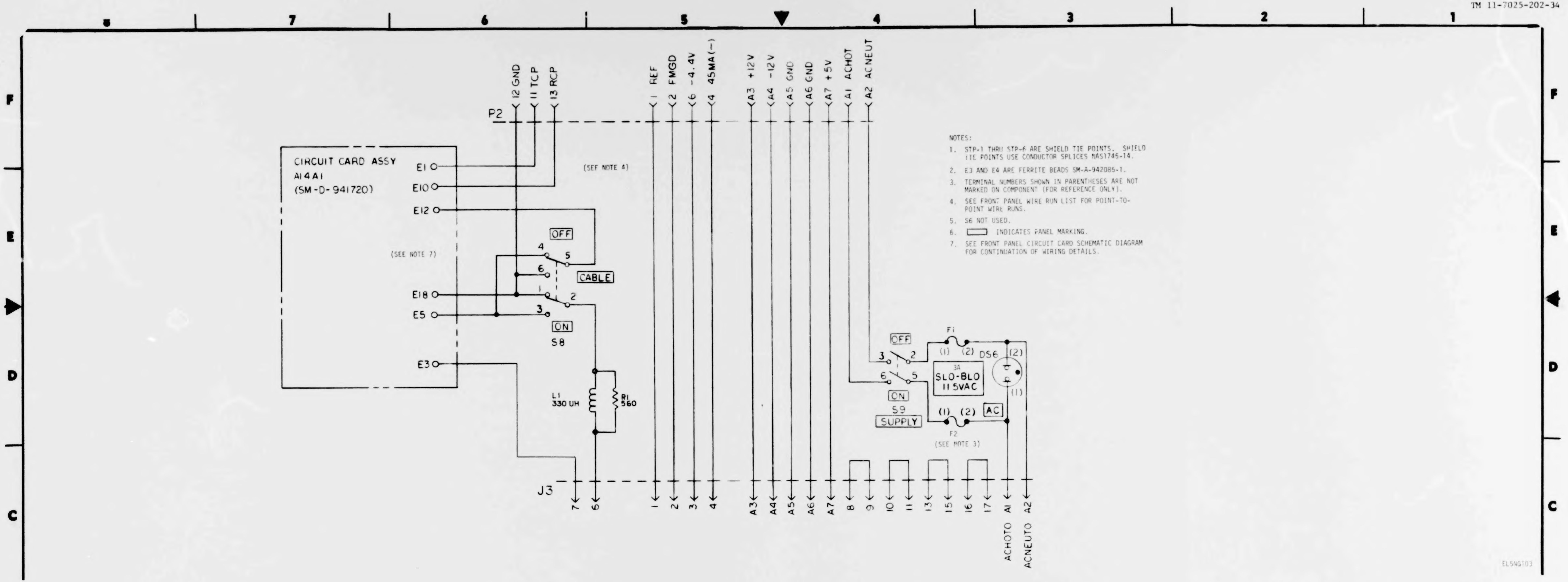

8
7
6
5
4
3
2
1
F
E
D
C
J2
A
B
C
HANDSET
E2
C1 .022 µf 100V
C2 .022 µf 100V
E3
E4
STP-4
STP-6
SEE NOTE 2
15 DC GND
16 +5VDC
17 +12VDC
P2
(SEE NOTE 4)
VOICE O.W.
DS1
CABLE CALL
DS2
SYSTEM CALL
DS3
IN
DS4
OUT
DS5
DC
(1)
(2)
GND 8
PDET 7
ON
S2
OFF
CABLE TEST
S1
DIGITAL LOOP BACK
J1
SYNC
E1
STP-2
STP-1
STP-3
STP-5
E52
E53
E43
E45
E46
E44
E9
E11
E6
E8
E2
E4
CIRCUIT CARD ASSY
A14A1
(SM-D-941720)
(SEE NOTE 7)
E13
E14
E15
E16
E17
E27
E29
E31
E32
E35
E36
E38
E40
E49
E50
E51
E48
E41
E39
E37
E34
E33
E30
E28
E26
E42
E47
E7
P1
CFNRM- 18
LOOP- 19
GND 42
TLFOMF 41
GND 16
GND 17
FTLB1 1
FTLB2 2
FTLB4 3
FTLB8 4
FTLB16 5
ICH8LPS 6
ICH7LPS 7
ICH6LPS 8
ICH5LPS 9
ICH4LPS 10
ICH3LPS 11
ICH2LPS 12
ICH1LPS 13
SGCLPS 14
SGSLPS 15
EQLPS 20
DMLPS 21
OCH1LPS 22
OCH2LPS 23
OCH3LPS 24
OCH4LPS 25
OCH5LPS 26
OCH6LPS 27
OCH7LPS 28
OCH8LPS 29
AVCALS 30
DVCALS 31
LEAR 32
GND 33
GND 39
LMIC 38
PWFLT 45
AALRM- 44
INAT 40
AVRNG- 34
DVRNG- 35
LATL- 36
LDTL- 37
AARSSW 43
ALARM
LS1
TEST
NC
NO
C
S4
C3 10 UF
(E2)
CABLE
RING
OFF
S7
TALK/LISTEN
S5
SELECT SYSTEM
S3
RESET
HIGHEST REFERENCE DESIGNATION USED
C2
E4
DS6
J3
LS1
P2
S9
A1E53
FL2
REFERENCE DESIGNATIONS NOT USED
S6
EL5NG102

Figure FO-17. Front panel 21A14, schematic diagram (sheet 1 of 2).


8
7
6
5
4
3
2
1
F
E
D
C
P2
12 GND
11 TCP
13 RCP
1 REF
2 FMGD
6 -4.4V
4 45MA(-)
A3 +12V
A4 -12V
A5 GND
A6 GND
A7 +5V
A1 ACHOT
A2 ACNEUT
CIRCUIT CARD ASSY
A14A1
(SM-D-941720)
E1
E10
E12
E18
E5
E3
(SEE NOTE 4)
(SEE NOTE 7)
OFF
CABLE
ON
S8
4
5
6
1
2
3
L1
330 UH
R1
560
OFF
ON
S9
SUPPLY
F1
(1)
(2)
3A
SLO-BLO
115VAC
DS6
AC
F2
(SEE NOTE 3)
J3
7
6
1
2
3
4
A3
A4
A5
A6
A7
8
9
10
11
13
15
16
17
A1
A2
ACHOTO
ACNEUTO
EL5NG103

NOTES:

1. STP-1 THRU STP-6 ARE SHIELD TIE POINTS. SHIELD TIE POINTS USE CONDUCTOR SPLICES NAS1745-14.
2. E3 AND E4 ARE FERRITE BEADS SM-A-942085-1.
3. TERMINAL NUMBERS SHOWN IN PARENTHESES ARE NOT MARKED ON COMPONENT (FOR REFERENCE ONLY).
4. SEE FRONT PANEL WIRE RUN LIST FOR POINT-TO-POINT WIRE RUNS.
5. S6 NOT USED.
6. ▭ INDICATES PANEL MARKING.
7. SEE FRONT PANEL CIRCUIT CARD SCHEMATIC DIAGRAM FOR CONTINUATION OF WIRING DETAILS.

Figure FO-17. Front panel 21A14, schematic diagram (sheet 2 of 2).

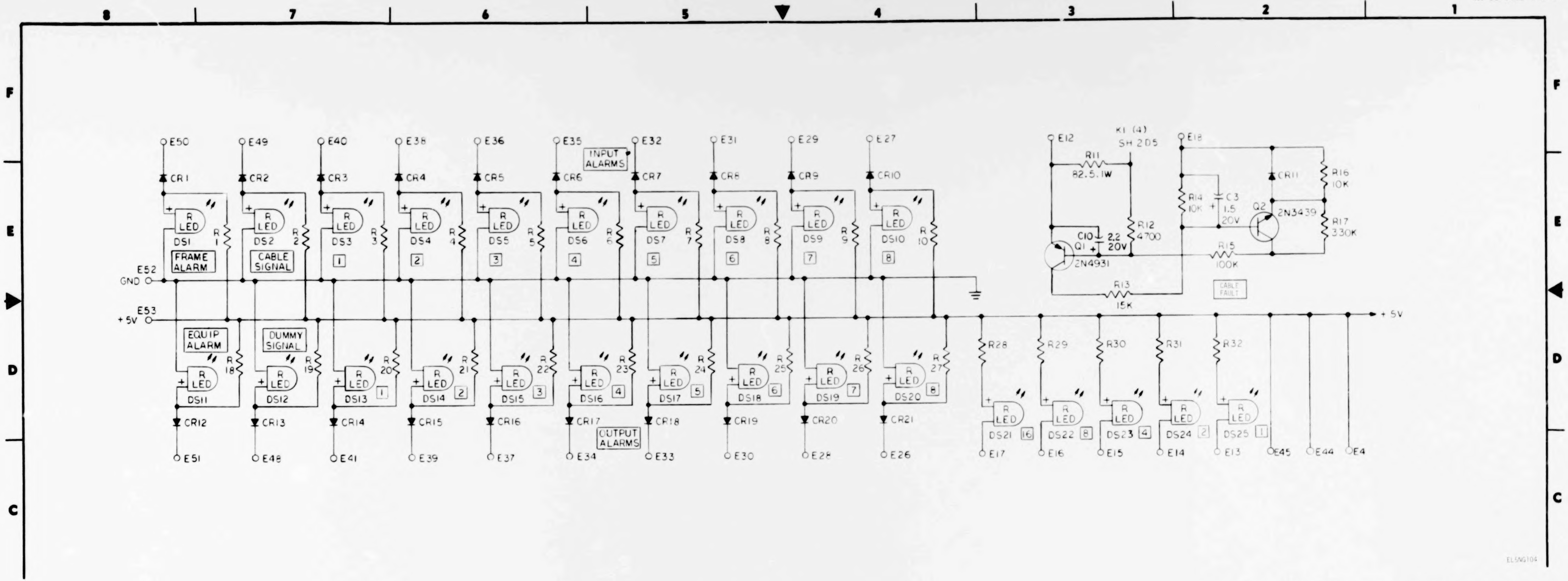
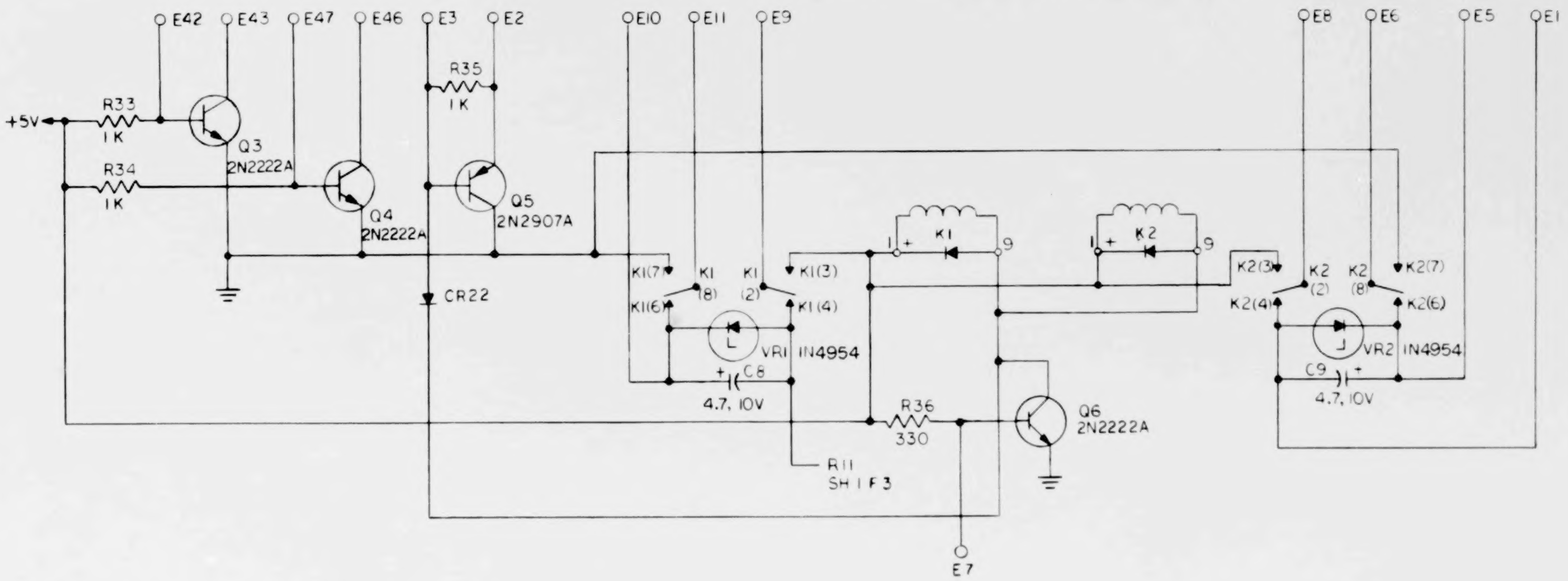

8
7
6
5
4
3
2
1
F
E
D
C
E50
E49
E40
E38
E36
E35
E32
E31
E29
E27
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
INPUT ALARMS
R LED
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
FRAME ALARM
CABLE SIGNAL
1
2
3
4
5
6
7
8
E52
GND
E53
+5V
EQUIP ALARM
DUMMY SIGNAL
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
DS11
DS12
DS13
DS14
DS15
DS16
DS17
DS18
DS19
DS20
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR21
OUTPUT ALARMS
E51
E48
E41
E39
E37
E34
E33
E30
E28
E26
E12
K1 (4)
SH 2D5
R11
82.5, 1W
R12
4700
C10
2.2
20V
Q1
2N4931
R13
15K
E18
R14
10K
C3
1.5
20V
CR11
Q2
2N3439
R16
10K
R17
330K
R15
100K
CABLE FAULT
+5V
R28
R29
R30
R31
R32
DS21
DS22
DS23
DS24
DS25
16
8
4
2
1
E17
E16
E15
E14
E13
E45
E44
E4
EL5NG104

Figure FO-18. Front panel circuit card 21A14A1, schematic diagram (sheet 1 of 2).


E42
E43
E47
E46
E3
E2
E10
E11
E9
E8
E6
E5
E1
+5V
R33
1K
R34
1K
Q3
2N2222A
Q4
2N2222A
R35
1K
Q5
2N2907A
CR22
K1(7)
K1(6)
K1
(8)
K1
(2)
K1(3)
K1(4)
VR1 1N4954
C8
4.7, 10V
K1
1
9
K2
1
9
K2(3)
K2(4)
K2
(2)
K2
(8)
K2(7)
K2(6)
VR2 1N4954
C9
4.7, 10V
R36
330
Q6
2N2222A
R11
SH 1 F3
E7

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NO. AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATIONS.

2. ALL LIGHT EMITTING DIODES DS1 — DS25 ARE SM-A-942039.

3. ALL RESISTORS ARE IN OHMS, ±5 PERCENT, AND ARE 1K UNLESS OTHERWISE SPECIFIED.

4. TERMINAL NUMBERS IN PARENTHESES ARE REFERENCE INFORMATION AND ARE NOT MARKED ON THE COMPONENTS.

5. ENCLOSED LEGENDS INDICATE ACTUAL MARKING ON EQUIPMENT.

6. ALL DIODES ARE 1N4153-1 UNLESS OTHERWISE SPECIFIED.

HIGHEST REF DESIGNATION		
C10	R36	
E53	CR22	
K2	DS25	
	VR2	
Q6		
REF DESIGNATIONS NOT USED		
C4-C7	C1,C2	
E19-E29		

Figure FO-18. Front panel circuit card 21A14A1, schematic diagram (sheet 2 of 2).

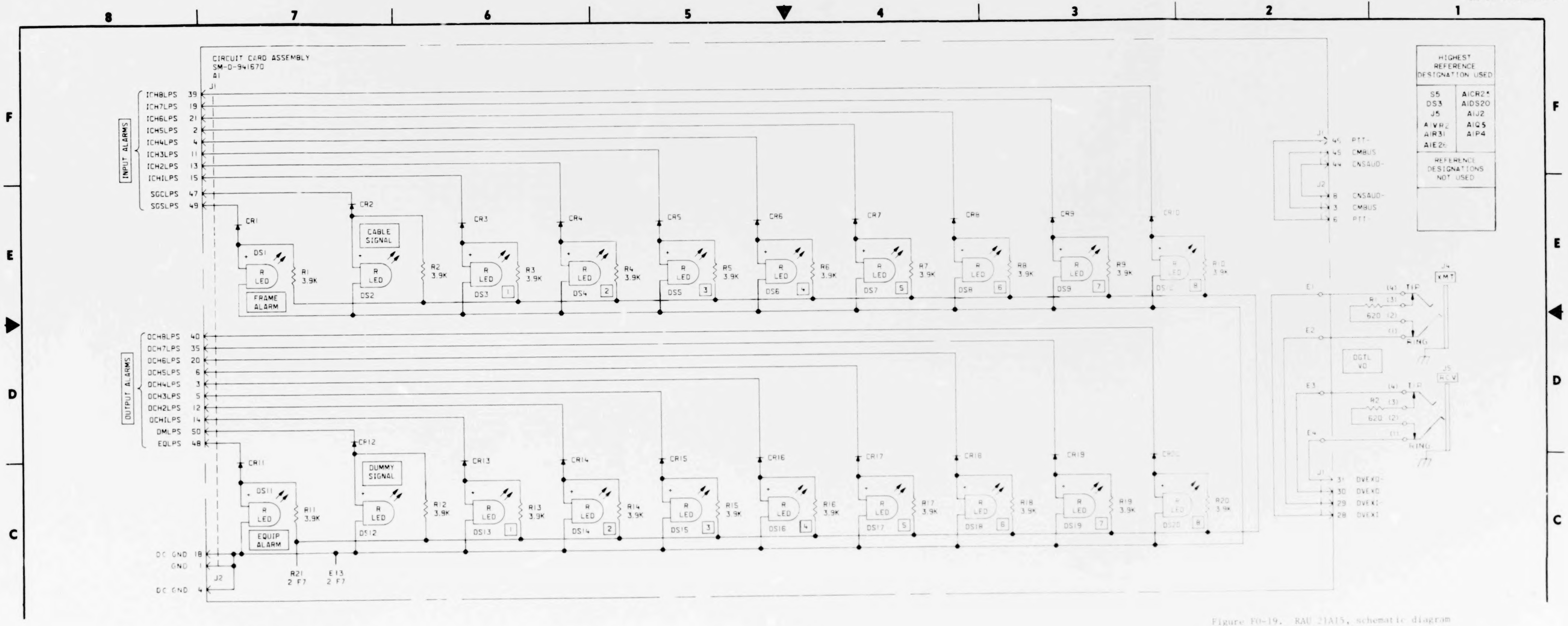
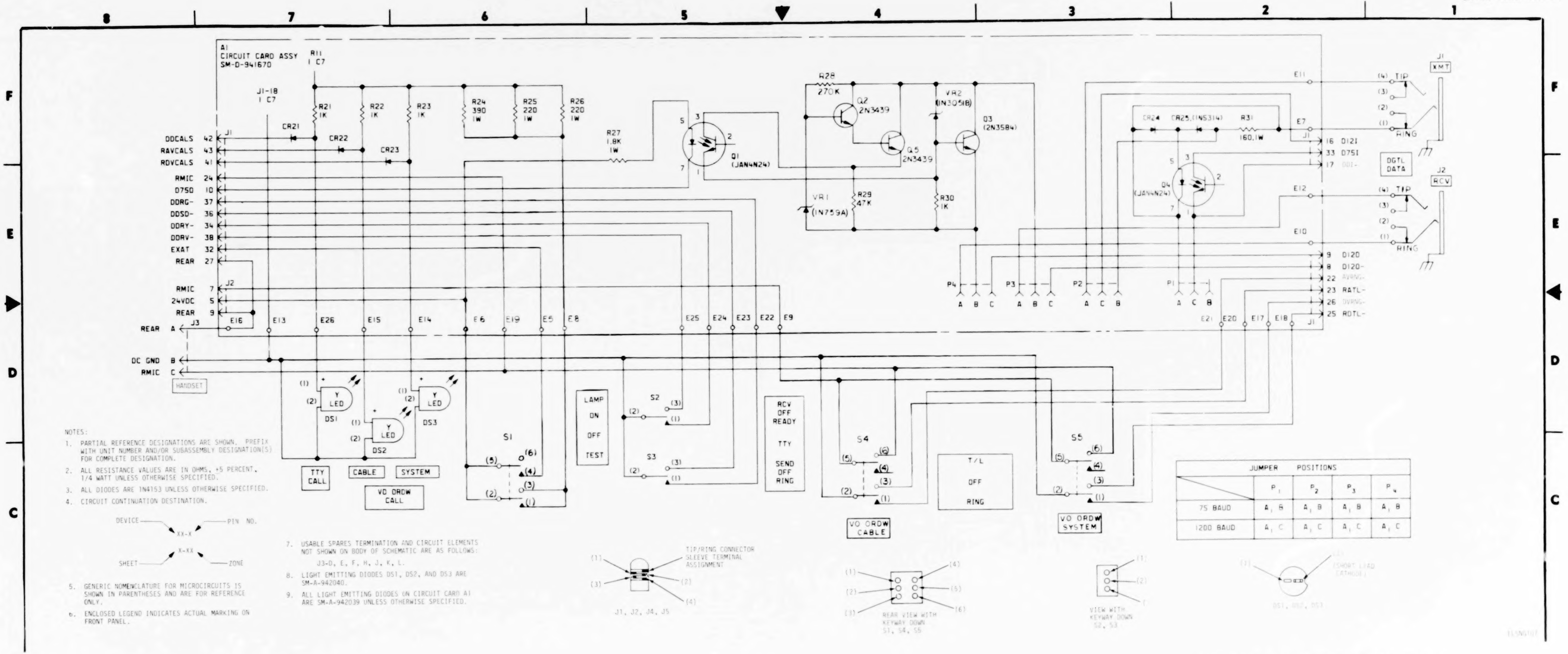

8
7
6
5
4
3
2
1
F
E
D
C
CIRCUIT CARD ASSEMBLY
SM-D-941670
A1
J1
INPUT ALARMS
ICH8LPS 39
ICH7LPS 19
ICH6LPS 21
ICH5LPS 2
ICH4LPS 4
ICH3LPS 11
ICH2LPS 13
ICH1LPS 15
SGCLPS 47
SGSLPS 49
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
DS1
R LED
R1 3.9K
FRAME ALARM
CABLE SIGNAL
DS2
R2 3.9K
DS3
R3 3.9K
DS4
R4 3.9K
DS5
R5 3.9K
DS6
R6 3.9K
DS7
R7 3.9K
DS8
R8 3.9K
DS9
R9 3.9K
DS10
R10 3.9K
1
2
3
4
5
6
7
8
OUTPUT ALARMS
OCH8LPS 40
OCH7LPS 35
OCH6LPS 20
OCH5LPS 6
OCH4LPS 3
OCH3LPS 5
OCH2LPS 12
OCH1LPS 14
DMLPS 50
EQLPS 48
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
DS11
R11 3.9K
EQUIP ALARM
DUMMY SIGNAL
DS12
R12 3.9K
DS13
R13 3.9K
DS14
R14 3.9K
DS15
R15 3.9K
DS16
R16 3.9K
DS17
R17 3.9K
DS18
R18 3.9K
DS19
R19 3.9K
DS20
R20 3.9K
DC GND 18
GND 1
DC GND 4
J2
R21 2 F7
E13 2 F7
J1
45 PTT-
45 CMBUS
44 CNSAUD-
J2
8 CNSAUD-
3 CMBUS
6 PTT-
HIGHEST REFERENCE DESIGNATION USED
S5
DS3
J5
A1VR2
A1R31
A1E26
A1CR21
A1DS20
A1J2
A1Q5
A1P4
REFERENCE DESIGNATIONS NOT USED
J4
XMT
E1
E2
(4) TIP
R1 (3)
620 (2)
(1)
RING
DGTL VD
J5
RCV
E3
E4
(4) TIP
R2 (3)
620 (2)
(1)
RING
J1
31 DVEXO-
30 DVEXO
29 DVEXI-
28 DVEXI

Figure FO-19. RAU 21A15, schematic diagram (sheet 1 of 2).


8
7
6
5
4
3
2
1
F
E
D
C
A1
CIRCUIT CARD ASSY
SM-D-941670
R11
1 C7
J1-18
1 C7
R21 1K
R22 1K
R23 1K
R24 390 1W
R25 220 1W
R26 220 1W
CR21
CR22
CR23
DDCALS 42
RAVCALS 43
RDVCALS 41
RMIC 24
D75O 10
DDRG- 37
DDSD- 36
DDRY- 34
DDRV- 38
EXAT 32
REAR 27
J1
J2
RMIC 7
24VDC 5
REAR 9
REAR A
J3
DC GND B
RMIC C
HANDSET
E16
E13
E26
E15
E14
E6
E19
E5
E8
E25
E24
E23
E22
E9
R27 1.8K 1W
Q1 (JAN4N24)
R28 270K
Q2 2N3439
Q5 2N3439
VR2 (1N3051B)
Q3 (2N3584)
VR1 (1N759A)
R29 47K
R30 1K
CR24
CR25 (1N5314)
R31 160,1W
Q4 (JAN4N24)
E11
E7
E12
E10
E21
E20
E17
E18
16 DI2I
33 D75I
17 DDI-
DGTL DATA
9 DI2O
8 DI2O-
22 AVRNG-
23 RATL-
26 DVRNG-
25 RDTL-
J1 XMT
J2 RCV
TIP
RING
P4
P3
P2
P1
A B C
DS1
DS2
DS3
Y LED
TTY CALL
CABLE
SYSTEM
VO ORDW CALL
S1
LAMP ON OFF TEST
S2
S3
RCV OFF READY
TTY
SEND OFF RING
S4
VO ORDW CABLE
T/L
OFF
RING
S5
VO ORDW SYSTEM
TIP/RING CONNECTOR SLEEVE TERMINAL ASSIGNMENT
J1, J2, J4, J5
REAR VIEW WITH KEYWAY DOWN S1, S4, S5
VIEW WITH KEYWAY DOWN S2, S3
(SHORT LEAD CATHODE)
DS1, DS2, DS3
EL5NG107

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5 PERCENT, 1/4 WATT UNLESS OTHERWISE SPECIFIED.
3. ALL DIODES ARE 1N4153 UNLESS OTHERWISE SPECIFIED.
4. CIRCUIT CONTINUATION DESTINATION.

DEVICE — XX-X — PIN NO.
SHEET — X-XX — ZONE

5. GENERIC NOMENCLATURE FOR MICROCIRCUITS IS SHOWN IN PARENTHESES AND ARE FOR REFERENCE ONLY.
6. ENCLOSED LEGEND INDICATES ACTUAL MARKING ON FRONT PANEL.
7. USABLE SPARES TERMINATION AND CIRCUIT ELEMENTS NOT SHOWN ON BODY OF SCHEMATIC ARE AS FOLLOWS:

   J3-D, E, F, H, J, K, L.

8. LIGHT EMITTING DIODES DS1, DS2, AND DS3 ARE SM-A-942040.
9. ALL LIGHT EMITTING DIODES ON CIRCUIT CARD A1 ARE SM-A-942039 UNLESS OTHERWISE SPECIFIED.

JUMPER POSITIONS

	P_1	P_2	P_3	P_4
75 BAUD	A, B	A, B	A, B	A, B
1200 BAUD	A, C	A, C	A, C	A, C

Figure FO-19. RAU 21A15, schematic diagram (sheet 2 of 2).

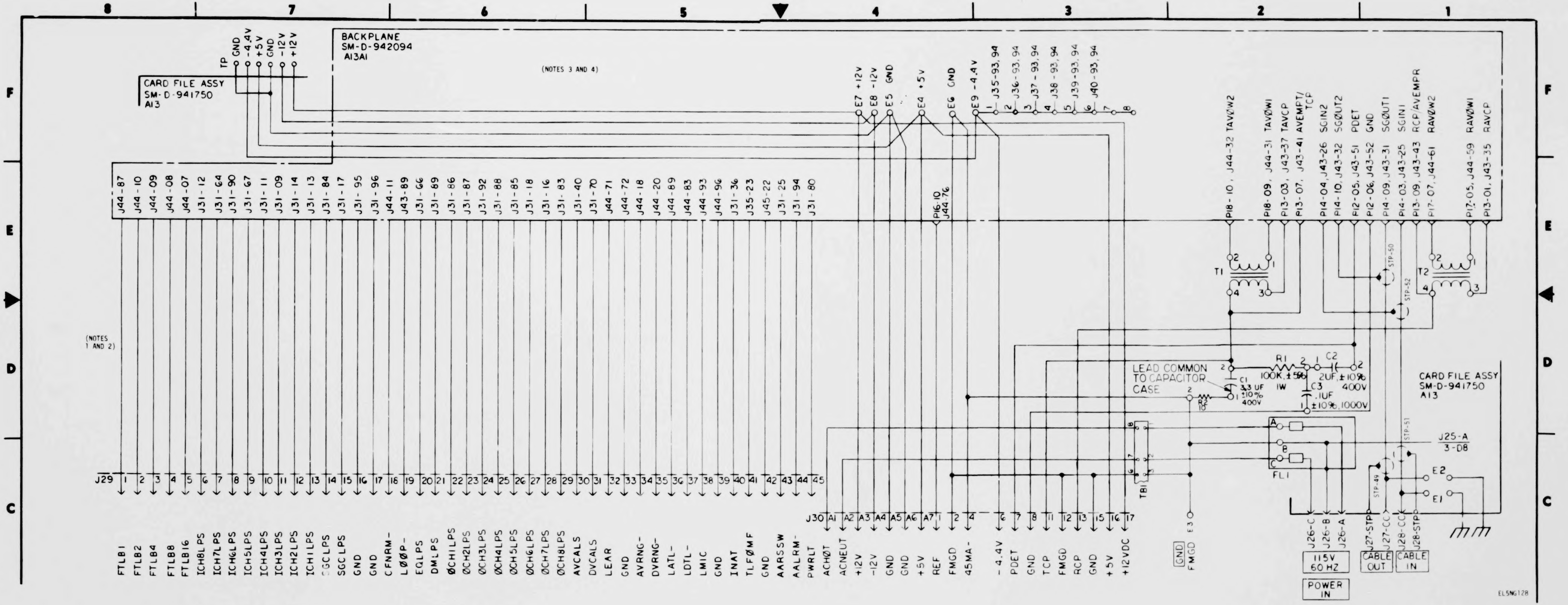
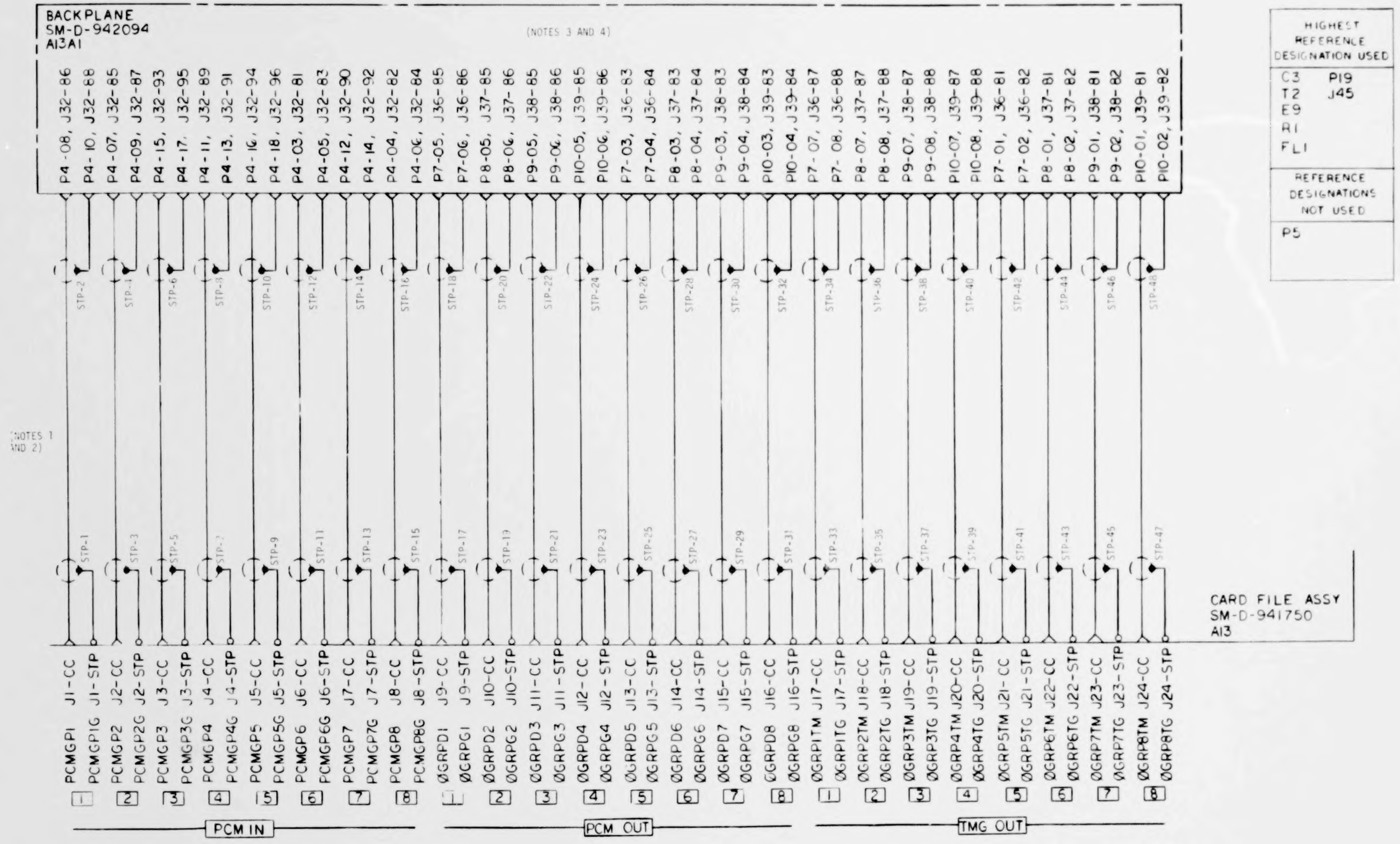

8
7
6
5
4
3
2
1
F
E
D
C
BACKPLANE
SM-D-942094
A13A1
CARD FILE ASSY
SM-D-941750
A13
TP
GND
-4.4V
+5V
GND
-12V
+12V
(NOTES 3 AND 4)
E7 +12V
E8 -12V
E5 GND
E4 +5V
E6 GND
E9 -4.4V
J35-93, 94
J36-93, 94
J37-93, 94
J38-93, 94
J39-93, 94
J40-93, 94
P16-10
J44-76
J44-87
J44-10
J44-09
J44-08
J44-07
J31-12
J31-64
J31-90
J31-67
J31-11
J31-09
J31-14
J31-13
J31-84
J31-17
J31-95
J31-96
J44-11
J43-89
J31-66
J31-89
J31-86
J31-87
J31-92
J31-88
J31-85
J31-18
J31-16
J31-83
J31-40
J31-70
J44-71
J44-72
J44-18
J44-20
J44-89
J44-83
J44-93
J44-96
J31-36
J35-23
J45-22
J31-25
J31-94
J31-80
P18-10, J44-32 TAVØW2
P18-09, J44-31 TAVØW1
P13-03, J43-37 TAVCP
P13-07, J43-41 AVEMPT/TCP
P14-04, J43-26 SGIN2
P14-10, J43-32 SGØUT2
P12-05, J43-51 PDET
P12-06, J43-52 GND
P14-09, J43-31 SGØUT1
P14-03, J43-25 SGIN1
P13-09, J43-43 RCP/AVEMPR
P17-07, J44-61 RAVØW2
P17-05, J44-59 RAVØW1
P13-01, J43-35 RAVCP
T1
T2
STP-50
STP-52
STP-51
STP-49
(NOTES 1 AND 2)
LEAD COMMON TO CAPACITOR CASE
C1 3.3 UF ±10% 400V
R1 100K, ±5% 1W
C2 2UF, ±10% 400V
C3 .1UF ±10%, 1000V
R2 10
CARD FILE ASSY
SM-D-941750
A13
TB1
FL1
A
B
C
J25-A
3-D8
E2
E1
E3
J29
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45
FTLB1
FTLB2
FTLB4
FTLB8
FTLB16
ICH8LPS
ICH7LPS
ICH6LPS
ICH5LPS
ICH4LPS
ICH3LPS
ICH2LPS
ICH1LPS
SGCLPS
SGCLPS
GND
GND
CFNRM-
LØØP-
EGLPS
DMLPS
ØCH1LPS
ØCH2LPS
ØCH3LPS
ØCH4LPS
ØCH5LPS
ØCH6LPS
ØCH7LPS
ØCH8LPS
AVCALS
DVCALS
LEAR
GND
AVRNG-
DVRNG-
LATL-
LDTL-
LMIC
GND
INAT
TLFØMF
GND
AARSSW
AALRM-
PWRLT
J30
A1 A2 A3 A4 A5 A6 A7 1 2 4 6 7 8 11 12 13 15 16 17
ACHØT
ACNEUT
+12V
-12V
GND
GND
+5V
REF
FMGD
45MA-
-4.4V
PDET
GND
TCP
FMGD
RCP
GND
+5V
+12VDC
GND
FMGD
J26-C
J26-B
J26-A
J27-STP
J27-CC
J28-CC
J28-STP
115V 60 HZ
POWER IN
CABLE OUT
CABLE IN
EL5NG128

Figure FO-20. Card file, schematic diagram (sheet 1 of 3).

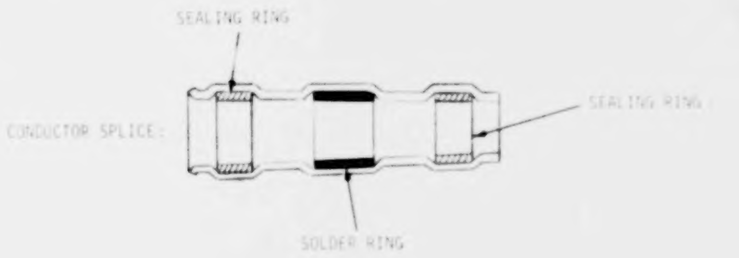

8
7
6
5
4
3
2
1
F
E
D
C
BACKPLANE
SM-D-942094
A13A1
(NOTES 3 AND 4)
P4-08, J32-86
P4-10, J32-88
P4-07, J32-85
P4-09, J32-87
P4-15, J32-93
P4-17, J32-95
P4-11, J32-89
P4-13, J32-91
P4-16, J32-94
P4-18, J32-96
P4-03, J32-81
P4-05, J32-83
P4-12, J32-90
P4-14, J32-92
P4-04, J32-82
P4-06, J32-84
P7-05, J36-85
P7-06, J36-86
P8-05, J37-85
P8-06, J37-86
P9-05, J38-85
P9-06, J38-86
P10-05, J39-85
P10-06, J39-86
P7-03, J36-83
P7-04, J36-84
P8-03, J37-83
P8-04, J37-84
P9-03, J38-83
P9-04, J38-84
P10-03, J39-83
P10-04, J39-84
P7-07, J36-87
P7-08, J36-88
P8-07, J37-87
P8-08, J37-88
P9-07, J38-87
P9-08, J38-88
P10-07, J39-87
P10-08, J39-88
P7-01, J36-81
P7-02, J36-82
P8-01, J37-81
P8-02, J37-82
P9-01, J38-81
P9-02, J38-82
P10-01, J39-81
P10-02, J39-82
STP-2
STP-4
STP-6
STP-8
STP-10
STP-12
STP-14
STP-16
STP-18
STP-20
STP-22
STP-24
STP-26
STP-28
STP-30
STP-32
STP-34
STP-36
STP-38
STP-40
STP-42
STP-44
STP-46
STP-48
(NOTES 1 AND 2)
STP-1
STP-3
STP-5
STP-7
STP-9
STP-11
STP-13
STP-15
STP-17
STP-19
STP-21
STP-23
STP-25
STP-27
STP-29
STP-31
STP-33
STP-35
STP-37
STP-39
STP-41
STP-43
STP-45
STP-47
CARD FILE ASSY
SM-D-941750
A13
PCMGP1 J1-CC
PCMGP1G J1-STP
PCMGP2 J2-CC
PCMGP2G J2-STP
PCMGP3 J3-CC
PCMGP3G J3-STP
PCMGP4 J4-CC
PCMGP4G J4-STP
PCMGP5 J5-CC
PCMGP5G J5-STP
PCMGP6 J6-CC
PCMGP6G J6-STP
PCMGP7 J7-CC
PCMGP7G J7-STP
PCMGP8 J8-CC
PCMGP8G J8-STP
ØGRPD1 J9-CC
ØGRPG1 J9-STP
ØGRPD2 J10-CC
ØGRPG2 J10-STP
ØGRPD3 J11-CC
ØGRPG3 J11-STP
ØGRPD4 J12-CC
ØGRPG4 J12-STP
ØGRPD5 J13-CC
ØGRPG5 J13-STP
ØGRPD6 J14-CC
ØGRPG6 J14-STP
ØGRPD7 J15-CC
ØGRPG7 J15-STP
ØGRPD8 J16-CC
ØGRPG8 J16-STP
ØGRP1TM J17-CC
ØGRP1TG J17-STP
ØGRP2TM J18-CC
ØGRP2TG J18-STP
ØGRP3TM J19-CC
ØGRP3TG J19-STP
ØGRP4TM J20-CC
ØGRP4TG J20-STP
ØGRP5TM J21-CC
ØGRP5TG J21-STP
ØGRP6TM J22-CC
ØGRP6TG J22-STP
ØGRP7TM J23-CC
ØGRP7TG J23-STP
ØGRP8TM J24-CC
ØGRP8TG J24-STP
1
2
3
4
5
6
7
8
1
2
3
4
5
6
7
8
1
2
3
4
5
6
7
8
PCM IN
PCM OUT
TMG OUT

HIGHEST REFERENCE DESIGNATION USED	
C3	P19
T2	J45
E9	
R1	
FL1	

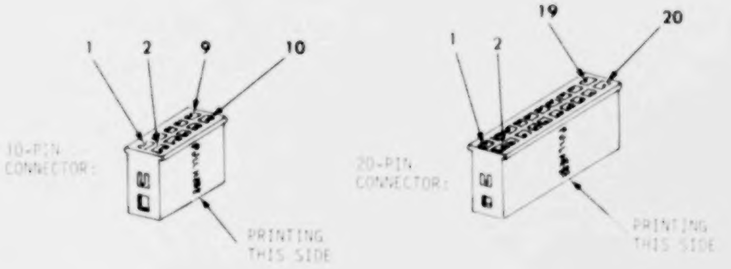
REFERENCE DESIGNATIONS NOT USED
P5

NOTES:

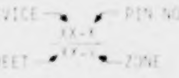
1. SEE CARD FILE WIRE RUN LIST FOR POINT-TO-POINT WIRE RUNS BETWEEN BACKPLANE AND OTHER COMPONENTS SHOWN ON SCHEMATIC.
2. STP-1 THRU STP-52 ARE SHIELD TIE POINTS. EACH SHIELD TIE POINT USES CONDUCTOR SPLICE MAS1745-14 TO CONNECT GROUND WIRE TO SHIELD.


SEALING RING
CONDUCTOR SPLICE:
SEALING RING
SOLDER RING

3. SEE BACKPLANE WIRE RUN LIST FOR POINT-TO-POINT WIRE RUNS BETWEEN CONNECTOR PINS ON BACKPLANE.
4. INTERFACE CONNECTORS P1, P3, P4, AND P15 ARE 20-PIN CONNECTORS. INTERFACE CONNECTORS P2, P6 THRU P14, AND P16 THRU P19 ARE 10-PIN CONNECTORS. SEE BACKPLANE CONNECTOR PIN LOCATION DIAGRAM FOR PIN LOCATION OF KEYING PLUG IN EACH INTERFACE CONNECTOR.


1
2
9
10
10-PIN CONNECTOR:
PRINTING THIS SIDE
1
2
19
20
20-PIN CONNECTOR:
PRINTING THIS SIDE

5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH UNIT NUMBER AND/OR SUBASSEMBLY DESIGNATION(S) FOR COMPLETE DESIGNATION.
6. CIRCUIT CONTINUATION DESTINATION:


DEVICE
PIN NO.
XX-X
XX-X
SHEET
ZONE

7. ☐ INDICATES PANEL MARKING.

Figure FO-20. Card file, schematic diagram (sheet 2 of 3).

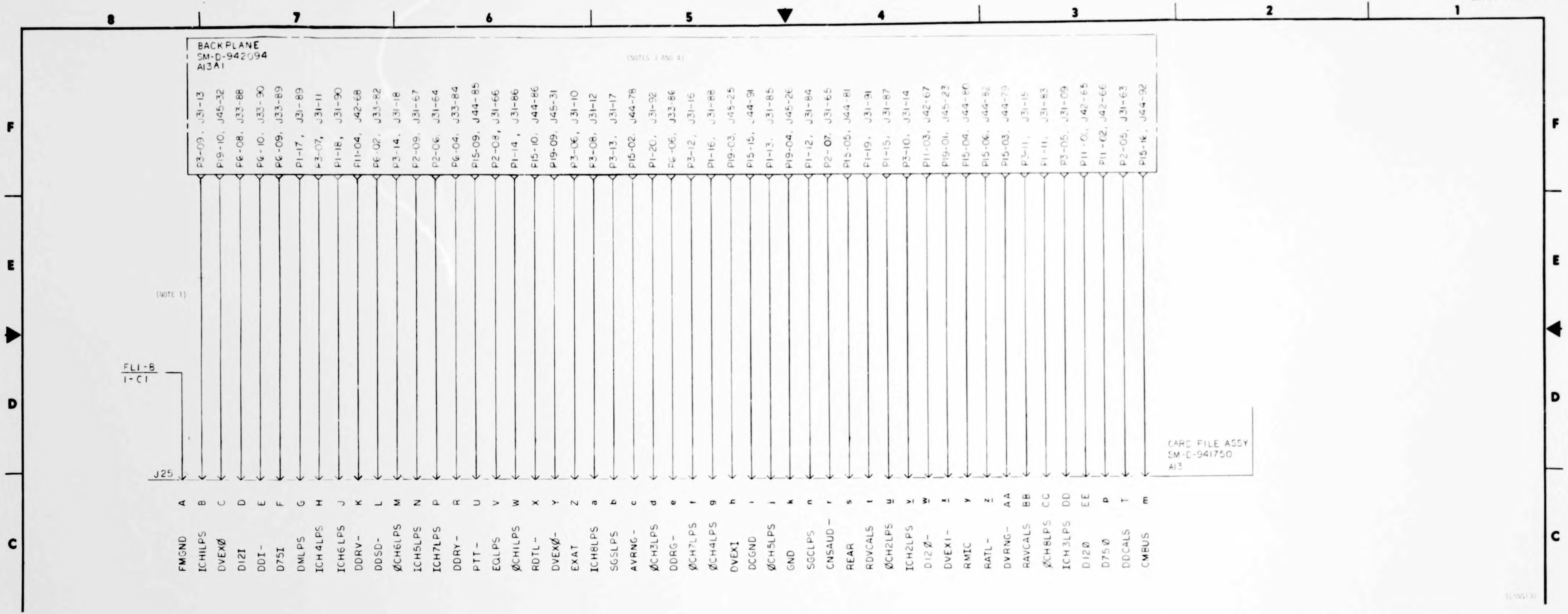

8
7
6
5
4
3
2
1
F
E
D
C
BACKPLANE
SM-D-942094
A13A1
(NOTES 3 AND 4)
P3-09, J31-13
P19-10, J45-32
P6-08, J33-88
P6-10, J33-90
P6-09, J33-89
P1-17, J31-89
P3-07, J31-11
P1-18, J31-90
P11-04, J42-68
P6-02, J33-82
P3-14, J31-18
P2-09, J31-67
P2-06, J31-64
P6-04, J33-84
P15-09, J44-85
P2-08, J31-66
P1-14, J31-86
P15-10, J44-86
P19-09, J45-31
P3-06, J31-10
P3-08, J31-12
P3-13, J31-17
P15-02, J44-78
P1-20, J31-92
P6-06, J33-86
P3-12, J31-16
P1-16, J31-88
P19-03, J45-25
P15-15, J44-91
P1-13, J31-85
P19-04, J45-26
P1-12, J31-84
P2-07, J31-65
P15-05, J44-81
P1-19, J31-91
P1-15, J31-87
P3-10, J31-14
P11-03, J42-67
P19-01, J45-23
P15-04, J44-80
P15-06, J44-82
P15-03, J44-79
P3-11, J31-15
P1-11, J31-83
P3-05, J31-09
P11-01, J42-65
P11-02, J42-66
P2-05, J31-63
P15-16, J44-92
(NOTE 1)
FL1-B
1-C1
J25
CARD FILE ASSY
SM-D-941750
A13
A FMGND
B ICH1LPS
C DVEXØ
D D12I
E DDI-
F D75I
G DMLPS
H ICH4LPS
J ICH6LPS
K DDRV-
L DDSD-
M ØCH6LPS
N ICH5LPS
P ICH7LPS
R DDRY-
U PTT-
V EQLPS
W ØCH1LPS
X RDTL-
Y DVEXØ-
Z EXAT
a ICH8LPS
b SGSLPS
c AVRNG-
d ØCH3LPS
e DDRG-
f ØCH7LPS
g ØCH4LPS
h DVEXI
i DCGND
j ØCH5LPS
k GND
n SGCLPS
r CNSAUD-
s REAR
t RDVCALS
u ØCH2LPS
v ICH2LPS
w D12Ø-
x DVEXI-
y RMIC
z RATL-
AA DVRNG-
BB RAVCALS
CC ØCH8LPS
DD ICH3LPS
EE D12Ø
p D75Ø
T DDCALS
m CMBUS

Figure FO-20. Card file, schematic diagram
(sheet 3 of 3).